DATA CONVERTERS

Product Catalog

INTRODUCTION

ILC Data Device Corporation (DDC) is a leading manufacturer of data conversion and MIL-STD-1553 data bus products including monolithic components, computer interfaces, instrumentation, power hybrid circuits, and solid-state power controllers. Headquartered in Bohemia, Long Island, New York, DDC occupies 166,000 square feet in the Airport International Plaza. A recent addition is a 27,500 square foot design and manufacturing facility in Ireland.

FACILITIES AND CAPABILITIES

DDC has one of the most modern thick- and thin-film hybrid manufacturing operations in the industry. Our quality system is in compliance with MIL-I-45208A, MIL-H-38534A, MIL-STD-883C, MIL-STD-1772, and MIL-STD-45662A. We are qualified as a QPL supplier of SEM (U.S. Navy Standard Electronic Modules) products to MIL-M-28787 and have provided equipment meeting the high-reliability levels required for manned space flight.

MIL-STD-1772 CERTIFIED FACILITY

DDC is listed on the first Qualified Manufacturers' List (QML) for Custom Hybrid Microcircuits under MIL-H-38534A. To obtain the QML status, DDC was certified and qualified by DESC. To achieve this distinction, DDC's facility including equipment, work instructions, documentation, revision control system, and personnel training were audited, certified, and qualified under the provisions of MIL-STD-1772.

DDC's Engineering Division is made up of a highly-specialized staff that engages in state-of-the-art analog and digital circuit design. Their capabilities include the design of: monolithic components, thick- and thin-film data-conversion hybrids, power hybrids, solid-state power controllers, computer interfaces, and test equipment. An extensive model shop is used for pilot production and experimental work.

DDC BACKGROUND

ILC Data Device Corporation was incorporated in 1964 as a supplier of high performance operational amplifiers. From its inception, emphasis has been place on state-of-the-art, high-quality data and signal conversion components and systems. In 1971 DDC was acquired by ILC Industries, sole supplier of the Apollo, Skylab, and Shuttle space suits. Since the acquisition, DDC has accelerated its progress in the data conversion field and today is the leading supplier of synchro conversion devices and MIL-STD-1553 equipment and is a dominant supplier of high-performance A/D and D/A conversion equipment. DDC's present capability includes diversification in the design and production of high-quality discrete and hybrid data conversion components and systems. This diversity in conjunction with research proficiency, manufacturing expertise, and strong customer support is responsible for DDC's recognized reputation for excellence.

DDC is conveniently located next to Long Island MacArthur Airport, which offers both non-stop service to most major east coast cities and convenient transportation to-and-from the two New York City airports.

HOW TO USE THIS CATALOG

DDC's Data Conversion Product Catalog is organized into fourteen sections labeled A through N. The Table of Contents identifies each section and lists the page number for each product. Each section contains a Product Summary Table that gives a brief description of the features of each product. Where useful, technical and application information have been included in the sections. Each product is described in an individual data sheet with all electrical and mechanical information included.

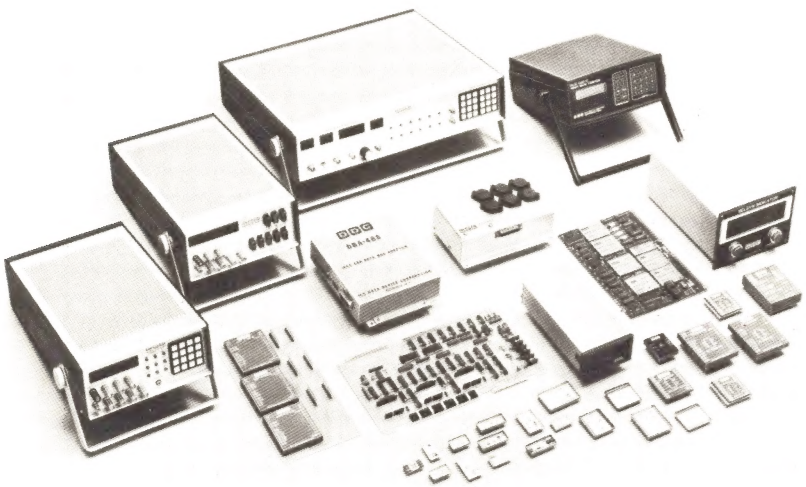
To locate a specific part number use the Product Index on the inside back cover to locate the page number of the desired part.

To locate a specific type of converter product use the Product Section thumb index on the first page to lead you to the desired section. The Product Summary Table will then guide you to the product(s) best serving your needs.

If you still have questions after reading this catalog, we invite you to contact our highly-trained factory Application Engineering staff or one of our Field Sales Representatives.

To locate a DDC office near you, refer to the back cover of this catalog.

A listing of Application Notes available from DDC can be found on the last page of this catalog.



DDC'S extensive product line, (samples shown at left) ranges from hybrid microcircuits through printed circuit assemblies and complex microprocessor based instruments.

SALE OFFICES

DDC maintains domestic regional sale offices in California, Virginia, and New Jersey. International offices are maintained in England, France, Germany, Sweden, and Japan. A Sales Representative force covers the rest of the United States, Canada, Western Europe, and the Far and Middle East.

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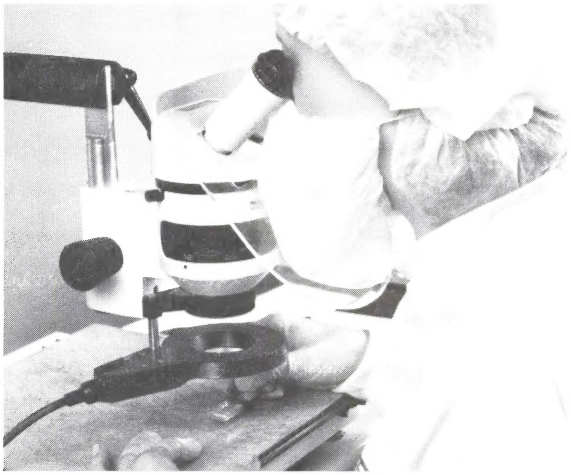
CAPABILITIES

ENGINEERING

DDC has a staff of highly-specialized engineers whose state-of-the-art design capabilities include: analog and digital circuits, computer interfaces, instrumentation, data conversion systems and thick- and thin-film hybrid design and packaging. Fundamental to DDC's leadership position in data conversion and MIL-STD-1553 data bus electronics is a fully-equipped engineering department that designs proprietary products, custom electronics, subsystems, and systems. Development and fabrication capabilities include two model shops (thick-film hybrid and discrete) plus a fully-equipped laboratory. A modern design and drafting department includes extensive CAD (Computer Aided Design) facilities. Approximately 25 percent of DDC is dedicated to engineering, an exceptionally high percentage for a manufacturing company. In addition, the percentage of our employees involved in engineering is very high, reflecting DDC's dedication to stringent-performance, high-reliability programs requiring specialized engineering talents.

Capabilities of the Engineering Department include: initial design, breadboard fabrication and testing, prototype assembly and evaluation, system and subsystem design, and a pilot production fabrication and testing capability of several million dollars annually. Maintaining two model shops (thick-film hybrid and discrete) yields a quick reaction capability for deliverable products, and allows product evaluation and development with minimal impact upon a continuous production line. New designs and products can be thoroughly tested prior to release to manufacturing.

Design and drafting facilities, including CAD, in a well lit, open area permits DDC to do its own original artwork for printed circuit boards, thick- and thin-film hybrids, and monolithics in addition to the normal product engineering and drafting requirements the electronics industry demands. A full documentation system is in place along with reproduction facilities, which use both ozalid and xerography for print duplication and distribution. With the use of a microfilm system, DDC has access to a complete range of military, industrial, and commercial standards, specifications, and handbooks.



PRODUCT ASSURANCE AND QUALITY CONTROL

At DDC, the Product Assurance function is headed by a Vice-President. He has sole responsibility for Product Assurance and reports directly to the President. This ensures independent actions, maintaining quality, reliability, and maintainability of DDC's products.

MIL-STDS-1772 AND 883

DDC's concern for quality starts at the proposal stage, with a thorough review of specifications and drawings, to establish work instructions and Product Assurance Plans. These plans assure proper monitoring throughout all stages of design, fabrication, and test. The DDC quality system complies with MIL-I-45208A, MIL-H-38534A, MIL-STD-883C, MIL-STD-1772, MIL-STD-45662A, and DDC's Product Assurance Manual. In the hybrid manufacturing area, specifications MIL-H-38534A and MIL-STD-883 establish workmanship standards. In the discrete manufacturing area, standards are set with MIL-STD-454 and MIL-STD-275. The calibration system is based upon MIL-STD-45662A.

The Reliability Programs employed by DDC are based on the requirements of MIL-STD-785, MIL-STD-781, and MIL-HDBK-217. DDC's complete product line - tried and proven components - can be presented in a Hi-Rel configuration and be integrated into a design for a Hi-Rel system. The Maintainability Programs employed by DDC are structured in accordance with the requirements of MIL-STD-470, MIL-STD-471, and MIL-HDBK-472. Both the maintainability and reliability functions are integrated with the design as well as manufacturing tasks to ensure a total system approach to product assurance.

DDC maintains a product assurance evaluation laboratory to: evaluate incoming materials, investigate manufacturing problems, support engineering studies, and perform detailed failure analysis. The laboratory is staffed with Quality Assurance professionals and contains the following state-of-the-art equipment:

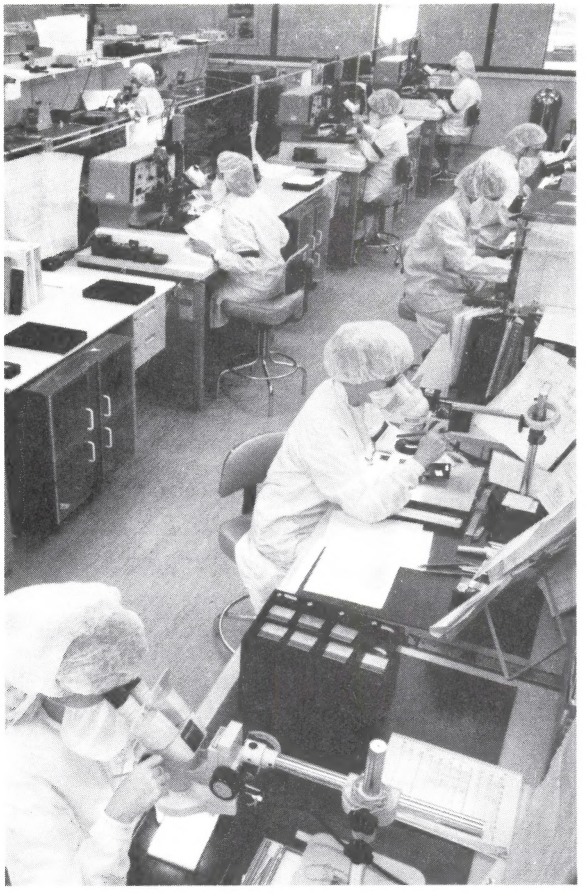
Scanning Electron Microscope (SEM). With SEM, DDC engineers can examine surface structure up to 200,000 times magnifications.

Energy Dispersive X-Ray Spectrometer (EDAX) With an EDAX attached to the SEM, the identification of chemical elements that may cause reliability problems in the hybrid is possible. The EDAX is especially valuable for incoming inspection and failure analysis studies.

MANUFACTURING

DDC's manufacturing capabilities are subdivided into the unique areas in which the company specializes. Approximately 35,000 square feet are dedicated to the manufacture of discrete components, harnesses, and assemblies; an additional 25,000 square feet are set aside for a clean, modern, environmentally controlled, thick-film hybrid area. Each, of these areas, is managed by an individual team of specialist, under the direction of a single Vice-President of Manufacturing. In addition 8,000 square feet are dedicated to the Material Control and Purchasing departments to assure an orderly flow of material onto the production lines. The Material Control Department also services Engineering's needs; Engineering maintains its own separate purchasing and expediting functions, minimizing the impact on the scheduled flow of manufactured products.

DDC is a leader in the field of military, high reliability, data conversion components, subsystems, and systems. DDC's Manufacturing expertise has been approved by most of America's leading aerospace companies as compliant to MIL-I-45208A and has also been certified by the U.S. Navy as a SEM (Standard Equipment Module) facility.

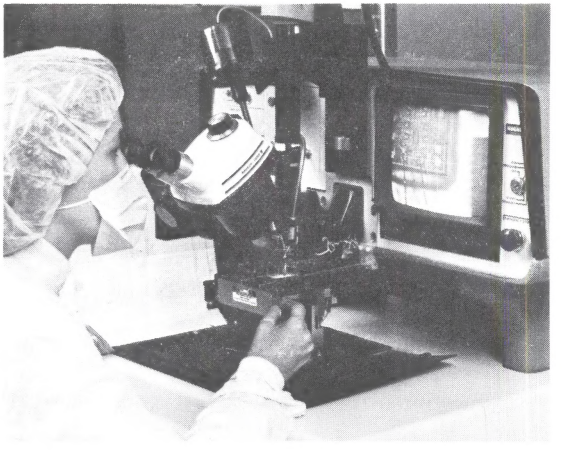


EQUIPMENT

DDC's capital equipment in its hybrid production facility includes: many ultrasonic and thermocompression wire bonders, epoxy and eutectic die-attach equipment. Machinery for these functions is the most modern type available and is updated regularly.

DDC used multizone belt furnaces for the deposition and firing of conductive and resistive substrate materials and manufactures its own substrate screens. Each hybrid operator and hybrid inspector is provided with the latest type stereoscopic and/or zoom microscopes to assure the proper placement and performance of the hybrid component parts. In addition, DDC's Quality Assurance Department possesses a unique lenseless microscope for inspection purposes, plus centrifuge, gross and fine leak testing, photographic examination, and PIND equipment.

DDC's Engineering Model Shop contains a representative sampling of each of the above-mentioned pieces of equipment. This insures that prototype quantities are fabricated on equipment identical to the ones used in the production process.



TESTING

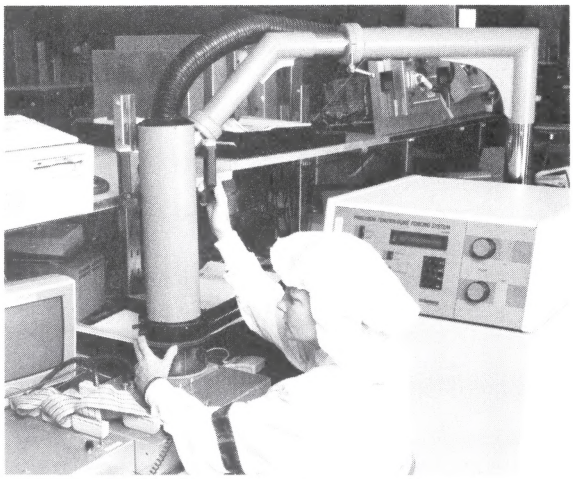
Testing facilities at DDC include state-of-the-art DVMs, oscilloscopes, signal generators, and other related test equipment. Automatic and semi-automatic computer test stations are used continuously to check individual components, subassemblies, and fully integrated systems. Since the Engineering Department's equipment reflects that used in Manufacturing, all Engineering evaluations and investigations are consistent with procedures used in the actual manufacturing process.

Temperature chambers are used for the burn-in and temperature testing of finished products. A fully-equipped component test facility under the direction of our Quality Assurance Department is used for characterizing, testing, and evaluation all incoming component parts to be used in DDC's products. Also, a Lorlan computer-aided transistor and diode test machine is used for incoming inspection and grading purposes. The Component Test Department tests all custom semiconductor wafers or chips either by probing or by mounting on test substrate and in test headers for full characterization and evaluation.

TEST METHODS FOR DISCRETE MODULES

Discrete modules meet the specific test methods and conditions of MIL-STD-202 (shown below) unless alternative methods are specified by the customer in procurement documentation.

MIL-STD-202 TEST METHODS		
METHOD	CONDITION	COMMENT
204	C	10G, 2kHz Vibration
213	A	50G, 11ms Shock
106*	–	Moisture
107	A	Thermal Shock
101	B	Salt Spray
105	B	50k ft. altitude
*When conformally coated on PC board.		

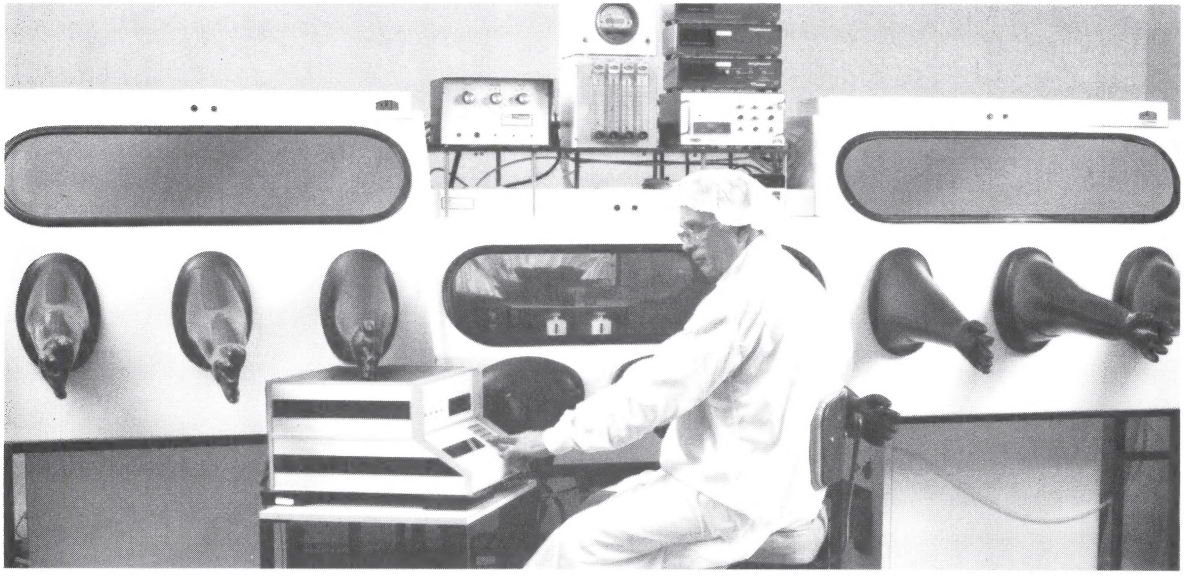


SALES AND MARKETING

DDC maintains a world-wide network of technical sales representatives and direct sales personnel to service its customers. Due to the high performance of DDC's product, most of this field organization consists of graduate engineers. An Applications Engineering staff offers professional applications assistance and detailed technical information.

DDC is frequently asked to modify its standard products to meet specific customer requirements for performance, quality, and configuration control. Our factory Applications Engineering staff is prepared to take individual customer request and translate them into documentation for engineering design, product manufacturing, and quality assurance.

Customer support, in the form of catalogs, product data sheets, application notes, and price lists is provided by DDC's Marketing staff in Bohemia.



SECTION A
ANALOG TO DIGITAL (A/D) CONVERTERS

PRODUCT SUMMARY TABLE

	MODEL	RESOLUTION	CONVERSION TIME	LINEARITY ERROR	PACKAGE	OPERATING TEMP. RANGE	POWER DISSIPATION	DESCRIPTION/ FEATURES	PAGE
	ADC-00110 **ADC-00111** **ADC-00113**	12 Bit	100 nsec	±0.025% FSR	46 Pin Plug-in Hybrid 1.6 x 2.4 x 0.2"	-55°C to +125°C	7W	10 MHz word rate, containing T/H, A/D converter, data registers, Tri-State output registers, and timing circuits.	A-5 A-5 A-11
	ADC-00115	12 Bit	200 nsec	±1/2 LSB	5.0 x 5.43 x 0.5" Card	0°C to +70°C	7.25 W	5 MHz word rate, containing T/H, A/D converter, data registers, Tri-State output registers, and timing circuits. Pin-for-pin low power MOD-1205 replacement.	A-18
*	**ADC-00145**	14 Bit	200 nsec	±1 LSB	40 Pin TDIP 1.1 x 2.1 x 0.25"	-55°C to +125°C	2.9 W	5 MHz word rate, containing T/H, A/D converter, data registers, Tri-State output registers, and timing circuits.	A-21
	ADC-00300 **ADC-00302**	12 Bit	500 nsec	±0.012% FSR	40 Pin TDIP 40 Pin Flatpack 1.2 x 2.2 x 0.25"	-55°C to +125°C	3W	2MHz word rate; includes T/H and all timing circuits. Very high speed.	A-27
	ADC-00305II	12 Bit	500 nsec	±0.012% FSR	40 Pin TDIP Hybrid	0°C to + 70°C	2.6W	2 MHz word rate; containing T/H, A/D converter, Tri-State output registers, and timing circuits. Low cost.	A-33
*	**ADC-00310**	12 Bit	200 nsec	±0.012% FSR	40 Pin TDIP Hybrid	0°C to + 70°C	2.6W	5 MHz word rate; containing T/H, A/D converter, Tri-State output registers, and timing circuits. Low cost.	A-39
	ADC-00403 **ADC-00404**	12 Bit	2µsec	±1/2 LSB	32 Pin TDIP 1.14 x 1.93 x 0.2"	-55°C to +125°C	2.4W	High-speed, pin-for-pin replacement for ADC87 and ADC85. Military applications. Hermetic seal.	A-45

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

* New Product

BACKGROUND INFORMATION

INTRODUCTION

In A/D converters, DDC has focused on high performance products based on the most recent advances in component technology and circuit design. Most converters are self-contained with internal clocking and reference, and require no external components except for optional offset and gain trimming. Pin programmable features include different input voltage ranges, unipolar or bipolar coding, and 3-state outputs.

THE SUCCESSIVE APPROXIMATION METHOD

An A/D converter using the successive approximation method contains an internal D/A converter. The digital input bits in the D/A converter are tried in succession until the D/A output is equal to the external analog input signal. The D/A digital input will then represent the digitized external signal.

All successive approximation converters are based on the closed loop technique shown in Figure 1. An internal successive approximation register (SAR) produces a digital output which activates the bits in the internal D/A converter. A clock and control logic circuit operates the register according to a comparator signal which detects the difference between the analog input and the output of the internal D/A. A conversion is initiated by an externally supplied pulse which starts the sequence. All bits except the MSB are initially turned off. The control logic then sets one bit at a time in the register, setting each bit high or low according to the comparator output. The most significant bit (bit 1, the MSB) is first set to logic 1, and the precision D/A produces a current equal to 1/2 full scale. This current I_{OUT} is compared to the current I_{IN} created by the input voltage V_{IN} at the summing junction. If the I_{OUT} is less than I_{IN}, the comparator tells the SAR to leave the first bit at logic 1 and, as the clock continues, bit 2 is set at logic 1. If I_{OUT} is greater than I_{IN}, the first bit is reset to logic 0 before trying bit 2.

Any succeeding bit that does not cause the combined bit currents to exceed the input current remains set at a logic 1, and any bit that causes the combined bit currents to exceed the input current is reset to a logic 0. After the LSB has been tried, the SAR transmits a Conversion Complete (CC) signal. The output of the SAR at this time is a digital number representing the analog input as a fraction of the internal reference voltage. The accuracy of the digital output will be proportional to the accuracy of the reference and internal D/A, and the highest accuracy attainable will be ±1/2 LSB.

THE TWO STEP METHOD

The speed of a successive approximation converter is limited by the need to wait for each bit to settle for each trial. At the cost of increased complexity, it is possible to use a two step technique, which can achieve more than twice the speed. In a two-step process, the bits are tried in two groups, called the coarse bits and the fine bits. Each group of bits is tried with its own A/D converter, and each A/D requires less resolution (fewer bits). A two step conversion process is faster than single stage conversion not only because a new conversion can be initiated while the fine bits are being tried, but also because the settling times for each bit are reduced when a A/D requires less accuracy.

Figure 2 shows how the two step technique can be implemented. The analog input is sampled by the track/hold amplifier and held for the first part of the conversion cycle. The coarse bits A/D converter digitizes the most significant bits at a relatively fast rate and the coarse bits are stored in the digital combiner. The analog voltage corresponding to the coarse bits which is formed by the D/A converter is subtracted from the analog input signal being held by the input track/hold amplifier. Correction circuits are usually required at the differencing junction to compensate for non-linearities in the A/D and D/A, track/hold errors, and temperature drifts. With a PROM these errors, which are highly repeatable, can be uniquely corrected for each converter.

As soon as the summed voltage from the differencing junction has been acquired by the fine bits track/hold amplifier, the input track/hold can acquire a fresh analog input voltage to commence a new conversion cycle. Meanwhile, the fine bits A/D digitizes the fine bits and the digital combiner accepts them to complete the first conversion cycle. The entire two-step conversion cycle is regulated by a clock with control logic, and a Start Conversion pulse initiates each conversion. An important advantage of two step conversion is that the ultimate accuracy of conversion is determined by the accuracy of the subtraction process, which involves the D/A and track and hold amplifier. These circuits need to settle only once during each conversion cycle. The internal coarse and fine bit A/D's may be successive approximation or flash converters.

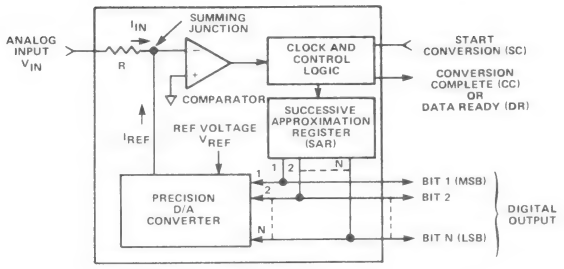


FIGURE 1. SUCCESSIVE APPROXIMATION A/D CONVERSION

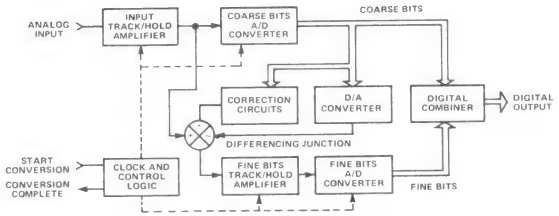


FIGURE 2. TWO-STEP A/D CONVERSION

THE FLASH QUANTIZATION METHOD

The flash quantization method which is illustrated in Figure 3 is the most rapid A/D conversion technique. A string of comparators is used to compare the analog input voltage directly with voltage steps on a resistance ladder. In Figure 3, for instance, if the analog input voltage lies between $3/8V_R$ and $4/8V_R$, the lower three comparators would respond and the upper four would not. The decoding logic translates the comparator responses into appropriately coded digital output.

Flash quantization is rapid because signals propagate very quickly through the parallel-connected comparators and the decoding logic. In constrast, the throughput delay in a successive approximation converter with n bits includes n D/A settling times and n comparator response times. On the other hand, the complexity of a flash quantization converter can be greater because the number of comparators required and the complexity of the decoding logic depends on the number of bits. A resolution of n bits will require 2^n resistors and 2^n-1 comparators. The three bit converter shown in Figure 3 requires $2^3=8$ resistors and $2^3-1=7$ comparators. A converter with 6 bit resolution requires $2^6 = 64$ resistors and $2^6 - 1 = 63$ comparators.

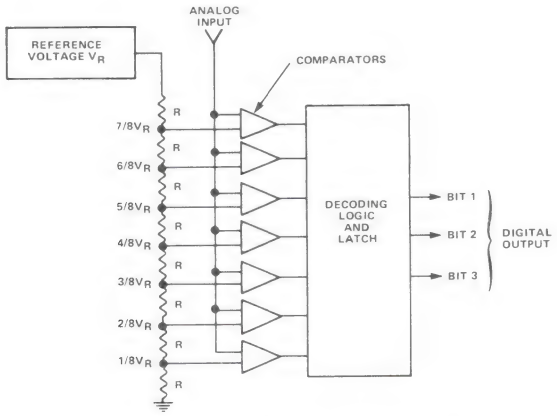


FIGURE 3. 3-BIT FLASH CONVERSION

A/D TRANSFER CHARACTERISTICS AND ACCURACY

The output of an A/D converter is inherently quantized and ideally any input analog value within ±1/2 LSB of the digital code to which it corresponds should give the same digital output. This results in the ideal transfer characteristic shown in Figure 4 for a 3 bit A/D converter with unipolar straight binary or bipolar offset binary coding. In Figure 4, for example, the 100 code output corresponds to all analog input values within ±1/2 LSB of the analog value in the center of the range.

It can be seen from Figure 4 that a transfer function described by transition values does not cover a full range of analog input values extending from 0 to F.S. or from −F.S. to +F.S. In Figure 4, for instance, the unipolar analog input extends from 0 to +F.S. − 1/2 LSB, and the code for +F.S. is not defined. For some converters, the analog scale is offset by 1 LSB in order to give +F.S. a code value. The code for the opposite end of the scale (0 to −F.S.) will then be undefined. This is most often done with complementary coding, in which logic 1 and logic 0 values are interchanged, so F.S. can correspond to a 000. . .code.

The accuracy of an A/D converter is measured by determining the analog input values corresponding to 50% dither between adjacent digital codes. Ideally, as shown in Figure 4, the transition points will occur midway between LSB values, at points such as 1/2 LSB, 3/2 LSB, 5/2 LSB, etc.. The transition table for a 3 bit converter in Figure 5 is equivalent to the transfer characteristic in Figure 4.

The total error in a converter is the sum of the offset error, the gain error and the linearity error. For a unipolar A/D, the offset error is usually specified for the transition corresponding to ±1/2 LSB, but can be assigned by the manufacturer to be at either end of the analog input range. For a bipolar A/D, the offset error could also be assigned to be at the transition close to the center of the range where the analog input is ±1/2 LSB. At whatever point offset is designated, the offset error will be the difference between the measured value for 50% dither and the theoretical analog value for that point.

The gain error is measured at the transition points at the opposite ends of the range. The gain is equal to the difference between the measured inputs at the two transition points (keeping negative signs for negative inputs), divided by the theoretical input

span between them. For the 3 bit converter described above, the input span is F.S. – 2 LSB for straight binary coding, and 2 F.S. – 2 LSB for offset binary coding.

Linearity measurements must be corrected for both offset and gain errors. The analog input is measured for 50% dither at each transition point. The linearity error at each point is the difference between the theoretical value and the measured value after the measured value has been corrected by first substracting the offset error and then multiplying by the gain correction. An alternative procedure, which simplifies calculations is to trim the offset error and then multiply by the gain correction.

Monotonicity is usually also an important requirement. If the converter is monotonic, the digital code will never decrease when the analog input is increased, and will never increase as the input is decreased. All DDC converters are monotonic.

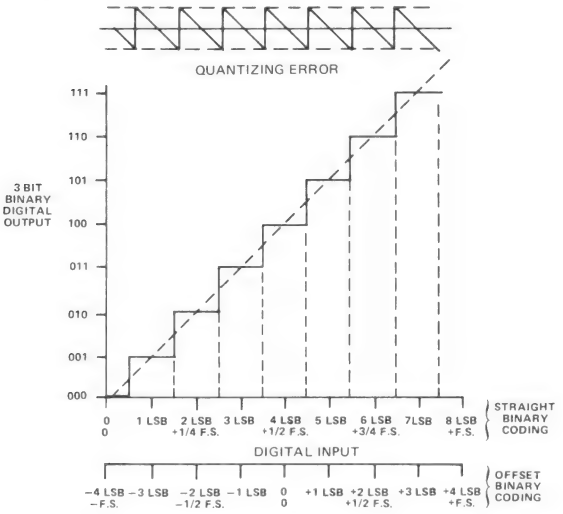


FIGURE 4. IDEAL TRANSFER CHARACTERISTIC FOR A 3-BIT A/D CONVERTER

ANALOG INPUT		BIT TRANSITION		
UNIPOLAR STRAIGHT BINARY	BIPOLAR OFFSET BINARY	(MSB) BIT 1	BIT 2	(LSB) BIT 3
+F.S. – 3/2 LSB	+F.S. – 3/2 LSB	1 1	1 1	0 1
+3/4 F.S. – 1/2 LSB	+1/2 F.S. – 1 LSB	1 1	0 1	1 0
+1/2 F.S. + 1/2 LSB	+1/2 LSB	1 1	0 0	0 1
+1/2 F.S. – 1/2 LSB	–1/2 LSB	0 1	1 0	1 0
+1/4 F.S. + 1/2 LSB	–1/2 F.S. + 1/2 LSB	0 0	1 1	0 1
+3/2 LSB	–F.S. + 3/2 LSB	0 0	0 1	1 0
+1/2 LSB	–F.S. + 1/2 LSB	0 0	0 0	0 1

FIGURE 5. THEORETICAL TRANSITION VALUES FOR 3 BIT A/D CONVERTER

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

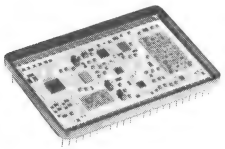
See page **N-19** for a list of Application Notes available from DDC.

DDC
ILC DATA DEVICE CORPORATION

ADC-00110 AND ADC-00111

12 BIT 10 MHz T/H + A/D HYBRID HIGH SPEED, SMALL SIZE, MIL-SPEC

A



DESCRIPTION

The ADC-00110 is a 12 bit, 10 MHz track/hold and A/D converter hybrid packaged in a 46 pin plug-in.

Containing T/H,A/D converter,data registers,tri-state output buffers,and timing circuits, the ADC-00110 is the fastest and smallest digitizer of its kind. The ADC-00110 operates over a temperature range of -55°C to +125°C and military processing is available.

The ADC-00110 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00110's technical breakthroughs in speed and size.

Foremost among them are proprietary ICs for the DAC, the conversion logic, and the gain amp functions. In addition, judicious use of thin film and thick film hybrid technology resulted in minimum layout area.

With its high speed, small package and wide operating temperature range, the ADC-00110 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and IR digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high-speed data acquisition and communications systems.

FEATURES

- *INCLUDES*
  - *– TRACK/HOLD*
  - *– A/D CONVERTER*
  - *– TRI-STATE OUTPUT REGISTERS*
  - *– TIMING CIRCUITS*
- *10 MHz WORD RATE*
- *SMALL 46 PIN PLUG-IN HERMETIC HYBRID*
- *INPUT VOLTAGE OPTIONS*
- *-55°C TO +125°C OPERATING TEMPERATURE*

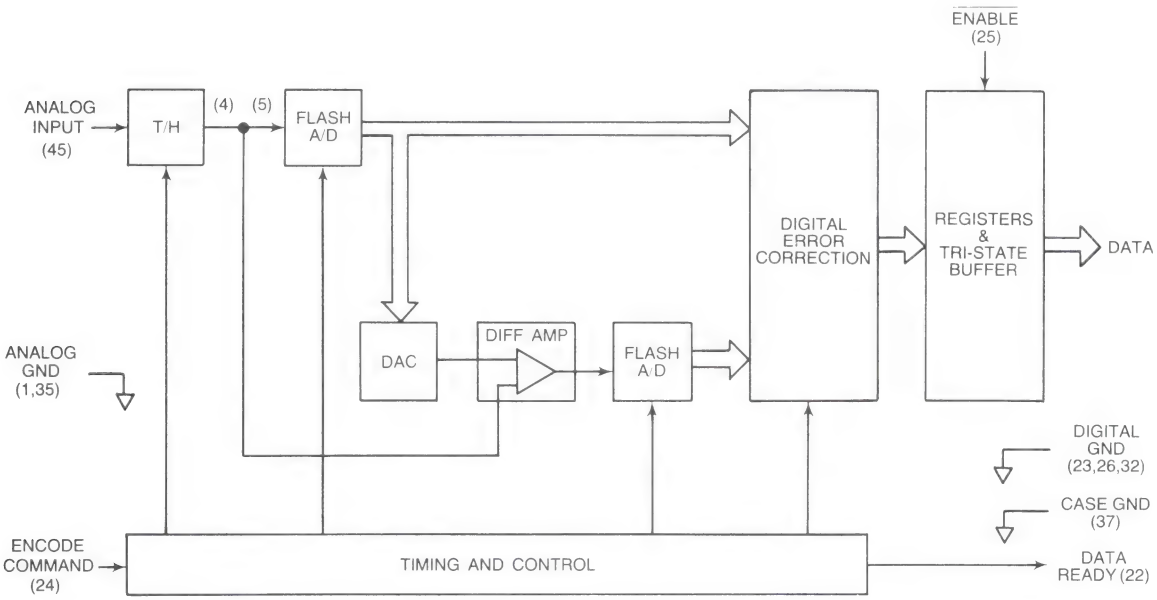


FIGURE 1. ADC-00110 BLOCK DIAGRAM

TABLE 1. ADC-00110 SPECIFICATIONS (T/H and A/D)

Typical values at +25°C case temperature, nominal power supply voltages, and 10 MHz encode rate, unless otherwise noted.

PARAMETER	UNITS	VALUES
Resolution	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.025 typ, ±0.050 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff Linearity Error	LSB	±1 max
Gain Error	%FSR	±0.5 max
Gain Error Tempco	ppm FSR/°C	50
Offset Error	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	50 max
No Missing Codes		Guaranteed
DYNAMIC CHARACTERISTICS		
Conversion Rate	MHz	DC to 10 min
Pipeline Delay [1]	nsec	2 Encode Commands +80 nsec
Aperture Uncertainty (Jitter)	psec RMS	9 typ, 20max
Aperture Time (Delay)	nsec	6(±3)
Signal to Noise Ratio (SNR) [2]		
5MHz analog input	db	68.5 typ, 64min
1MHz analog input	db	69.5 typ, 65min
100kHz analog input	db	70.5 typ, 66min
Transient Response [3]	nsec	100 max
Overvoltage Recovery [4]	nsec	200 max
Input Bandwidth		
Small Signal, 3dB [5]	MHz	70typ, 50min
Large Signal, 3dB [6]	MHz	40typ, 30min
Total Harmonic Distortion		
5MHz analog input	db below FS	64min
100kHz analog input	db below FS	66min
Two-tone linearity(at input freq.)		
60KHz; 62KHz	db below FS	62 min
2.498MHz; 2.500MHz	db below FS	62 min
4.996M Hz; 4.998MHz	db below FS	60 min
ANALOG INPUT	ADC-	00110 00111
Voltage Range		
(Normal Operation)	V	±2.5 ±1
(Absolute Max)	V	±5 max ±2max
Impedance		
Resistance	Ohms	1M min 50k min
Capacitance	pF	10 10
ENCODE COMMAND INPUT [7] (ADC-00110)		
Logic Levels, TTL Compatible	V	Logic 0 = 0.4 Logic 1 = 2.4
Minimum Pulse Width	nsec	10
Maximum Pulse Width	nsec	Encode Command Period -20 nsec
DIGITAL OUTPUT		
Format	Bits	12 parallel; NRZ
Logic Levels, TTL Compatible	V	Logic 0 = 0.4 Logic 1 = 2.4
Time Skew	nsec	5 max
Coding		Offset binary two's complement
Drive	TTL Loads	3
POWER SUPPLIES (ADC-00110)		
+15 Volt Supply	V	+15 ±5%
Current Drain	mA	80 typ, 120 max
-15 Volt Supply	V	-15 ±5%
Current Drain	mA	80 typ, 125 max
+5 Volt Supply	V	+5 ±5%
Current Drain	mA	300 typ, 400 max
- 5.2 Volt Supply	V	- 5.2 ±5%
Current Drain	mA	600 typ, 700 max
Power Dissipation	W	7.0 typ, 9.25 max
PSRR:		
±15V Supplies	%FSR/%V_S	0.01
+ 5V and -5.2V Supplies	%FSR/%V_S	0.03

TABLE 1. ADC-00110 SPECIFICATIONS (T/H and A/D) (continued)

PARAMETER	UNITS	VALUES
POWER SUPPLIES (ADC-00111)		
+15 Volt Supply	V	+15 ±5%
Current Drain	mA	40 typ, 70 max
-15 Volt Supply	V	-15 ±5%
Current Drain	mA	40 typ, 75 max
+5 Volt Supply	V	+5 ±5%
Current Drain	mA	315 typ, 420 max
- 5.2 Volt Supply	V	- 5.2 ±5%
Current Drain	mA	615 typ, 720 max
Power Dissipation	W	5.9 typ, 8.0 max
PSRR:		
±15V Supplies	%FSR/%V_S	0.01
+ 5V and -5.2V Supplies	%FSR/%V_S	0.03
TEMPERATURE RANGE		
Operating (Case)		
-1 Option	°C	-55 to +125
-3 Option	°C	0 to +70
Storage	°C	-55 to +165

Notes:

(1) Measured from the rising edge of Encode Command to the falling edge of Data Ready; use rising edge to strobe output data into external circuits. See figure 2, timing diagram.
(2) Rms signal to rms noise ratio.
(3) For full-scale step input, 12-bit accuracy attained in specified time.
(4) Recovers to 12-bit accuracy in specified time after 2 x FS input overvoltage.
(5) With analog input 40 dB below FS.
(6) With FS analog input (Large-signal bandwidth flat within 0.2 dB,DC to 5MHz).
(7) Transition from digital 0 to digital 1 initiates encoding.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00110 sampling A/D converter. Its major elements are a track/hold amplifier, 6-bit and 8-bit flash A/D converters, a 6-bit D/A converter, and a differential amplifier. The remaining functions are timing and control circuits, digital buffers, and registers.

These components implement a straightforward 2-step A/D conversion algorithm. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. The flash A/D then generates a coarse encode of the sampled voltage. Its 6-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 6-bit word is input to the DAC, which converts it to an analog voltage.

The differential amplifier subtracts the voltage representing the coarse encode from the sampled input, and scales it up to the correct full scale range.

Next, the 8-bit flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 8-bit word is stored in the LSB register. Finally, the contents of the 6-bit MSB and 8-bit LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffer.

Since the ADC-00110 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

Care must be taken when designing with the ADC-00110, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power supply and ground currents. For this reason, it is recommended that decoupling

capacitors be used on each power supply line. See the paragraph on Power Supply Decoupling for more detail. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00110. Conductor lengths should be kept to a minimum, and a large area ground plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A Typical ADC-00110 timing diagram is shown in figure 2. Note that the Encode Command repeats at 100 nsec intervals with a throughput (pipeline) delay of 280 nsec.

A conversion cycle is initiated by the application of a positive pulse (15 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. First the internal track/hold is placed in the HOLD mode. The output signal is then delivered to the 6-bit flash A/D converter for a coarse conversion of thee 6 MSBs. The output of the 6-bit flash A/D is also delivered to the D/A whose output is applied to the differential amplifier. The output of the differential amplifier is then delivered to the 8-bit flash A/D converter. Once the 8-bit flash conversion is complete, the internal T/H is returned to the TRACK mode. The output of the 8-bit flash A/D converter along with the original coarse 6-bit word is input to the digital error correction circuit with output to the 12-bit register. The Encode Command input then updates the register to take data.

The idea behind pipelining is that a second Encode is started before the first Encode has completed conversion. Consequently, the input signal is encoded and output data is delivered at a 10MHz rate. The pipeline delay is two Encode periods plus 80 nsec, or 280 nsec, minimum. Since Data Ready stays low for 50 nsec, it is possible to use the Encode Command to enable and continuously take data at a 10M Hz rate, though output data lags analog input by two encode periods plus 80 nsec. Note that data is not valid during the first 5 nsec following the falling edge of Data Ready, but is otherwise valid. The timing diagram also indicates the tri-state propagation delays for both enabling and disabling the latch as 8 nsec typ, and 10 nsec max.

LAYOUT PRECAUTIONS

The ADC-00110 high-speed sampling A/D converter generates high-frequency power supply and ground currents, and is sensitive to coupled signals. High-frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package, with connection to the case ground pin. While the case ground pin may be left floating it is recommended that the case be tied to system ground in order to minimize ground contributions to noise.

POWER SUPPLY DECOUPLING

Decoupling capacitors are required on each power supply to minimize noise. Figure 5 illustrates the recommended decoupling scheme. Each decoupled line must have a 10 µF or larger tantalum capacitor in parallel with a 0.01 µF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package. While the user may use the same power supply for the 5.2V analog and digital supplies, it is recommended that the supply lines to the ADC-00110 be separated at the supply and treated as individual supplies at the board in order to minimize crosstalk. The same applies to the 5V analog and digital supplies. It is further recommended that an inductor, such as the Ferrox Cube Bead model #VK20020/4B be used in the digital supply line to prevent digital switching from being transposed on the analog supply. For instances where the user has a seperate analog and digital supplies: the +5V current drain is approximately 20% digital; and the -5.2V current drain is approximately 50% digital.

OUTPUT CODING

Output coding is illustrated in table 2. The ADC-00110 is TTL compatible and outputs offset binary and two's complement data. Moreover, data is accessed through a tri-state latch. A LOW state input to pin 25, $\overline{\text{Enable}}$, enables output data; input HIGH disables as illustrated in the figure 2.

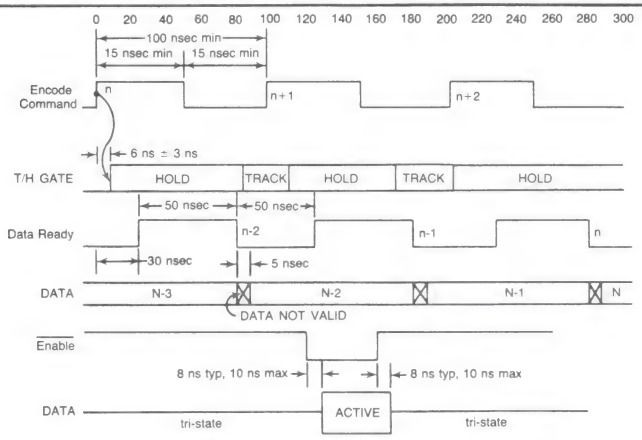


FIGURE 2. ADC-00110 TIMING DIAGRAM

TABLE 2. OUTPUT CODING

INPUT VOLTAGE	BIPOLAR	
	Offset Binary	Two's Complement
−FS	0000 0000 0000	1000 0000 0000
−¾FS	0001 1111 1111	1001 1111 1111
−½FS	0011 1111 1111	1011 1111 1111
−1 LSB	0111 1111 1110	1111 1111 1110
0	0111 1111 1111	1111 1111 1111
+1 LSB	1000 0000 0000	0000 0000 0000
+½FS	1011 1111 1111	0011 1111 1111
+¾FS	1101 1111 1111	0101 1111 1111
+FS−1LSB	1111 1111 1110	0111 1111 1110
+FS	1111 1111 1111	0111 1111 1111
	B1 thru B12	$\overline{\text{B1}}$, B2 thru B12

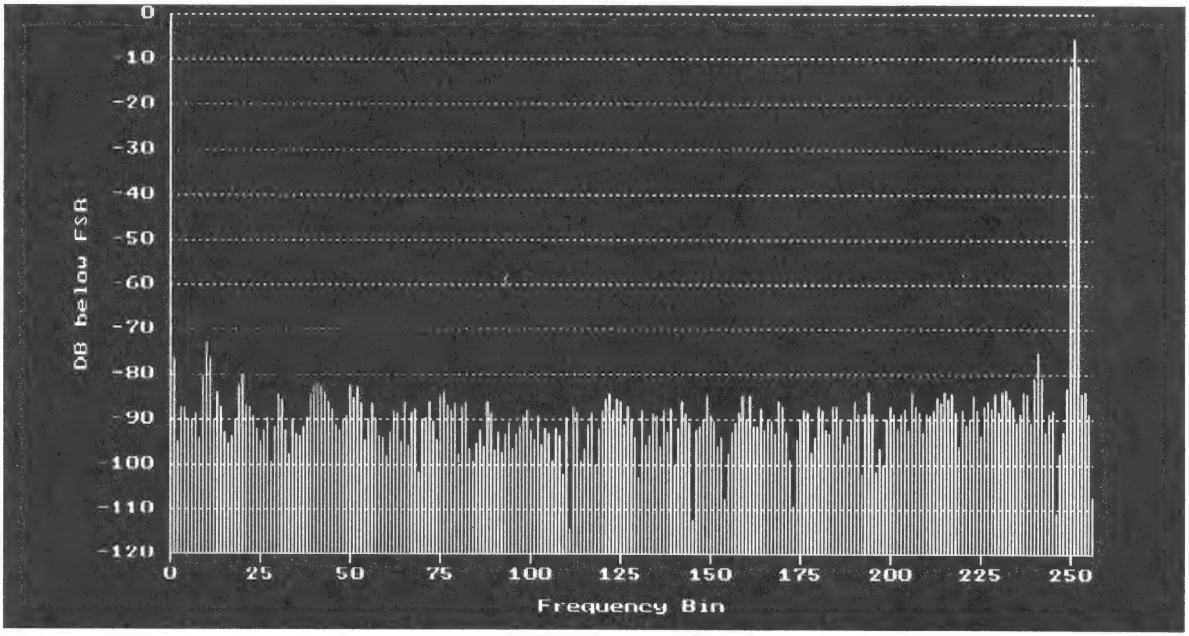
FFT TEST DESCRIPTION

In order to determine the harmonic distortion and signal to noise ratio of the ADC-00110 and ADC-00111, DDC uses some specialized hardware and an FFT analysis program. The details of the method are described below and illustrated in figure 3.

The FFT used is 512 points. The extra points that are taken can be used for either increasing the spectral resolution or for averaging a number of records to minimize the run-to run variation in readings. A single 512 point record typically gives run-to-run variations of as much as 1 db in signal to noise ratio. An 8 record average can decrease this to about 0.2 db. The 512 data samples are windowed using Hanning weighting. An FFT is then performed on the weighted bins. The frequency bins are then scanned for the bin with the largest amplitude. This is defined as the fundamental frequency. The amplitude of the fundamental is determined by computing the RMS sum of the bin below the fundamental, the fundamental and the bin above the fundamental.

This 3-cell summation yields an amplitude accurate to less than 0.01 db. The amplitude for each harmonic is calculated by summing the 3 bins around 2X the fundamental for the second harmonic, 3X the fundamental for the third and so on. This yields the harmonic distortion.

The signal to noise ratio is calculated by taking the RMS sum of the frequency bins up to 255 (the Nyquist rate) with the exception of the D.C term (bins 1, 2, and 3), the fundamental frequency (10 bins below the fundamental to 10 bins above the fundamental) and ±2 bins around each harmonic. The number of bins eliminated in each case is due to the leakage of the windowing function causing spillover into the area around the frequency terms. The summed frequency bins are then compared to the normalized fundamental for calculation of the broadband signal-to-noise ratio.



HARMONIC	BIN #	AMPLITUDE (db)
1	251	- 1.04
2	10	-70.74
3	241	-80.69
4	20	-77.65
5	231	-80.07

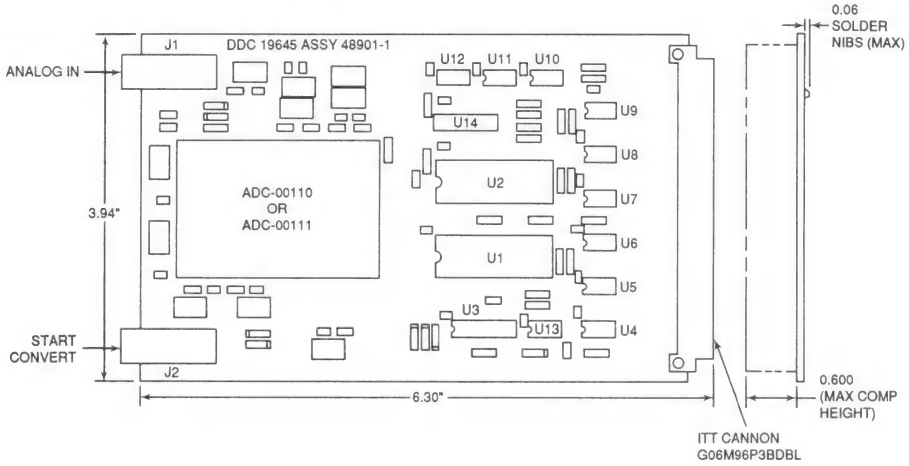
SIGNAL-TO-NOISE RATIO = 65.10 db
TOTAL HARMONIC DISTORTION = -68.17 db
SIGNAL-TO-(NOISE + DISTORTION) = 63.68 db
FFT size is 512 points.
Input Data Weighted by Hanning Window.

FIGURE 3. DYNAMIC TEST DATA

A

ADC-00110-615 EVALUATION CARD

The ADC-00110-615 Evaluation Card enables analysis of the ADC-00110 performance via digital interface. Figure 4 illustrates the ADC-00110-615 and Table 3 enumerates the input/output pin locations and functions. With on-board FIFO the card allows the user to capture up to 1024 WORDS for subsequent digital signal processing. DDC uses this fixturization for capturing data and performance of histogram and FFT in order to characterize the dynamic performance of the ADC-00110 and ADC-00111.

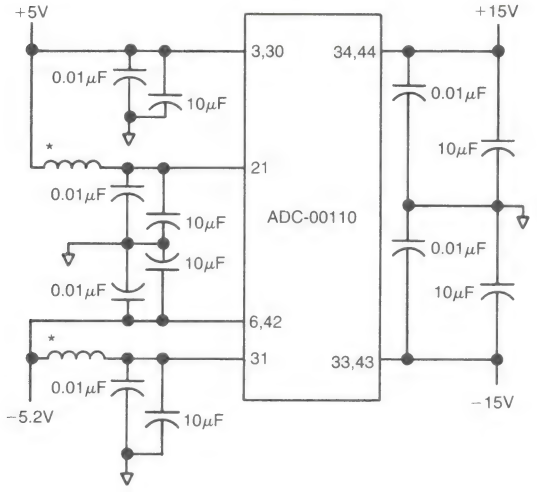


ACTIVE PARTS LIST		
COMPONENT	P/N	DESCRIPTION
U1, U2	IDT7202	FIFO
U3	75LS00N	GATE
U4 - U13	HPCL2231	OPTO-COUPLERS
U14	74HCT74	FLIP - FLOP

FIGURE 4. ADC-00110-615 MECHANICAL OUTLINE

TABLE 3. ADC-00110 VME PIN ASSIGNMENTS

ROW A				ROW C			
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	GND	A17	GND	C1	GND	C17	GND
A2	(ACQUIRE/$\overline{\text{RESET}}$)	A18	$\overline{\text{RE-TRANSMIT}}$	C2	N/C	C18	BIT2
A3	$\overline{\text{HALF-FULL FLAG}}$	A19	+5V COMP	C3	$\overline{\text{EMPTY FLAG}}$	C19	BIT1 (MSB)
A4	N/C	A20	COMP RTN	C4	BIT12	C20	$\overline{\text{BIT1 (MSB)}}$
A5	GND	A21	GND	C5	GND	C21	GND
A6	GND	A22	GND	C6	BIT11	C22	OUT REG
A7	GND	A23	GND	C7	BIT10	C23	$\overline{\text{FULL FLAG}}$
A8	$\overline{\text{READ}}$	A24	+15V	C8	BIT9	C24	+15V
A9	GND	A25	GND	C9	GND	C25	GND
A10	N/C	A26	-15V	C10	BIT8	C26	-15V
A11	GND	A27	$\overline{\text{WR INH}}$	C11	BIT7	C27	DATA READY
A12	GND	A28	+5V	C12	BIT6	C28	+5V
A13	GND	A29	GND	C13	GND	C29	GND
A14	N/C	A30	-5.2V	C14	BIT5	C30	-5.2V
A15	GND	A31	-5.2V	C15	BIT4	C31	-5.2V
A16	GND	A32	N/C	C16	BIT3	C32	N/C



*Ferrite bead. (See text on **POWER SUPPLY DECOUPLING**).

FIGURE 5. POWER SUPPLY DECOUPLING

TABLE 4. ADC-00110 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Analog Ground	46	Analog Return
2	NC	45	T/H Analog Input
3	+5V Analog Supply	44	+15V Supply
4	T/H Analog Output	43	−15V Supply
5	A/D Analog Input	42	−5.2V Analog Supply
6	−5.2V Analog Supply	41	NC
7	Overrange	40	NC (Factory Test Point)
8	$\overline{\text{MSB}}$	39	NC
9	Bit 1 (MSB)	38	NC
10	Bit 2	37	Case Ground
11	Bit 3	36	NC (Factory Test Point)
12	Bit 4	35	Analog Ground
13	Bit 5	34	+15V Supply
14	Bit 6	33	−15V Supply
15	Bit 7	32	Digital Ground
16	Bit 8	31	−5.2V Digital Supply
17	Bit 9	30	+5V Analog Supply
18	Bit 10	29	NC (Factory Test Point)
19	Bit 11	28	NC (Factory Test Point)
20	Bit 12 (LSB)	27	NC (Factory Test Point)
21	+5V Digital Supply	26	Digital Ground
22	Data Ready	25	$\overline{\text{Output Enable}}$
23	Digital Ground	24	Encode Command

Notes:
1. Pins 4 and 5 are to be externally connected.
2. NC means do not connect any signal to these pins as damage may occur to the hybrid.

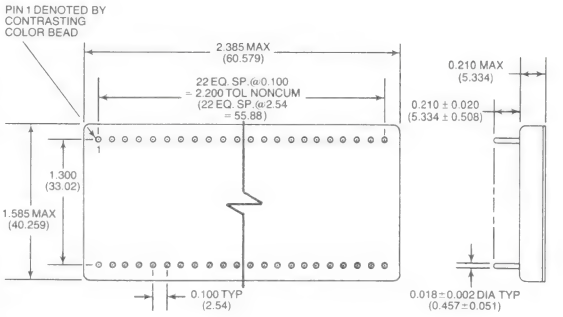
ORDERING INFORMATION

ADC- 00110 - 1 0 2

- Reliability:
  - 0 = Standard DDC procedures
  - 1 = Military processing available (Consult Factory)
  - 2 = Military processing available but without QCI testing.(Consult Factory)
- Operating Temperature Range:
  - 1 = -55 to +125°C
  - 3 = 0 to +70°C
- Input Voltage Range:
  - 0 = ±2.5V Input
  - 1 = ±1.0V Input

Consult factory for ECL Logic Compatibility.

ADC-00110-615 EVALUATION CARD



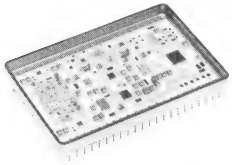
Notes:
1. Dimensions are in inches (mm).
2. Pin clusters to be centralized within ± 0.010 of outline dimensions

FIGURE 6. ADC-00110 AND ADC-00112 MECHANICAL OUTLINE

G

ADC-00113

12 BIT 10 MHz T/H + A/D HYBRID
HIGH SPEED, SMALL SIZE, MIL-SPEC



DESCRIPTION

The ADC-00113 is a 12 bit, 10 MHz track/hold and A/D converter hybrid packaged in a 46 pin plug-in. Pin-for-pin compatible with the ADC603.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00113 is the fastest and smallest digitizer of its kind. The ADC-00113 operates over a temperature range of -55°C to +125°C and military processing is available.

The ADC-00113 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00113's technical breakthroughs in speed and size. Foremost among them are proprietary ICs for the DAC, the conversion logic, and the gain amp functions. In addition, judicious use of thin-film and thick-film hybrid technology resulted in minimum layout area.

With its high speed, small package and wide operating temperature range, the ADC-00113 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and IR digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high-speed data acquisition and communications systems.

FEATURES

- ***Improved Pin-For-Pin ADC603***
- ***Includes***
  - ***Track/Hold***
  - ***A/D Converter***
  - ***Tri-State Output Registers***
  - ***Timing Circuits***
- ***10 MHz Word Rate***
- ***Small 46 Pin Plug-In Hermetic Hybrid***
- ***Input Voltage Options***
- ***-55°C TO +125°C Operating Temperature***

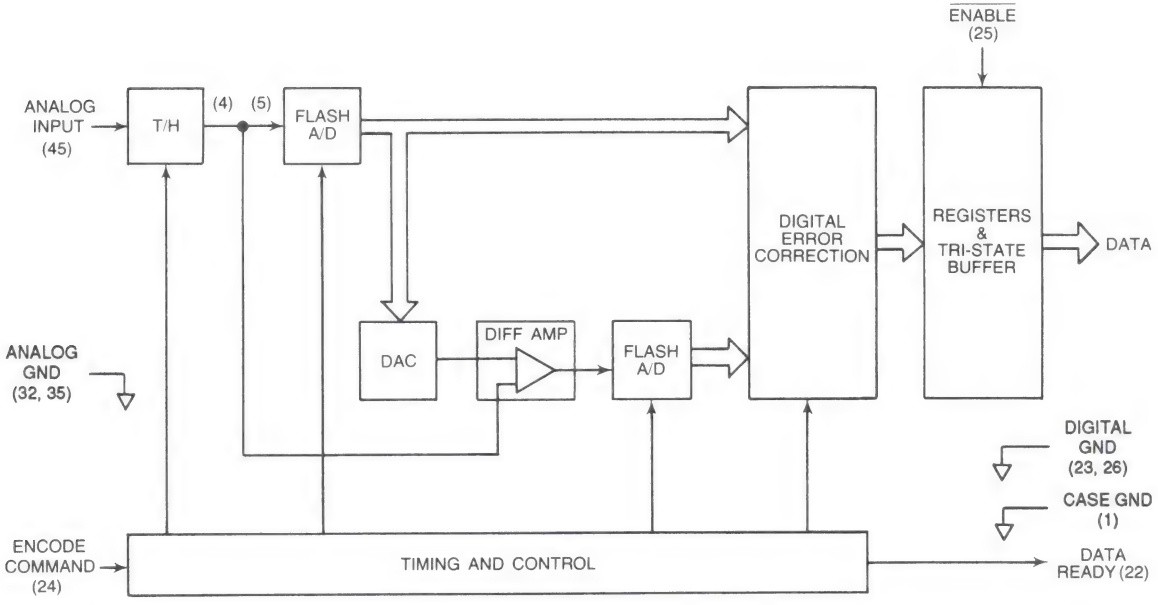


FIGURE 1. ADC-00113 BLOCK DIAGRAM

TABLE 1. ADC-00113 SPECIFICATIONS (T/H and A/D)

Typical values at listed temperature range, nominal power supply voltages, 10 MHz encode rate, and 15 minute warmup, unless otherwise noted.

PARAMETER	UNITS	VALUES FOR: ADC-00113-1XX at 25°C			ADC-00113-1XX at −55 to +125°C			ADC-00113-3XX at 25°C			ADC-00113-3XX at 0 to +70°C			CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE	°C		25		−55		+125		25		0	25	+70	T_{case}
RESOLUTION	Bits		12			12			12			12		
ACCURACY														
Linearity Error	LSB		0.75			0.75			0.75			0.75		F = 200Hz
Diff Linearity Error														
■ 68.3% of all codes	LSB		0.3			0.4			0.3			0.4		F = 200Hz
■ 99.7% of all codes	LSB		0.4			0.5			0.4			0.5		F = 200Hz
■ 100% of all codes	LSB		0.5			0.75			0.5			0.75		F = 200Hz
Gain Error	%FSR[1]		±0.2	±2		±0.4	±2		±0.2	1.0		±0.4	1.5	F = 200Hz
Offset Error	%FSR		±0.2	±2		±0.4	±2		±0.2	0.75		±0.4	1.0	dc
No Missing Codes		Guaranteed												
DYNAMIC CHARACTERISTICS														
Conversion Rate	MHz	dc		10	dc		10	dc		10	dc		10	Fixed
Pipeline Delay[2]		3 Encode Commands												Fixed
Aperture Uncertainty (Jitter)	psec rms		9			10			9			10		
Aperture Time (Delay)	nsec		−5			−6			−5			−6		
Signal-to-Noise Ratio[3] (SNR)														
■ 5MHz analog input	dB	64	67		64	67		64	67		64	67		F_S = 9.99MHz
■ 1MHz analog input	dB	65	67.5		65	67.5		65	67.5		65	67.5		F_S = 9.99MHz
■ 100kHz analog input	dB	66	68		66	68		66	68		66	68		F_S = 9.99MHz
Transient Response[4]	nsec		100			100			100			100		See note 4.
Overvoltage Recovery[5]	nsec		80			80			80			80		2x full-scale input
Input Bandwidth														
■ Small Signal, 3dB[6]	MHz		70			70			70			70		
■ Large Signal, 3dB[7]	MHz		40			40			40			40		
Total Harmonic Distortion														
■ 5MHz analog input	dB		−68	−64		−67	−60		−68	−64		−67	−64	F_S = 9.99MHz
■ 100kHz analog input	dB		−70	−66		−69	−64		−70	−66		−69	−66	F_S = 9.99MHz
Two-tone linearity														
■ 2.20MHz	dB		−75	−67		−72	−68		−75	−67		−72	−68	F_S = 8.006MHz
■ 2.50MHz	dB		−75	−67		−72	−68		−75	−67		−72	−68	F_S = 8.006MHz
ANALOG INPUT														
Voltage Range	V	−1.25		+1.25	−1.25		+1.25	−1.25		+1.25	−1.25		+1.25	Full scale
Impedance														
■ Resistance	MΩ		0.15			0.15			0.15			0.15		
■ Capacitance	pF		5			5			5			5		
ENCODE COMMAND INPUT[8]														
Logic Levels	V	TTL Compatible												t = Encode Command Period
Pulse Width	nsec	10		t-20	10		t-20	10		t-20	10		t-20	
DIGITAL OUTPUT														
Format	Bits	12 parallel; NRZ												
Logic Levels	V	TTL Compatible												
Time Skew	nsec	5	35		5	35		5	35		5	35		
Coding		Two's complement and inverted two's complement												
Drive	TTL Loads		3			3			3			3		

A

TABLE 1. ADC-00113 SPECIFICATIONS (T/H and A/D) (continued)

Typical values at listed temperature range, nominal power supply voltages, 10 MHz encode rate, and 15 minute warmup, unless otherwise noted.

PARAMETER	UNITS	VALUES FOR: ADC-00113-1XX at 25°C			ADC-00113-1XX at −55 to +125°C			ADC-00113-3XX at 25°C			ADC-00113-3XX at 0 to +70°C			CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES														
+15 Volt Supply	V	+14.25	+15	+15.75	+14.25	+15	+15.75	+14.25	+15	+15.75	+14.25	+15	+15.75	
■ Current Drain	mA		+ 40			+40			+40			+ 40		
−15 Volt Supply	V	−14.25	−15	−15.75	−14.25	−15	−15.75	−14.25	−15	−15.75	−14.25	−15	−15.75	
■ Current Drain	mA		−40			−40			−40			− 40		
+5 Volt Supply	V	+ 4.75	+5	+5.25	+4.75	+5	+5.25	+4.75	+5	+5.25	+ 4.75	+5	+5.25	
■ Current Drain	mA		+320			+320			+320			+320		
− 5.2 Volt Supply	V	− 4.95	− 5.2	− 5.46	− 4.95	− 5.2	− 5.46	− 4.95	− 5.2	− 5.46	− 4.95	− 5.2	− 5.46	
■ Current Drain	mA		−620			−620			−620			−620		
Power Dissipation	W		6.1			6.1			6.1			6.1		
PSRR:														
±15V Supplies	%FSR/%V_S		0.01			0.01			0.01			0.01		
+ 5V and -5.2V Supplies	%FSR/%V_S		0.03			0.03			0.03			0.03		

Notes:

(1) FSR: Full-Scale Range = 2.5V_{p-p}; F = input frequency; F_S = sampling Frequency.
(2) Measured from the rising edge of Encode Command to the falling edge of Data Ready; use rising edge to strobe output data into external circuits. See figure 2, timing diagram.
(3) Rms signal to rms noise ratio.
(4) For full-scale step input, 12-bit accuracy attained in specified time.
(5) Recovers to 12-bit accuracy in specified time after 2 x FS input overvoltage.
(6) With analog input 40 dB below FS.
(7) With F_S analog input (Large-signal bandwidth flat within 0.2dB,dc to 5MHz).
(8) Transition from digital 0 to digital 1 initiates encoding.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00113 sampling A/D converter. Its major elements are a track/hold amplifier, 6-bit and 8-bit flash A/D converters, a 6-bit D/A converter, and a differential amplifier. The remaining functions are timing and control circuits, digital buffers, and registers.

These components implement a straightforward 2-step A/D conversion algorithm. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. The flash A/D then generates a coarse encode of the sampled voltage. Its 6-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 6-bit word is input to the DAC, which converts it to an analog voltage.

The differential amplifier subtracts the voltage representing the coarse encode from the sampled input, and scales it up to the correct full scale range.

Next, the 8-bit flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 8-bit word is stored in the LSB register. Finally, the contents of the 6-bit MSB and 8-bit LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffer.

Since the ADC-00113 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

Care must be taken when designing with the ADC-00113, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line. See the paragraph on Power Supply Decoupling for more detail. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00113. Conductor lengths should be kept to a minimum, and a large area ground plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A Typical ADC-00113 timing diagram is shown in figure 2. Note that the Encode Command repeats at 100 nsec intervals with a throughput (pipeline) delay of 280 nsec.

A conversion cycle is initiated by the application of a positive pulse (15 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. First the internal track/hold is placed in the HOLD mode. The output signal is then

delivered to the 6-bit flash A/D converter for a coarse conversion of the 6 MSBs The output of the 6-bit flash A/D is also delivered to the D/A whose output is applied to the differential amplifier. The output of the differential amplifier is then delivered to the 8-bit flash A/D converter. Once the 8-bit flash conversion is complete, the internal T/H is returned to the TRACK mode. The output of the 8-bit flash A/D converter along with the original coarse 6-bit word is input to the digital error correction circuit with output to the 12-bit register. The Encode Command input then updates the register to take data.

The idea behind pipelining is that a second Encode is started before the first Encode has completed conversion. Consequently, the input signal is encoded and output data is delivered at a 10MHz rate. The pipeline delay is two Encode periods plus 80 nsec, or 280 nsec, minimum. Since Data Ready stays low for 50 nsec, it is possible to use the Encode Command to enable and continuously take data at a 10M Hz rate, though output data lags analog input by two encode periods plus 80 nsec. Note that data is not valid during the first 5 nsec following the falling edge of Data Ready, but is otherwise valid. The timing diagram also indicates the tri-state propagation delays for both enabling and disabling the latch as 8 nsec typ, and 10 nsec max.

LAYOUT PRECAUTIONS

The ADC-00113 high-speed sampling A/D converter generates high-frequency power supply and ground currents, and is sensitive to coupled signals. High-frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package, with connection to the case ground pin. While the case ground pin may be left floating it is recommended that the case be tied to system ground in order to minimize ground contributions to noise.

OUTPUT CODING

Output coding is illustrated in table 2. The ADC-00113 is TTL compatible and outputs two's complement data and inverted two's complement. Two's complement coding occurs when a LOW state TTL input is applied to pin 27, Output Logic Invert; application of a HIGH state TTL input results in inverted two's complement output data. Moreover, data is accessed through a tri-state latch. A LOW state input to pin 25, $\overline{\text{Enable}}$, enables output data; input HIGH disables as illustrated in the figure 2.

TABLE 2. OUTPUT CODING

INPUT VOLTAGE	BIPOLAR	
	TWO'S COMPLEMENT (pin 27 = low)	INVERTED TWO'S COMPLEMENT (pin 27 = high)
+FS (+1.25V)	0111 1111 1111	1000 0000 0000
+FS –1 LSB	0111 1111 1110	1000 0000 0001
3/4 FS	0001 1111 1111	1110 0000 0000
+1/2 FS	0011 1111 1111	1100 0000 0000
+1 LSB	0000 0000 0000	1111 1111 1111
0	1111 1111 1111	0000 0000 0000
–1 LSB	1111 1111 1110	0000 0000 0001
–1/2 FS	1011 1111 1111	0100 0000 0000
–3/4 FS	1001 1111 1111	0110 0000 0000
–FS + 1 LSB	1000 0000 0000	0111 1111 1111
	B1(MSB) thru B12(LSB)	B1(MSB) thru B12(LSB)

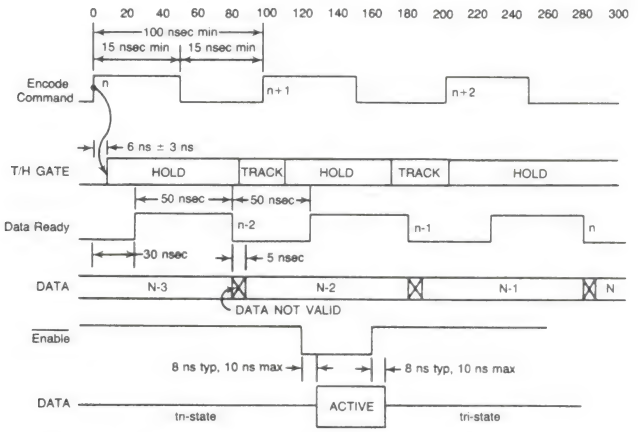


FIGURE 2. ADC-00113 TIMING DIAGRAM

A

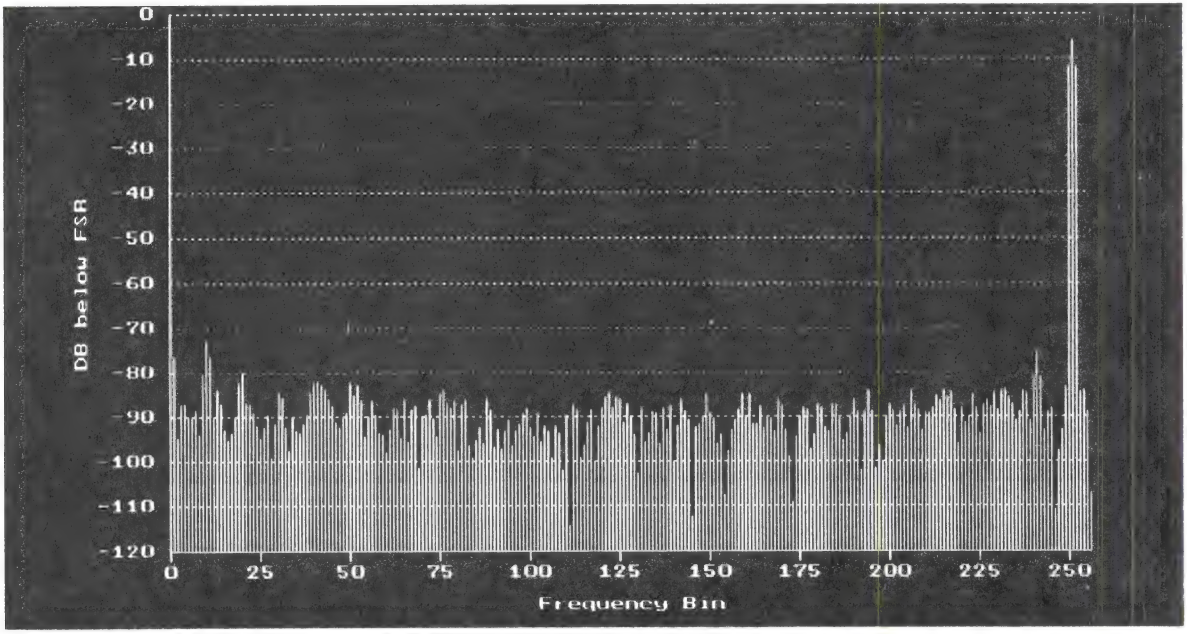
FFT TEST DESCRIPTION

In order to determine the harmonic distortion and signal to noise ratio of the ADC-00113, DDC uses some specialized hardware and an FFT analysis program. The details of the method are described below and illustrated in figure 3.

The FFT used is 512 points. The extra points that are taken can be used for either increasing the spectral resolution or for averaging a number of records to minimize the run-to run variation in readings. A single 512 point record typically gives run-to-run variations of as much as 1 dB in signal to noise ratio. An 8 record average can decrease this to about 0.2 dB. The 512 data samples are windowed using Hanning weighting. An FFT is then performed on the weighted bins. The frequency bins are then scanned for the bin with the largest amplitude. This is defined as the fundamental frequency. The amplitude of the fundamental is determined by computing the rms sum of the bin below the fundamental, the fundamental and the bin above the fundamental.

This 3-cell summation yields an amplitude accurate to less than 0.01 dB. The amplitude for each harmonic is calculated by summing the 3 bins around 2X the fundamental for the second harmonic, 3X the fundamental for the third and so on. This yields the harmonic distortion.

The signal to noise ratio is calculated by taking the rms sum of the frequency bins up to 255 (the Nyquist rate) with the exception of the dc term (bins 1, 2, and 3), the fundamental frequency (10 bins below the fundamental to 10 bins above the fundamental) and ±2 bins around each harmonic. The number of bins eliminated in each case is due to the leakage of the windowing function causing spillover into the area around the frequency terms. The summed frequency bins are then compared to the normalized fundamental for calculation of the broadband signal-to-noise ratio.



HARMONIC	BIN #	AMPLITUDE (dB)
1	251	- 1.04
2	10	-70.74
3	241	-80.69
4	20	-77.65
5	231	-80.07

SIGNAL-TO-NOISE RATIO = 65.10 dB
TOTAL HARMONIC DISTORTION = -68.17 dB
SIGNAL-TO-(NOISE + DISTORTION) = 63.68 dB
FFT size is 512 points.
Input Data Weighted by Hanning Window.

FIGURE 3. DYNAMIC TEST DATA

OFFSET AND GAIN ADJUSTMENT

The ADC-00113 is carefully laser-trimmed to its rated accuracy without external adjustments. The user may trim both input offset voltage error and gain error to zero by using external potentiometers (see Figure 4). The trim is typically 2%.

Note:

When large offset and gain changes are desired use other means, within the system, to achieve them; such as, using an input buffer amplifier.

For good high-speed analog practice, decoupling is recommended.

If offset and gain adjustment is not needed, pins 36 and 37 should be unconnected

TABLE 4. ADC-00113 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Case Ground	46	Analog Ground
2	NC	45	T/H Analog Input
3	+5V Analog Supply	44	+15V Supply
4	T/H Analog Output	43	-15V Supply
5	A/D Analog Input	42	-5.2V Analog Supply
6	-5.2V Analog Supply	41	NC
7	NC	40	NC(Factory Test Point)
8	NC	39	NC
9	Bit 1 (MSB)	38	NC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Analog Ground
13	Bit 5	34	+15V Supply
14	Bit 6	33	-15V Supply
15	Bit 7	32	Analog Ground
16	Bit 8	31	-5.2V Digital Supply
17	Bit 9	30	+5V Analog supply
18	Bit 10	29	NC (Factory Test Point)
19	Bit 11	28	NC (Factory Test Point)
20	Bit 12 (LSB)	27	Output Logic Invert
21	+5V Digital Supply	26	Digital Ground
22	Data Ready	25	$\overline{\text{Output Enable}}$
23	Digital Ground	24	Encode Command

Notes:

1. Pins 4 and 5 are to be externally connected.
2. NC means do not connect any signal to these pins as damage may occur to the hybrid.

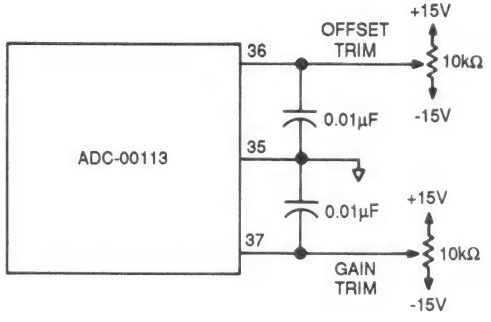
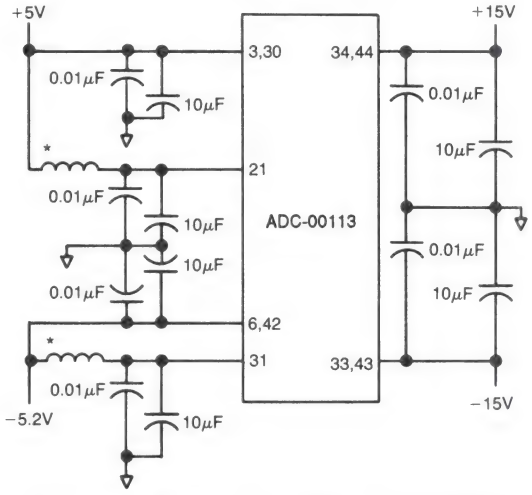


FIGURE 4. OFFSET AND GAIN ADJUSTMENT

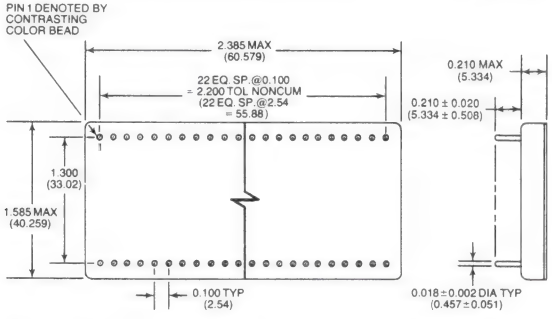
POWER SUPPLY DECOUPLING

Decoupling capacitors are required on each power supply to minimize noise. Figure 5 illustrates the recommended decoupling scheme. Each decoupled line must have a 10 µF or larger tantalum capacitor in parallel with a 0.01 µF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package. While the user may use the same power supply for the 5.2V analog and digital supplies, it is recommended that the supply lines to the ADC-00113 be separated at the supply and treated as individual supplies at the board in order to minimize crosstalk. The same applies to the 5V analog and digital supplies. It is further recommended that an inductor, such as the Ferrox Cube Bead model #VK20020/4B be used in the digital supply line to prevent digital switching from being transposed on the analog supply. For instances where the user has a separate analog and digital supplies: the +5V current drain is approximately 20% digital; and the -5.2V current drain is approximately 50% digital.



*Ferrite bead. (See text on **POWER SUPPLY DECOUPLING**).

FIGURE 5. POWER SUPPLY DECOUPLING



Notes:
1. Dimensions are in inches (mm).
2. Pin clusters to be centralized within ±0.010 of outline dimensions.

FIGURE 6. ADC-00113 MECHANICAL OUTLINE

ORDERING INFORMATION

ADC-00113 – 1 0 2

Reliability:
- 0 = Standard DDC procedures
- 1 = Military processing available (Consult Factory)
- 2 = Military processing available but without QCI testing.(Consult Factory)

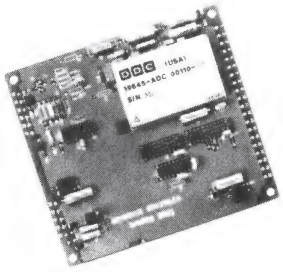
Operating Temperature Range:
- 1 = -55 to +125°C
- 3 = 0 to +70°C

Consult factory for ECL Logic Compatibility.

B

ADC-00115

12 BIT 5 MHz T/H + A/D BOARD HIGH SPEED



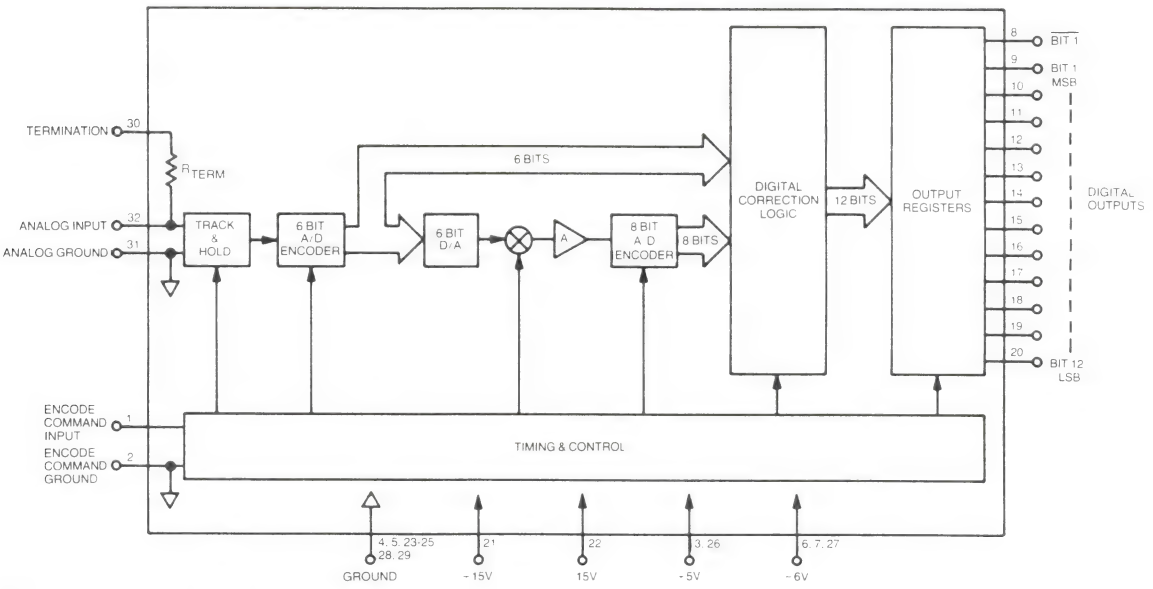
FEATURES

- *INCLUDES:*
  - *— TRACK/HOLD*
  - *— A/D CONVERTER*
  - *— TIMING CIRCUITS*
- *5 MHz WORD RATE*
- *PIN-FOR-PIN, LOW POWER MOD 1205 REPLACEMENT*

DESCRIPTION

The ADC-00115 is a 12 bit, 5 MHz track/hold and A/D converter board which pin-for-pin replaces the MOD 1205. Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00115 meets MOD 1205 form, fit, and function at lower power with higher performance and reliability. The ADC-00115 is implemented with a 2-step A/D conversion algorithm. The advent of the ADC-00110 hybrid makes the performance enhancements possible.

With its high speed and industry standard format, the ADC-00115 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and sonar digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high speed data acquisition and communications systems.



Note:
With pin 30 open, analog input impedance is 400 Ohms; with pin 30 grounded, analog impedance is 50 Ohms.

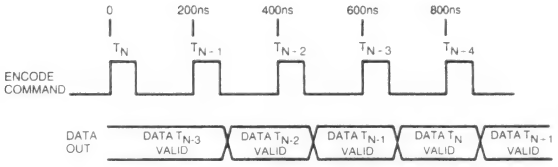
FIGURE 1. ADC-00115 BLOCK DIAGRAM

TABLE 1. ADC-00115 SPECIFICATIONS (T/H and A/D)
Typical values at +25°C case temperature, nominal power supply voltages unless otherwise noted.

MODEL	ADC-00115	
RESOLUTION (FS = FULL SCALE)	12 Bits (0.024% FS)	
LSB WEIGHT	1mV	
ACCURACY (INCLUDING LINEARITY) @ DC	±0.0125% Full Scale ±1/2LSB	
Monotonicity	Guaranteed (0 to +70°C)	
Nonlinearity vs. Temperature	0.0005% of FS/°C, max	
Gain vs. Temperature	0.002% of FS/°C, typ; 0.005% of FS/°C, max	
DYNAMIC CHARACTERISTICS		
AC Linearity[1] (dc to 1MHz)	Spurious Signals >70dB below FS, max	
(1MHz to 2.5MHz)	Spurious Signals >65dB below FS, max; >68dB, typ	
Conversion Time	See Text and Timing Diagram	
Conversion Rate (Word Rate)	dc to 5MHz min	
Aperture Uncertainty (Jitter)	±25ps max	
Aperture Time	6ns (±3ns from unit to unit)	
Signal to Noise Ratio[2]	64dB min; 66dB, typ	
Noise Power Ratio[3]	56dB min, 58dB typ	
Transient Response[4]	12-Bit (0.0125%) Accuracy within 200ns	
Overvoltage Recovery Time[5]	200ns	
Input Bandwidth (small signal, 3dB)	15MHz min	
Input Bandwidth (large signal, 3dB)	10MHz min; flat within ±0.1dB, dc through 5MHz	
ANALOG INPUT		
Voltage Range	±2.048V FS	
	±4V Absolute max	
Impedance	400Ω with pin 30 open, 50Ω with pin 30 grounded	
Offset Voltage	Adjust to 0 with On Board Potentiometer	
Offset vs. Temperature	0.002% FS/°C, typ; 0.005% of FS/°C, max	
ENCODE COMMAND INPUT		
Logic Levels, TTL Compatible	"0" = 0 to +0.4V	
	"1" = +2.4V to +5V	
Logic Loading	1 Standard TTL Gate	
Rise and Fall Times	10ns max	
Duration min/max	20ns min, Encode Command Period −20ns max	
Frequency (Random or Periodic)	dc to 5MHz min	
DIGITAL DATA OUTPUT		
Format	12 Parallel Bits, NRZ	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V	
	"1" = +2.4V to +5V	
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or	
	2 Standard TTL Loads	
Time Skew	10ns max	
Coding	Offset Binary (OBN) or 2's complement (2SC)	
Pipeline Delay	2 Encode Periods +275nsec (See figure 2)	
POWER REQUIREMENTS	typ	max
+15V ±5%	70mA	120mA
−15V ±5%	90mA	150mA
−6V ±5%	600mA	700mA
+5V ±5%	250mA	400mA
Power Consumption	7.25W	10.25W
TEMPERATURE RANGE		
Operating	0 to +70°C	
Storage	−55°C to +85°C	
Cooling Requirements	500 Linear Feet Per Min (LFPM) @ +70°C	
PHYSICAL CHARACTERISTICS		
Construction	Single Printed Circuit Card	

Table 1. Notes:

1. AC linearity expressed in terms of spurious in-band signals generated at specified encode rates at analog input frequencies.
2. Rms signal to rms noise at 500kHz analog input.
3. DC to 2.4MHz white noise bandwidth with slot frequency of 512kHz.
4. For full-scale step input, attains 12-bit accuracy in time specified.
5. Recovers to 12-bit accuracy after 2 X FS input overvoltage in time specified.



Note:
Data T_N (the result of the encode command T_N) occurs two conversion periods plus 275 ns after encode command T_N. For a 5MHz word rate as shown, data is valid 275 ns after the third encode command pulse or T_N + 675 ns. In all cases, three encode command pulses are required for transfer of data to the output, due to the pipeline delay effect through the A/D.

FIGURE 2. ADC-00115 TIMING DIAGRAM

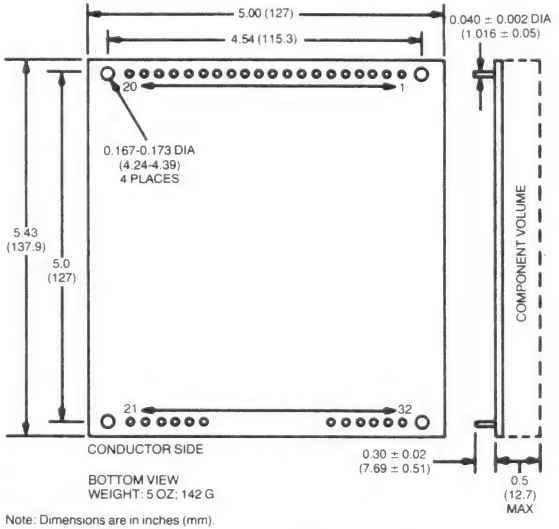
TABLE 2. ADC-00115 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ENCODE COMMAND	17	BIT 9
2	GND*	18	BIT 10
3	+5V	19	BIT 11
4	GND*	20	BIT 12 (LSB)
5	GND*	21	+15V
6	−6V	22	−15V
7	−6V	23	GND*
8	$\overline{\text{BIT 1}}$	24	GND*
9	BIT 1 (MSB)	25	GND*
10	BIT 2	26	+5V
11	BIT 3	27	−6V
12	BIT 4	28	GND*
13	BIT 5	29	GND*
14	BIT 6	30	TERMINATION
15	BIT 7	31	GND*
16	BIT 8	32	ANALOG INPUT

*All ground pins are connected together within the ADC-00115.

ORDERING INFORMATION

ADC-00115



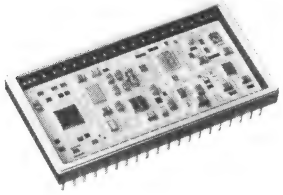
Note: Dimensions are in inches (mm).

FIGURE 3. ADC-00115 MECHANICAL OUTLINE

B

ADC-00145

14 BIT 5 MHz T/H + A/D HYBRID HIGH SPEED, SMALL SIZE



PRELIMINARY

DESCRIPTION

The ADC-00145 is a 14 bit, 200 nsec (5 MHz) track/hold and A/D converter hybrid, in 40 pin TDIP or flatpack packages, following in the footsteps of the industry standard ADC-00300.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00145 is the fastest and smallest digitizer of its kind.

The ADC-00145 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00145's technical breakthroughs in speed and size. Foremost among them were the high-speed T/H, DAC, and the gain amplifier. All are DDC proprietary designs and single custom monolithics. In addition, judicious use of thin-film and thick-film hybrid technology resulted in minimum layout area.

With its high speed, small package, and wide operating temperature range, the ADC-00145 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and sonar digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high-speed data-acquisition systems.

FEATURES

- ***Includes:***
  - ***–Track/Hold***
  - ***– A/D Converter***
  - ***–Tri-State Output Registers***
  - ***–Timing Circuits***
- ***5 MHz Word Rate***
- ***Small 40 Pin TDIP Hermetic Hybrid***

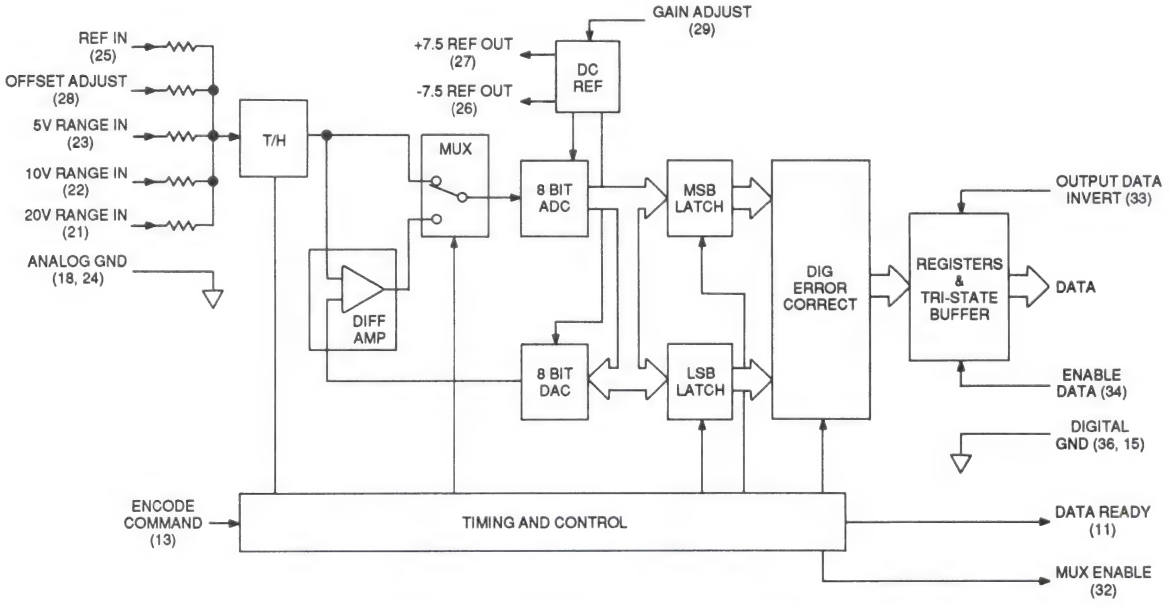


FIGURE 1. ADC-00145 BLOCK DIAGRAM

TABLE 1. ADC-00145 SPECIFICATIONS (T/H and A/D)
Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
RESOLUTION	Bits	14
ACCURACY		
Linearity Error	LSB	1 typ,
Linearity Error Tempco	ppm FSR/°C	± 1/2 max
Diff Linearity Error	LSB	±1 max
Gain Error(1)	%FSR	±0.5 max
Gain Error Tempco	ppm FSR/°C	15 max
Offset Error(1) Bipolar	%FSR	±0.5 max
Offset Error(1) Unipolar	%FSR	±1.2 max
Offset Error Tempco	ppm FSR/°C	8 typ.
DYNAMICS		
Conversion Rate(2)	MHz	DC to 5 min
Harmonics(3)	dB below FSR	78 min
Signal to Noise Ratio(2)(4)	dB	75 typ,
Input Bandwidth(2)		
Small Signal(5)	MHz	20 typ.
Large Signal(6)	MHz	20 typ.
Flat to 0.25 db	MHz	DC to 2.5
Aperture Jitter	psec	10 max
Apparent Aperture Delay	nsec	-5
Overvoltage Recovery(7)	µsec	5 max
ANALOG INPUT		See table 2
DIGITAL INPUTS		
Encode Command(8)		
Width	nsec	50 min, 150max
Rise/Fall Time	nsec	25 max
Frequency	MHz	DC to 5 min
Output Data Invert Loading	Ohms	50K
DIGITAL OUTPUTS		
Parallel Data		
Format	Bits	14(tri-state)
Drive	LS Loads	3
Coding		See table 3
Data Ready(9)		
Rise/Fall Time	nsec	25 max
Drive	LS Loads	3
INTERNAL REFERENCE		
Pos Voltage Output	V	+7.5±0.51%
Pos Current Output(10)	mA	±5
Pos Voltage Tempco	ppm/°C	±15 max
Neg Voltage Output	V	-7.5±1.2%
Neg Current Output(10)	mA	±5
Voltage Tempco (± Ref)	ppm/°C	±15 max
POWER SUPPLIES		
+15 Volt Supply	V	+15±5%
Current Drain	mA	50 typ, 75 max
-15 Volt Supply	V	-15±5%
Current Drain	mA	20 typ, 30 max
+5 Volt Supply	V	+5±5%
Current Drain	mA	250 typ, 325 max
-5 Volt Supply	V	-5±5%
Current Drain	mA	120 typ, 160 max
PSRR	%FSR/V	0.1

TABLE 1. ADC-00145 SPECIFICATIONS (T/H and A/D) (continued)

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	2.9 typ, 4.0 max
TEMPERATURE RANGE		
Operating (Case)		
-3 Option	°C	0 to +70
Storage	°C	-65 to +150
PACKAGE		
Type		40 pin TDIP
Size	in(mm)	1.2 x 2.2 x 0.2 (30.5 x 56.0 x 5.1)

Notes:
(1) Trimmable to zero with external potentiometer.
(2) Value specified over operating temperature range.
(3) For dc to 2.5MHz input with 5 MHz encode rate.
(4) Rms signal to rms noise ratio with 2.3 MHz analog input, within 0 to -1dB of peak.
(5) 3 dB bandwidth with analog input 40 dB below full scale.
(6) 3 dB bandwidth with full scale analog input.
(7) Recovery to rated accuracy from twice full scale input step.
(8) LOW to HIGH transition initiates encoding.
(9) LOW to HIGH transition indicates start of valid data interval.
(10) Current load for no performance degradation.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00145 sampling A/D converter. Its major elements are a track/hold amplifier, a 8-bit flash A/D converter, a 8-bit D/A converter, a differential amplifier, and a 2-channel multiplexer. The remaining functions are timing and control circuits, digital buffers and registers, and dc voltage references.

These components implement a 2-step A/D conversion algorithm, whose operation is quite straight-forward. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. Then, the flash A/D converter generates a coarse encode of the sampled voltage. Its 8-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 8-bit word is input to the DAC, which converts it to an analog voltage. The differential amplifier subtracts the voltage representing the coarse encode from the sampled input and scales it up to the correct full scale range. Next, the flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 8-bit word is stored in the LSB register. Finally, the contents of the 8-bit MSB and LSB registers are combined in the digital error correction circuit to yield a 14-bit output word. This 14-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffers.

The entire 2-step conversion can be accomplished in as little as 200 nsec. Since the ADC-00145 has output storage registers, its

digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

The ADC-00145 may be configured for any of seven (7) different input signal ranges by means of jumper wires between pins. Three bipolar ranges, two positive unipolar, and two negative unipolar input ranges are implemented by using the 2 internal references, along with precision resistors, to scale and offset the input signal.

The positive and negative internal references are made available to the user at output pins. If they are used, care must be taken not to load them beyond their rated outputs, or else converter performance will deteriorate. Residual gain and offset errors may be trimmed to zero, with the addition of external potentiometers.

A number of digital output codes are available from the ADC-00145(see Table 3). For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

Care must be taken when designing with the ADC-00145, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power-supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line and both internal references. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00145. Conductor lengths should be kept to a minimum, and a large-area ground-plane should be used to keep ground impedances as low as possible.

A

TIMING DIAGRAM

A diagram of typical ADC-00145 timing is shown in figure 2. It is to be noted that the diagram shows the Encode Command repeating at 200 nsec intervals which corresponds with the minimum conversion time. The Encode Command may be repeated up to 200 nsec intervals and is independent of internal timing.

A conversion cycle is initiated by the application of a positive pulse (25 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. The internal track/hold is placed in the HOLD mode and MUX Enable makes a LOW to HIGH transition 20 nsec max after the Encode Command leading edge. This delay reflects the digital aperture delay of the internal track/hold. Relay differential between T/H gate and T/H analog delay reflects the apparent aperature. MUX Enable remains HIGH for approximately 120 nsec before making a transition to LOW. This causes the track/hold to go into the TRACK mode.

At this point the internal flash A/D converter has completed its second encode and the track/hold can begin to acquire a new analog input. The remaining time in the conversion cycle is associated with delays through the digital sections that follow the flash A/D converter. Approximately 10 nsec after the HIGH to LOW transition of the MUX Enable signal the Data Ready signal makes a HIGH to LOW transition. The Data Ready line stays LOW for 50 nsec, during which time the output register is updated with the new data word. Updating the output data register is accomplished during the first 20 nsec of the interval

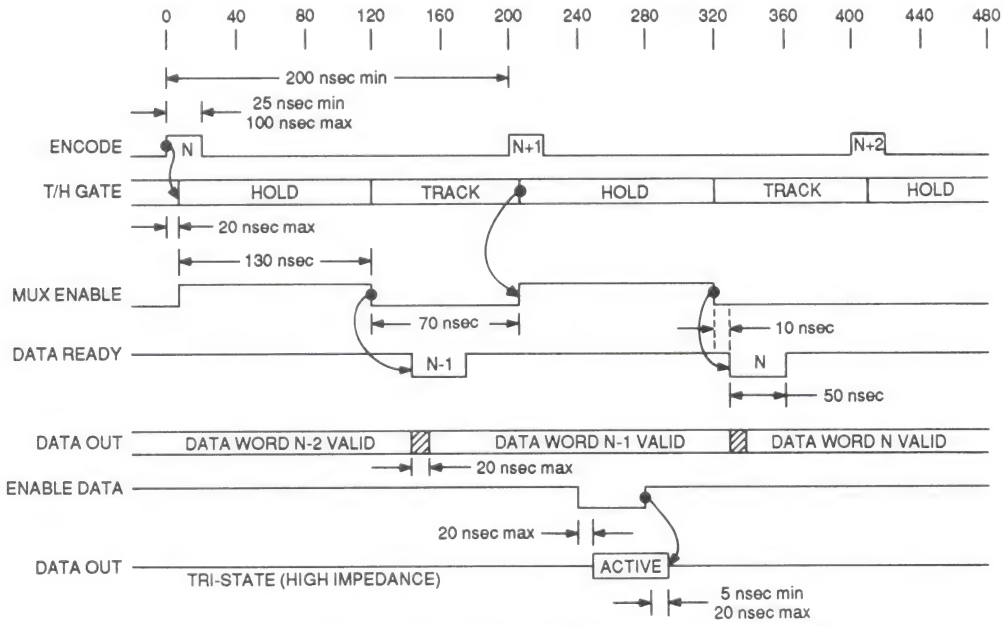


FIGURE 2. ADC-00145 TIMING DIAGRAM

during which the Data Ready line is LOW. Output data is not valid during this 20 nsec interval. ADC-00145 data is valid at all times that the Data Ready line is HIGH and during the final 30 nsec of its 50 nsec LOW interval.

Enable Data, which is active LOW, has a propagation delay of 10 nsec typ., 20 nsec max to active ADC-00145 data output. The LOW to HIGH transition of Enable Data is followed by a 5 nsec min, 20 nsec max tri-state propagation delay as illustrated in figure 2. The HIGH to LOW transition of the MUX Enable signal is passed through a delay chain that eventually generates the negative Data Ready pulse. If no additional Encode Commands are received, the MUX Enable line will remain Low. The timing diagram in figure 2 shows Encode Commands occurring at 200 nsec intervals.

MUX ENABLE

The ADC-00145 provides a Mux Enable signal (pin 32), whose rising edge is coincident with the internal HOLD signal (see figure 2). This signal can be used to advance the address to a multiplexer in time-division multiplexed applications.

ANALOG INPUT RANGES

The ADC-00145 may by configured for any of seven (7) different input signal ranges by means of jumper wires between pins. Three bipolar, two positive unipolar, and two negative unipolar ranges are possible. Table 2, Analog Input Range, lists the jumper connection and appropriate analog input terminal to be used for each configuration. For each analog input range, the absolute maximum input voltage is listed, along with the corresponding input impedance.

OUTPUT CODING

The ADC-00145 provides a number of digital output data codes. For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary . For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. Table 3, Output Coding, lists the output data for various analog inputs for each of the code configurations. The Output Data Invert pin (pin 33), when tied to +5V, inverts all of the above codes.

TABLE 2. ANALOG INPUT RANGE

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE*	INPUT TERMINAL	JUMPER CONNECTION
± 2.5V	± 5V	500Ω	PIN 23	PINS 21,22,25 TO PIN 24
± 5V	± 10V	1000Ω	PIN 22	PINS 21,23,25 TO PIN 24
± 10V	± 20V	2000Ω	PIN 21	PINS 21,23,25 TO PIN 24
0 to +5V	+10V	500Ω	PIN 23	PIN 25 TO PIN 26, PINS 21,22 TO PIN 24
0 to +10V	+20V	1000Ω	PIN 22	PIN 25 TO PIN 26, PINS 21,23 TO PIN 24
0 to -5V	-10V	500Ω	PIN 23	PIN 25 TO PIN 27, PINS 21,22 TO PIN 24
0 to -10V	-20V	1000Ω	PIN 22	PIN 25 TO PIN 27, PINS 21,23 TO PIN 24

*All unused input terminals must be connected to Analog Gnd.

TABLE 3. OUTPUT CODING(1)

INPUT VOLTAGE	BIPOLAR	POS UNIPOLAR	NEG UNIPOLAR
	Inverted Offset Binary	Inverted Binary	Inverted Binary
+FS - 1LSB	0000 0000 0000 00	0000 0000 0000 00	—
+3/4FS	0001 1111 1111 11	0011 1111 1111 11	—
+1/2FS	0011 1111 1111 11	0111 1111 1111 11	—
+1 LSB	0111 1111 1111 10	1111 1111 1111 10	—
0	0111 1111 1111 11	1111 1111 1111 11	0000 0000 0000 00
-1 LSB	1000 0000 0000 00	—	0000 0000 0000 01
-1/2LSB	1011 1111 1111 11	—	0111 1111 1111 11
-3/4LSB	1101 1111 1111 11	—	1100 0000 0000 00
-FS + 1LSB	1111 1111 1111 10	—	1111 1111 1111 11
-FS	1111 1111 1111 11	—	—

Note:
(1)Codes shown for pin 33 (Output Data Invert) open or tied to Ground. When Pin 34 is tied to +5V, all of the above codes are inverted.

PARALLEL OUTPUT DATA

Bit 1 (MSB) through Bit 14 (LSB), plus complement Bit 1, are the parallel output data lines provided by the ADC-00145. Each signal can drive a minimum of 3 standard TTL loads. Parallel output data is valid during the time that the Data Ready line is HIGH. If a strobe signal is required to read the parallel output data into a register, the rising edge of the Data Ready signal can drive a minimum of 3 standard TTL loads.

OUTPUT REGISTERS & TRI-STATE BUFFERS

The ADC-00145 has data output storage registers which hold the most recently converted 14-bit word. The data is available at the output at all times, except for the initial 30 nsec of the interval when the Data Ready line is LOW. The ADC-00145 also has tri-state output buffers, for parallel data bus operation. The buffer outputs remain in a high-impedance state until an Enable signal is received. The buffers can be made transparent (constantly enabled) by holding the Enable signal LOW. Where possible the user should avoid digital activity on the tri-stated output during the Track to Hold transition. Should this be unavoidable, an external tri-state buffer should be used for isolation.

LAYOUT PRECAUTIONS

The ADC-00145 high-speed sampling A/D converter generates high-frequency power-supply and ground currents, and is sensitive to coupled signals. High-frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large-area ground-plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package.

POWER SUPPLY DECOUPLING

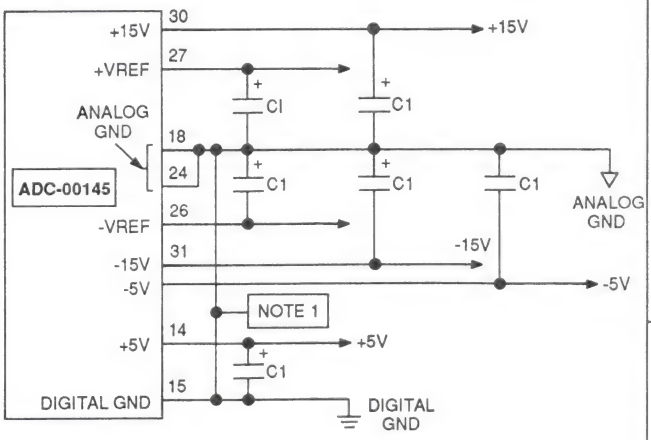
Decoupling capacitors are required on each power supply and both of the internal references to minimize noise. Figure 3 illustrates the recommended decoupling configuration. Each of the lines that is decoupled must have a 10 µF or larger tantalum capacitor. All capacitors must be mounted as close as possible to the hybrid package. The ADC-00145 has extensive ceramic capacitor decoupling internal to the hybrid.

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00145 are factory trimmed to be less than the values listed in Table 1, Specifications. Both gain and offset errors are trimmable to zero, with the use of external potentiometers. This affords the user with flexibility for maximizing performance for critical applications. Figures 4 and 5 show the external trim pot circuit required to trim gain and offset errors to zero. Multi-turn trim pots, with a temperature coefficient of less than 100 ppm/°C, are recommended for best results. If trim pots are not used, gain and offset adjust pins must be connected to analog ground.

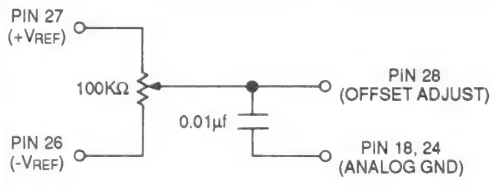
INTERNAL REFERENCE

The ADC-00145 contains +7.5V and -7.5V precision internal references, which are made available to the user. Care must be taken to observe the loading limitations on these references, to maintain rated performance. If the external load on either reference exceeds 5 mA, gain and linearity errors will increase. Damage will result from excessive loading.



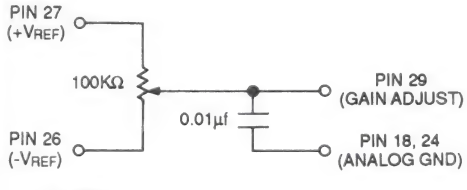
NOTES:
1. Analog ground and digital ground pins are to be connected together with a single short connection very close to the hybrid package.
2. C1 is a 10µf or larger tantalum capacitor.

FIGURE 3. POWER SUPPLY DECOUPLING



NOTE:
If offset trim pot is not used, offset adjust (pin 28) must be connected to analog ground.

FIGURE 4. OFFSET TRIM



NOTE:
If gain trim pot is not used, gain adjust (pin 29) must be connected to analog ground.

FIGURE 5. GAIN TRIM

TABLE 4. ADC-00145 PIN FUNCTIONS			
PIN	FUNCTION	PIN	FUNCTION
1	BIT 10	40	BIT 11
2	BIT 9	39	BIT 12
3	BIT 8	38	BIT 13
4	BIT 7	37	BIT 14 (LSB)
5	BIT 6	36	DIG GND
6	BIT 5	35	DNC (Factory Test Point)
7	BIT 4	34	ENABLE
8	BIT 3	33	OUTPUT DATA INVERT
9	BIT 2	32	MUX ENABLE
10	BIT 1 (MSB)	31	-15V
11	DATA READY	30	+15V
12	DNC (Factory Test Point)	29	GAIN ADJ
13	ENCODE	28	OFFSET ADJ
14	+5V	27	+7.5V REF
15	DIG. GND	26	-7.5V REF
16	-5V	25	REF IN
17	DNC (Factory Test Point)	24	ANA GND
18	ANA GND	23	5V RANGE
19	DNC (Factory Test Point)	22	10V RANGE
20	DNC (Factory Test Point)	21	20V RANGE

ORDERING INFORMATION

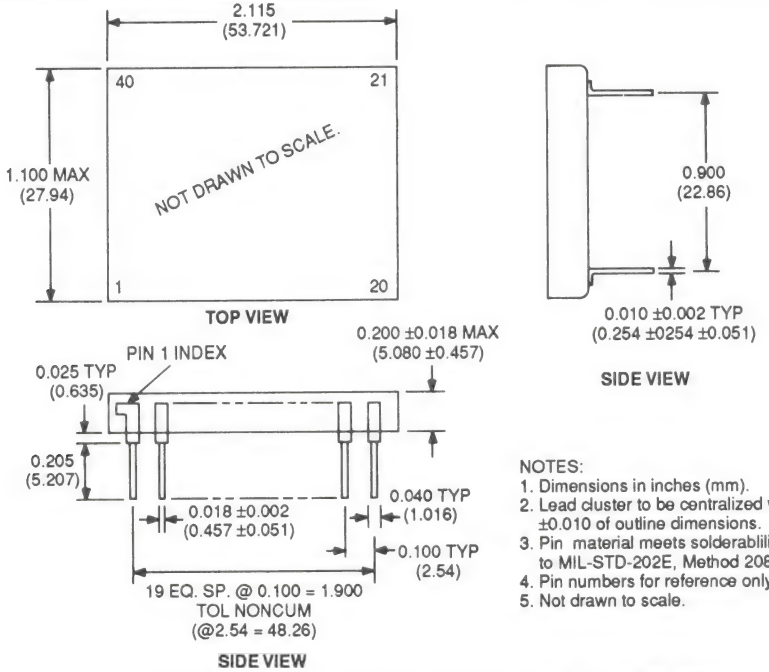
ADC- 00145 - 3 0 0

Reliability:
0 = Standard DDC procedures

Operating Temperature Range:
3 = 0 to +70°C

Packaging:
5 = 40 pin TDIP

Socket: Broadline SS-120-T-2 (or Samtec equivalent)

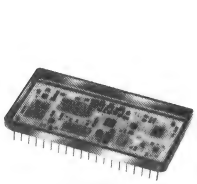


NOTES:
1. Dimensions in inches (mm).
2. Lead cluster to be centralized within ±0.010 of outline dimensions.
3. Pin material meets solderablility requirements to MIL-STD-202E, Method 208C.
4. Pin numbers for reference only.
5. Not drawn to scale.

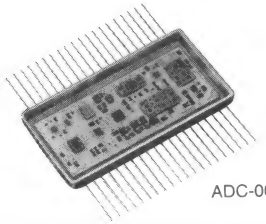
FIGURE 6. ADC-00145 MECHANICAL OUTLINE 40 Pin TDIP

ADC-00300® and ADC-00302®

12 BIT 2 MHz T/H + A/D HYBRID HIGH SPEED, SMALL SIZE



ADC-00300



ADC-00302

DESCRIPTION

The ADC-00300 is a 12 bit, 500nsec (2 MHz) track/hold and A/D converter hybrid in 40 pin TDIP or flatpack packages.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00300 is the fastest and smallest digitizer of its kind. The ADC-00300 operates over a temperature range of −55°C to +125°C and is available screened to MIL-STD-883.

The ADC-00300 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00300's technical breakthroughs in speed and size. Foremost among them were the high speed DAC and the amplifier which follows it. Both are DDC proprietary designs, and moreover the DAC is a single custom IC. In addition, judicious use of thin film and thick film hybrid technology resulted in minimum layout area.

With its high speed, small package and wide operating temperature range, the ADC-00300 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and sonar digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high speed data acquisition systems.

FEATURES

- *INCLUDES:*
  - *TRACK/HOLD*
  - *A/D CONVERTER*
  - *TRI-STATE OUTPUT REGISTERS*
  - *TIMING CIRCUITS*
- *2 MHz WORD RATE*
- *SMALL 40 PIN TDIP & FLATPACK HERMETIC HYBRIDS*
- *−55°C TO +125°C OPERATING TEMPERATURE*
- *MIL-STD-883B SCREENING*

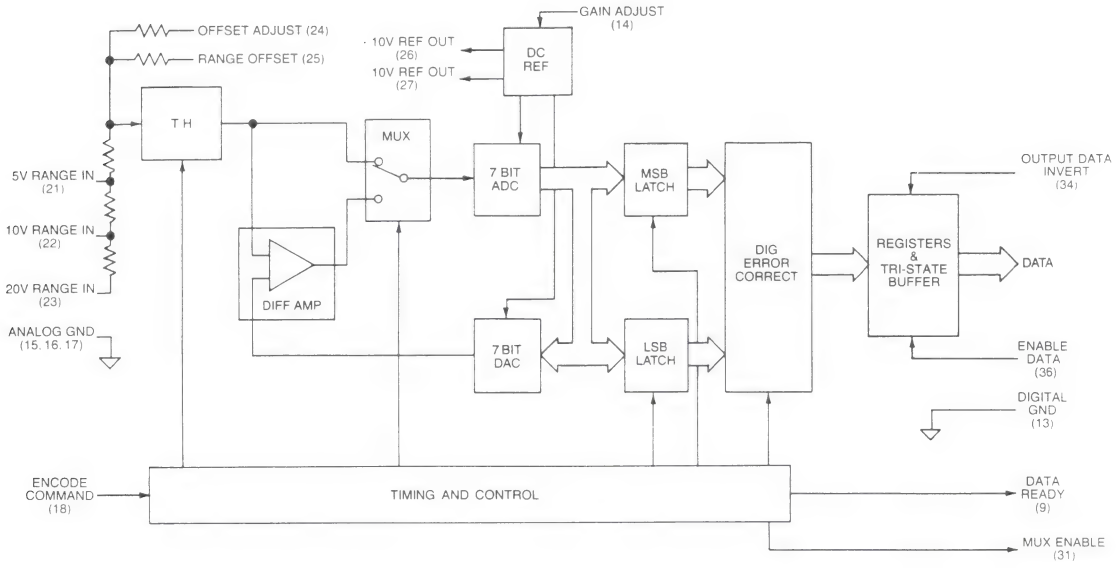


FIGURE 1. ADC-00300 BLOCK DIAGRAM

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TABLE 1. ADC-00300 SPECIFICATIONS (T/H and A/D)
Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
RESOLUTION	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.012 typ, ±0.025 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff Linearity Error	LSB	±1 max
Gain Error(1)	%FSR	±0.3 max
Gain Error Tempco	ppm FSR/°C	40
Offset Error(1)	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	20 max
DYNAMICS		
Conversion Rate(2)(13)	MHz	DC to 2 min
Harmonics(3)	db below FSR	72 typ, 68 min
Signal to Noise Ratio(2)(4)(13)	db	68 typ, 65 min
Input Bandwidth(2)		
Small Signal(5)	MHz	10 min
Large Signal(6)	MHz	10 min
Flat to 0.25 db	MHz	DC to 1
Aperture Jitter	psec	50 max
Aperture Delay	nsec	21 typ, 35 max
Overvoltage Recovery(7)	usec	5 max
ANALOG INPUT		See table 2
DIGITAL INPUTS		
Encode Command(8)		
Width	nsec	50 min, Tconv-50 max
Rise/Fall Time	nsec	25 max
Loading	HC Loads	4
Frequency	MHz	DC to 2 min
Enable Data Loading	HC Loads	4
Output Data Inv. Loading	Ohms	50K
DIGITAL OUTPUTS		
Parallel Data		
Format	Bits	12 (tri-state)
Drive	TTL Loads	3
Coding		See table 3
Data Ready(9)		
Rise/Fall Time	nsec	25 max
Drive	TTL Loads	3
INTERNAL REFERENCE		
Pos Voltage Output	V	+10 ± 0.65%
Pos Current Output(10)	mA	±2
Pos Voltage Tempco	ppm/°C	±25 max
Neg Voltage Output	V	−10 ± 0.5%
Neg Current Output(10)	mA	±2
Neg Voltage Tempco	ppm/°C	±20 max
POWER SUPPLIES		
+15 Volt Supply	V	+15 ± 5%
Current Drain	mA	70 typ, 85 max
−15 Volt Supply	V	−15 ± 5%
Current Drain	mA	75 typ, 90 max
+5 Volt Supply	V	+5 ± 5%
Current Drain	mA	175 typ, 200 max
PSRR	%FSR/V	0.1

TABLE 1. ADC-00300 SPECIFICATIONS (T/H and A/D) (Cont'd)
Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	3.0 typ, 3.6 max
THERMAL RESISTANCE		
$\theta_{c\text{-}a}$ (Case-Ambient)(11)	°C/W	15
$\theta_{j\text{-}c}$ (Junction-Case)(12)	°C/W	5.7
TEMPERATURE RANGE		
Operating (Case)		
−1 Option	°C	−55 to +125
−3 Option	°C	0 to +70
Storage	°C	−65 to +150
PACKAGE		
Type		40 pin TDIP and 40 pin flatpack
Size	in (mm)	1.2 x 2.2 x 0.2 (30.5 x 56.0 x 5.1)

Notes:
(1) Trimmable to zero with external potentiometer.
(2) Value specified over operating temperature range.
(3) For DC to 500 KHz input with 1.5 MHz encode rate.
(4) RMS signal to RMS noise ratio with 100 KHz analog input.
(5) 3 db bandwidth with analog input 40 db below full scale.
(6) 3 db bandwidth with full scale analog input.
(7) Recovery to rated accuracy from twice full scale input step.
(8) LOW to HIGH transition initiates encoding.
(9) LOW to HIGH transition indicates start of valid data interval.
(10) Current load for no performance degradation.
(11) Calculated using Pd = 3.0 W.
(12) Calculated using temperature of hottest die and Pd = 3.0 W.
(13) Specified over operating temperature range.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00300 sampling A/D converter. Its major elements are a track/hold amplifier, a 7-bit flash A/D converter, a 7-bit D/A converter, a differential amplifier, and a 2-channel multiplexer. The remaining functions are timing and control circuits, digital buffers and registers, and DC voltage references.

These components implement a 2-step A/D conversion algorithm, whose operation is quite straight-forward. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. Then, the flash A/D converter generates a coarse encode of the sampled voltage. Its 7-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 7-bit word is input to the DAC, which converts it to an analog voltage. The differential amplifier subtracts the voltage representing the coarse encode from the sampled input, and scales it up to the correct full scale range. Next, the flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 7-bit word is stored in the LSB register. Finally, the contents of the 7-bit MSB and LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffers.

The entire 2-step conversion can be accomplished in as little as 500 nsec. Since the ADC-00300 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

The ADC-00300 may be configured for any of nine (9) different input signal ranges by means of jumper wires between pins. Three bipolar ranges, two positive unipolar, and two negative unipolar input ranges are implemented by using the 2 internal references, along with precision resistors, to scale and offset the input signal.

The positive and negative internal references are made available to the user at output pins. If they are used, care must be taken not to load them beyond their rated outputs, or else converter performance will deteriorate. Residual gain and offset errors may be trimmed to zero, with the addition of external potentiometers.

A number of digital output codes are available from the ADC-00300 (see Table 3). For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

Care must be taken when designing with the ADC-00300, to achieve its rated performance. This high speed sampling A/D converter generates high frequency power supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line and both internal references. High frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00300. Conductor lengths should be kept to a minimum, and a large area ground plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A diagram of typical ADC-00300 timing is shown in figure 2. It is to be noted that the diagram shows the Encode Command repeating at 500 nsec intervals which corresponds with the minimum conversion time. The Encode Command may be repeated at greater than 500 nsec intervals and is independent of internal timing.

A conversion cycle is initiated by the application of a positive pulse (50 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. The internal track/hold is placed in the HOLD mode and MUX Enable makes a LOW to HIGH transition 35 nsec max after the Encode Command leading edge. This delay reflects the aperture delay of the internal track/hold. MUX Enable remains HIGH for approximately 240 nsec before making a transiton to LOW. This coincides with the track/hold going into the Track mode.

At this point the internal flash A/D converter has completed its coarse and fine encode and the track/hold can begin to acquire a new analog input. The remaining time in the conversion cycle is associated with delays through the digital sections that follow the flash A/D converter. Approximately 200 nsec after the HIGH to LOW transition of the MUX Enable signal the Data Ready signal makes a HIGH to LOW transition. The Data Ready line stays LOW for 100 nsec, during which time the output register is updated with the new data word. Updating the output data register is accomplished during the first 30 nsec of the interval

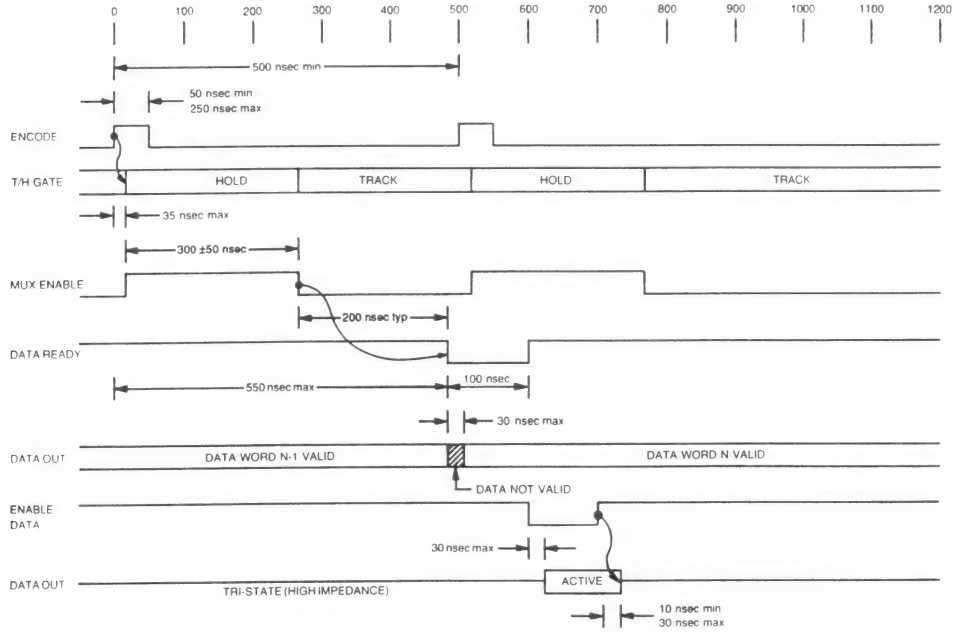


FIGURE 2. ADC-00300 TIMING DIAGRAM

during which the Data Ready line is LOW. Output data is not valid during this 30 nsec interval. ADC-00300 data is valid at all times that the Data Ready line is HIGH and during the final 70 nsec of its 100 nsec LOW interval.

Enable Data, which is active LOW, has a propagation delay of 15 nsec typ., 30 nsec max to active ADC-00300 data output. The LOW to HIGH transition of Enable Data is followed by a 10 nsec min, 30 nsec max tri-state propagation delay as illustrated in figure 2. The HIGH to LOW transition of the MUX Enable signal is passed through a delay chain that eventually generates the negative Data Ready pulse. If no additional Encode Commands are received, the MUX Enable line will remain LOW. The timing diagram in figure 2 shows Encode Commands occurring at 500 nsec intervals. Pin 10 must be tied to +5V, enabling operation from DC to 2MHz. A potentiometer for clock rate trim is not required.

MUX ENABLE

The ADC-00300 provides a MUX Enable signal (pin 31), whose digital state coincides with the internal HOLD T/H status (see figure 2). This signal can be used to advance the address to a multiplexer in time-division multiplexed applications.

ANALOG INPUT RANGES

The ADC-00300 may be configured for any of nine (9) different input signal ranges by means of jumper wires between pins. Three bipolar, three positive unipolar, and three negative unipolar ranges are possible. Table 2, Analog Input Range, lists the jumper connection and appropriate analog input terminal to be used for each configuration. For each analog input range, the absolute maximum input voltage is listed, along with the corresponding input impedance.

OUTPUT CODING

The ADC-00300 provides a number of digital output data codes. For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. Table 3, Output Coding, lists the output data for various analog inputs for each of the code configurations. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

TABLE 2. ANALOG INPUT RANGE

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT * IMPEDANCE	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±5V	500Ω	PIN 21	PIN 16 to PIN 25
±5V	±10V	1000Ω	PIN 22	PIN 16 to PIN 25
±10V	±20V	2000Ω	PIN 23	PIN 16 to PIN 25
0 to +5V	+10V	500Ω	PIN 21	PIN 25 to PIN 27
0 to +10V	+20V	1000Ω	PIN 22	PIN 25 to PIN 27
0 to +20V	+40V	2000Ω	PIN 23	PIN 25 to PIN 27
0 to −5V	−10V	500Ω	PIN 21	PIN 25 to PIN 26
0 to −10V	−20V	1000Ω	PIN 22	PIN 25 to PIN 26
0 to −20V	−40V	2000Ω	PIN 23	PIN 25 to PIN 26

* ±1.1% at 25°C, ±50 ppm/°C

TABLE 3. OUTPUT CODING(1)

INPUT VOLTAGE	BIPOLAR		POS UNIPOLAR	NEG UNIPOLAR
	Inverted Offset Binary	Inverted Two's Complement	Inverted Binary	Inverted Binary
+FS−1LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000	–
+¾FS	0001 1111 1111	1001 1111 1111	0011 1111 1111	–
+½FS	0011 1111 1111	1011 1111 1111	0111 1111 1111	–
+1LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110	–
0	0111 1111 1111	1111 1111 1111	1111 1111 1111	0000 0000 0000
−1 LSB	1000 0000 0000	0000 0000 0000	–	0000 0000 0001
−½FS	1011 1111 1111	0011 1111 1111	–	0111 1111 1111
−¾FS	1101 1111 1111	0111 1111 1111	–	1100 0000 0000
−FS+1LSB	1111 1111 1110	0111 1111 1110	–	1111 1111 1111
−FS	1111 1111 1111	0111 1111 1111	–	–
	B1 thru B12	$\overline{B1}$, B2 thru B12		

Note:
(1) Codes shown for pin 34 (Output Data Invert) open or tied to Ground. When pin 34 is tied to +5V, all of the above codes are inverted.

PARALLEL OUTPUT DATA

Bit 1 (MSB) through Bit 12 (LSB), plus complement Bit 1, are the parallel output data lines provided by the ADC-00300. Each signal can drive a minimum of 3 standard TTL loads. Parallel output data is valid during the time that the Data Ready line is HIGH. If a strobe signal is required to read the parallel output data into a register, the rising edge of the Data Ready signal can drive a minimum of 3 standard TTL loads.

OUTPUT REGISTERS & TRI-STATE BUFFERS

The ADC-00300 has data output storage registers which hold the most recently converted 12-bit word. The data is available at the output at all times, except for the initial 30 nsec of the interval when the Data Ready line is LOW. The ADC-00300 also has tri-state output buffers, for parallel data bus operation. The buffer outputs remain in a high impedance state until an Enable signal is received. The buffers can be made transparent (constantly enabled) by holding the Enable signal LOW.

LAYOUT PRECAUTIONS

The ADC-00300 high speed sampling A/D converter generates high frequency power supply and ground currents, and is sensitive to coupled signals. High frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package.

POWER SUPPLY DECOUPLING

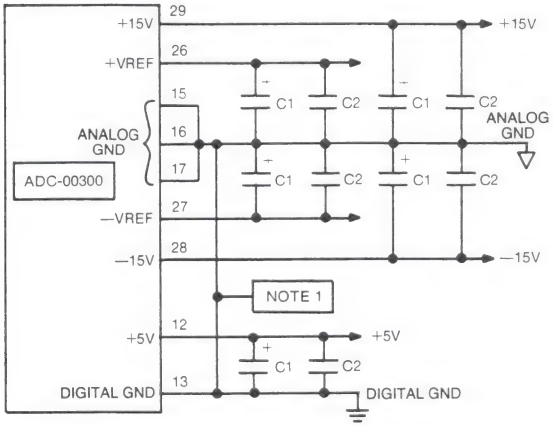
Decoupling capacitors are required on each power supply and both of the internal references to minimize noise. Figure 3 illustrates the recommended decoupling configuration. Each of the lines that is decoupled rnust have a 10 uF or larger tantalum capacitor in parallel with a 0.01 uF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00300 are factory trimmed to be less than the values listed in Table 1, Specifications. Both gain and offset errors are trimmable to zero, with the use of external potentiometers. This affords the user with flexibility for maximizing performance for critical applications. Figures 4 and 5 show the external trim pot circuit required to trim gain and offset errors to zero. Multi-turn trimpots, with temperature coefficient of less than 100 ppm/°C, are recommended for best results. If trim pots are not used, gain and offset adjust pins must be connected to analog ground.

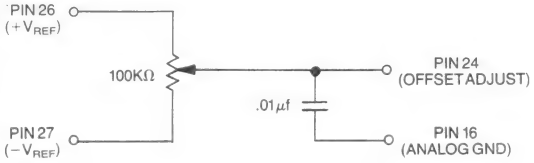
INTERNAL REFERENCE

The ADC-00300 contains +10V and −10V precision internal references, which are made available to the user. Care must be taken to observe the loading limitations on these references, to maintain rated performance. If the external load on either reference exceeds 2 mA, gain and linearity errors will increase. Damage will result from excessive loading.



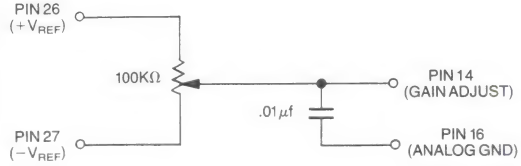
Notes:
(1) Analog ground and digital ground pins are to be connected together with a single short connection very close to the hybrid package.
(2) C1 is a 10μf or larger tantalum capacitor.
(3) C2 is a 0.01μf ceramic capacitor.

FIGURE 3. POWER SUPPLY DECOUPLING



Note:
If offset trim pot is not used, offset adjust (pin 24) must be connected to analog ground (pin 16).

FIGURE 4. OFFSET TRIM



Note:
If gain trim pot is not used, gain adjust (pin 14) must be connected to analog ground (pin 16).

FIGURE 5. GAIN TRIM

TABLE 4. ADC-00300 AND ADC-00302 PIN FUNCTIONS			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Bit 8	21	5V Range In
2	Bit 7	22	10V Range In
3	Bit 6	23	20V Range In
4	Bit 5	24	Offset Adjust
5	Bit 4	25	Range Offset
6	Bit 3	26	+10V Ref Out
7	Bit 2	27	−10V Ref Out
8	Bit 1 (MSB)	28	−15V Supply
9	Data Ready	29	+15V Supply
10	+5V Input *	30	NC (Factory Test Point)
11	NC (Factory Test Point)	31	MUX Enable
12	+5 V Supply	32	NC (Factory Test Point)
13	Digital Ground	33	NC (Factory Test Point)
14	Gain Adjust	34	Output Data Invert
15	Analog Ground	35	$\overline{\text{Bit 1 (MSB)}}$
16	Analog Ground	36	$\overline{\text{Enable Data}}$
17	Analog Ground	37	Bit 12 (LSB)
18	Encode Command	38	Bit 11
19	NC (Factory Test Point)	39	Bit 10
20	NC (Factory Test Point)	40	Bit 9

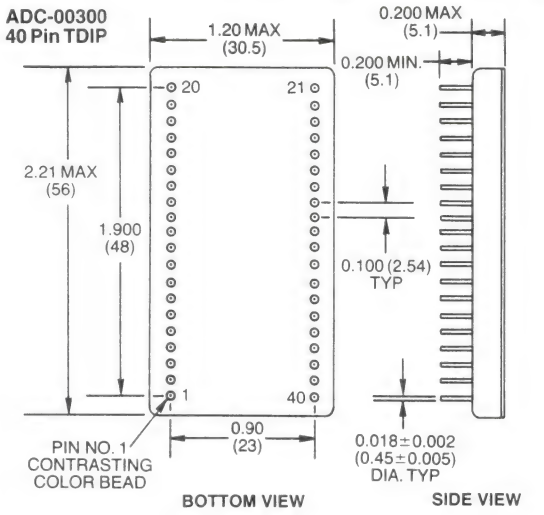
*External jumper to pin 12.

ORDERING INFORMATION

ADC-00300-302

- Reliability Grade
  - 0 = Standard DDC Processing
  - 1 = Fully compliant with MIL-STD-883
  - 2 = Screened to MIL-STD-883 but without QCI testing.
- Operating Temperature Range (case):
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Packaging:
  - 0 = 40 pin TDIP
  - 2 = 40 pin flatpack

Socket: Broadline SS-120-T-2 (or Samtec equivalent)



Notes:
(1) Dimensions in inches (mm).
(2) Lead identification numbers are for reference only.
(3) Lead spacing dimensions apply only at seating plane (TDIPs only).
(4) Lead cluster to be centralized within ±0.01 of outline dimension.
(5) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

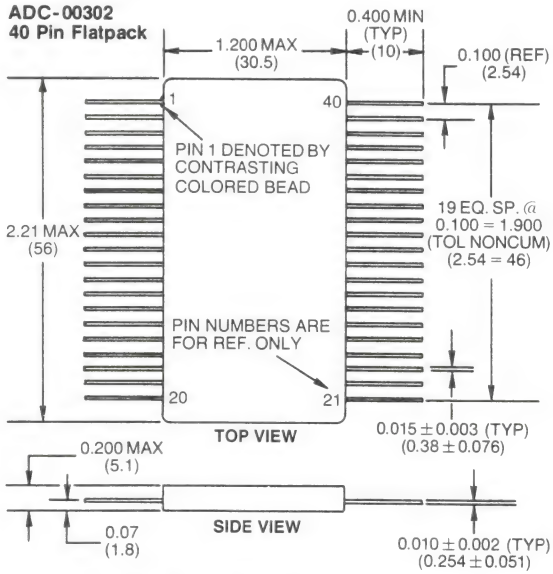
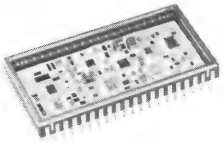


FIGURE 7. MECHANICAL OUTLINES

ADC-00305II

12 BIT 2 MHz T/H + A/D HYBRID
HIGH SPEED, SMALL SIZE, LOW COST



IMPROVED

DESCRIPTION

The ADC-00305II is a 12 bit, 500 nsec (2 MHz) track/hold and A/D converter hybrid packaged in a 40 pin TDIP, following in the footsteps of the industry standard ADC-00300 and ADC-00305.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00305II is a fast and small full-function digitizer. The ADC-00305II operates over a temperature range of 0°C to +70°C and is ideal for low-cost industrial applications.

The ADC-00305II is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00305II's technical breakthroughs in speed and size. Foremost among them were the high-speed T/H, DAC, and the gain amplifier. All are DDC proprietary designs and single custom monolithics. In addition, judicious use of thin-film and thick-film hybrid technology resulted in minimum layout area and power consumption.

With its high speed, small package, and wide operating temperature range, the ADC-00305II is ideal for the most demanding commercial data conversion applications. Typical of these applications are radar, IR, and NMR digitizing; vibration and FFT analysis; medical and scientific instrumentation; and high-speed data-acquisition systems.

FEATURES

- ***Includes:***
  - ***–Track/Hold***
  - ***–A/D Converter***
  - ***–Tri-state Output Registers***
  - ***–Timing Circuits***
- ***2 MHz Word Rate***
- ***Pin-for-pin Enhanced Revision to the ADC-00305***
- ***Low Power***
- ***Small 40 Pin TDIP Hermetic Hybrid***
- ***Low Cost***

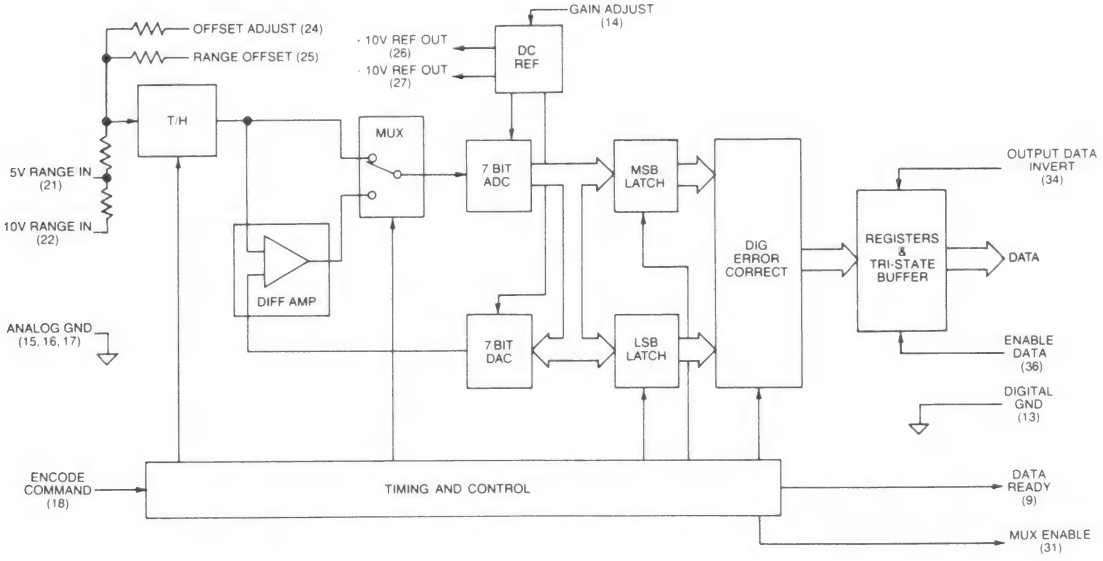


FIGURE 1. ADC-00305II BLOCK DIAGRAM

TABLE 1. ADC-00305II SPECIFICATIONS (T/H and A/D)
Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
RESOLUTION	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.012 typ, ±0.025 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff Linearity Error	LSB	±1 max
Gain Error(1)	%FSR	±0.5 max
Gain Error Tempco	ppm FSR/°C	40
Offset Error(1)	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	20 max
DYNAMICS		
Conversion Rate(2)	MHz	dc to 2 min
Harmonics(3)	dB below FSR	72 typ, 68 min
Signal to Noise Ratio(2)(4)	dB	68 typ, 65 min
Input Bandwidth(2)		
Small Signal(5)	MHz	10 min
Large Signal(6)	MHz	10 min
Flat to 0.25 dB	MHz	dc to 1
Aperture Jitter	psec	25 max
Aperture Delay	nsec	25 max
Overvoltage Recovery(7)	µsec	5 max
ANALOG INPUT		See table 2
DIGITAL INPUTS		
Encode Command(8)		
Width	nsec	50 min, 300max
Rise/Fall Time	nsec	25 max
Frequency	MHz	dc to 2 min
Output Data Invert Loading	Ohms	50K
DIGITAL OUTPUTS		
Parallel Data		
Format	Bits	12(tri-state)
Drive	TTL Loads	3
Coding		See table 3
Data Ready(9)		
Rise/Fall Time	nsec	25 max
Drive	TTL Loads	3
INTERNAL REFERENCE		
Pos Voltage Output	V	+10±0.65%
Pos Current Output(10)	mA	±2
Pos Voltage Tempco	ppm/°C	±25 max
Neg Voltage Output	V	-10±0.3%
Neg Current Output(10)	mA	±2
Neg Voltage Tempco	ppm/°C	±20 max
POWER SUPPLIES		
+15 Volt Supply	V	+15±5%
Current Drain	mA	40 typ, 60 max
-15 Volt Supply	V	-15±5%
Current Drain	mA	55 typ, 70 max
+5 Volt Supply	V	+5±5%
Current Drain	mA	175 typ, 220 max
-5 Volt Supply	V	+5±10%
Current Drain	mA	40 typ, 50 max
PSRR	%FSR/V	0.1

TABLE 1. ADC-00305II SPECIFICATIONS (T/H and A/D) (continued)

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	2.5 typ, 3.5 max
TEMPERATURE RANGE		
Operating (Case)	°C	0 to +70
PACKAGE		
Type		40 pin TDIP
Size	in(mm)	1.3 x 2.2 x 0.25 (33 x 56.0 x 6.4)

Notes:
(1) Trimmable to zero with external potentiometer.
(2) Value specified over operating temperature range.
(3) For dc to 1MHz input with 2 MHz encode rate.
(4) Rms signal to rms noise ratio with 200 kHz analog input.
(5) 3 dB bandwidth with analog input 40 dB below full scale.
(6) 3 dB bandwidth with full scale analog input.
(7) Recovery to rated accuracy from twice full scale input step.
(8) LOW to HIGH transition initiates encoding.
(9) LOW to HIGH transition indicates start of valid data interval.
(10) Current load for no performance degradation.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00305II sampling A/D converter following in the footsteps of the industry standard ADC-00300. Its major elements are a track/hold amplifier, a 7-bit flash A/D converter, a 7-bit D/A converter, a differential amplifier, and a 2-channel multiplexer. The remaining functions are timing and control circuits, digital buffers and registers, and dc voltage references.

These components implement a 2-step A/D conversion algorithm, whose operation is quite straight-forward. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. Then, the flash A/D converter generates a coarse encode of the sampled voltage. Its 7-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 7-bit word is input to the DAC, which converts it to an analog voltage. The differential amplifier subtracts the voltage representing the coarse encode from the sampled input and scales it up to the correct full scale range. Next, the flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 7-bit word is stored in the LSB register. Finally, the contents of the 7-bit MSB and LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffers.

The entire 2-step conversion can be accomplished in as little as 250 nsec. Since the ADC-00305II has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

The ADC-00305II may be configured for any of six (6) different input signal ranges by means of jumper wires between pins. Two bipolar ranges, two positive unipolar, and two negative unipolar input ranges are implemented by using the 2 internal references, along with precision resistors, to scale and offset the input signal.

The positive and negative internal references are made available to the user at output pins. If they are used, care must be taken not to load them beyond their rated outputs, or else converter performance will deteriorate. Residual gain and offset errors may be trimmed to zero, with the addition of external potentiometers.

A number of digital output codes are available from the ADC-00305II (see Table 3). For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

Care must be taken when designing with the ADC-00305II, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power-supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line and both internal references. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00305II. Conductor lengths should be kept to a minimum, and a large-area ground-plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A diagram of typical ADC-00305II timing is shown in figure 2. It is to be noted that the diagram shows the Encode Command repeating at 500 nsec intervals, which corresponds with the minimum conversion time. The Encode Command may be repeated at intervals ≥ 500 nsec and is independent of internal timing.

A conversion cycle is initiated by the application of a positive pulse (50 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. The internal track/hold is placed in the HOLD mode and MUX Enable makes a LOW to HIGH transition 25 nsec max after the Encode Command leading edge. This delay reflects the aperture delay of the internal track/hold. MUX Enable remains HIGH for approximately 160 nsec before making a transition to LOW. This coincides with the track/hold going into the TRACK mode.

At this point the internal flash A/D converter has completed its second encode and the track/hold can begin to acquire a new analog input. The remaining time in the conversion cycle is associated with delays through the digital sections that follow the flash A/D converter. Approximately 100 nsec after the HIGH to LOW transition of the MUX Enable signal the Data Ready signal makes a HIGH to LOW transition. The Data Ready line stays LOW for 100 nsec, during which time the output register is updated with the new data word. Updating the output data register is accomplished during the first 30 nsec of the interval

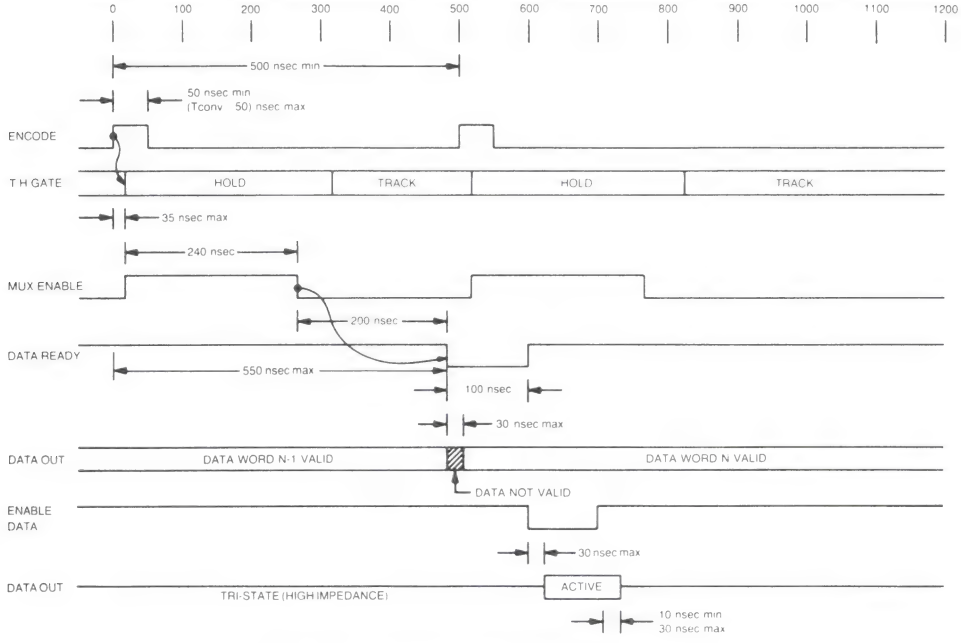


FIGURE 2. ADC-00305II TIMING DIAGRAM

during which the Data Ready line is LOW. Output data is not valid during this 30 nsec interval. ADC-00305II data is valid at all times that the Data Ready line is HIGH and during the final 70 nsec of its 100 nsec LOW interval.

Enable Data, which is active LOW, has a propagation delay of 15 nsec typ., 30 nsec max to active ADC-00305II data output. The LOW to HIGH transition of Enable Data is followed by a 10 nsec min, 30 nsec max tri-state propagation delay as illustrated in figure 2. The HIGH to LOW transition of the MUX Enable signal is passed through a delay chain that eventually generates the negative Data Ready pulse. If no additional Encode Commands are received, the MUX Enable line will remain Low. The timing diagram in figure 2 shows Encode Commands occurring at 500 nsec intervals. Pin 10 must be tied to +5V, enabling operation from dc to 2 MHz.

MUX ENABLE

The ADC-00305II provides a Mux Enable signal (pin 31), whose digital state is coincident with the internal T/H status (see figure 2). This signal can be used to advance the address to a multiplexer in time-division multiplexed applications.

ANALOG INPUT RANGES

The ADC-00305II may by configured for any of six (6) different input signal ranges by means of jumper wires between pins. Two bipolar, two positive unipolar, and two negative unipolar ranges are possible. Table 2, Analog Input Range, lists the jumper connection and appropriate analog input terminal to be used for each configuration. For each analog input range, the absolute maximum input voltage is listed, along with the corresponding input impedance.

OUTPUT CODING

The ADC-00305II provides a number of digital output data codes. For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. Table 3, Output Coding, lists the output data for various analog inputs for each of the code configurations. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

TABLE 2. ANALOG INPUT RANGE

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE (1)	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±5V	500Ω	PIN 21	PIN 16 to PIN 25
±5V	±10V	1000Ω	PIN 22	PIN 16 to PIN 25
0 to +5V	+10V	500Ω	PIN 21	PIN 25 to PIN 27
0 to +10V	+20V	1000Ω	PIN 22	PIN 25 to PIN 27
0 to −5V	−10V	500Ω	PIN 21	PIN 25 to PIN 26
0 to −10V	−20V	1000Ω	PIN 22	PIN 25 to PIN 26

Note: (1) ± 1.1% at 25°C, ± 50ppm/°C

TABLE 3. OUTPUT CODING (1)

INPUT VOLTAGE	BIPOLAR		POS UNIPOLAR	NEG UNIPOLAR
	Inverted Offset Binary	Inverted Two's Complement	Inverted Binary	Inverted Binary
+FS−1LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000	–
+¾FS	0001 1111 1111	1001 1111 1111	0011 1111 1111	–
+½FS	0011 1111 1111	1011 1111 1111	0111 1111 1111	–
+1LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110	–
0	0111 1111 1111	1111 1111 1111	1111 1111 1111	0000 0000 0000
−1LSB	1000 0000 0000	0000 0000 0000	–	0000 0000 0001
−½FS	1011 1111 1111	0011 1111 1111	–	0111 1111 1111
−¾FS	1101 1111 1111	0111 1111 1111	–	1100 0000 0000
−FS+1LSB	1111 1111 1110	0111 1111 1110	–	1111 1111 1111
−FS	1111 1111 1111	0111 1111 1111	–	–
	B1 thru B12	$\overline{B1}$, B2 thru B12		

Note:
(1)Codes shown for pin 34 (Output Data Invert) open or tied to Ground. When Pin 34 is tied to +5V, all of the above codes are inverted.

A

PARALLEL OUTPUT DATA

Bit 1 (MSB) through Bit 12 (LSB), plus complement Bit 1, are the parallel output data lines provided by the ADC-00305II. Each signal can drive a minimum of 3 standard TTL loads. Parallel output data is valid during the time that the Data Ready line is HIGH. If a strobe signal is required to read the parallel output data into a register, the rising edge of the Data Ready signal can drive a minimum of 3 standard TTL loads.

OUTPUT REGISTERS & TRI-STATE BUFFERS

The ADC-00305II has data output storage registers which hold the most recently converted 12-bit word. The data is available at the output at all times, except for the initial 30 nsec of the interval when the Data Ready line is LOW. The ADC-00305II also has tri-state output buffers, for parallel data bus operation. The buffer outputs remain in a high-impedance state until an Enable signal is received. The buffers can be made transparent (constantly enabled) by holding the Enable signal LOW. Where possible the user should avoid digital activity on the tri-stated output during the Track to Hold transition. Should this be unavoidable, an external tri-state buffer should be used for isolation.

LAYOUT PRECAUTIONS

The ADC-00305II high-speed sampling A/D converter generates high-frequency power-supply and ground currents, and is sensitive to coupled signals. High-frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large-area ground-plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package.

POWER SUPPLY DECOUPLING

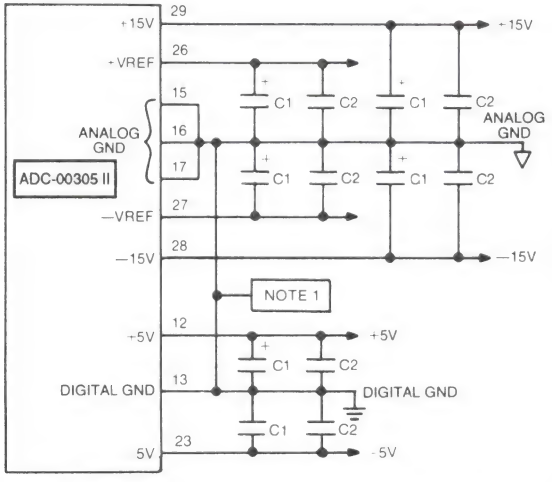
Decoupling capacitors are required on each power supply and both of the internal references to minimize noise. Figure 3 illustrates the recommended decoupling configuration. Each of the lines that is decoupled must have a 10 µF or larger tantalum capacitor in parallel with a 0.01 µF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00305II are factory trimmed to be less than the values listed in Table 1, Specifications. Both gain and offset errors are trimmable to zero, with the use of external potentiometers. This affords the user with flexibility for maximizing performance for critical applications. Figures 4 and 5 show the external trim pot circuit required to trim gain and offset errors to zero. Multi-turn trim pots, with a temperature coefficient of less than 100 ppm/°C, are recommended for best results. If trim pots are not used, gain and offset adjust pins must be connected to analog ground.

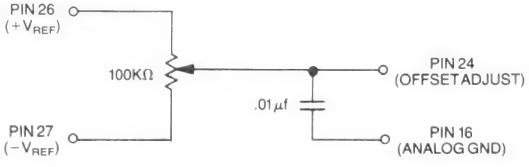
INTERNAL REFERENCE

The ADC-00305II contains +10V and -10V precision internal references, which are made available to the user. Care must be taken to observe the loading limitations on these references, to maintain rated performance. If the external load on either reference exceeds 2 mA, gain and linearity errors will increase. Damage will result from excessive loading.



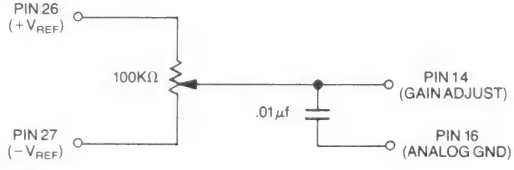
Notes:
(1) Analog ground and digital ground pins are to be connected together with a single short connection very close to the hybrid package
(2) C1 is a 10µf or larger tantalum capacitor.
(3) C2 is a 0.01µf ceramic capacitor.

FIGURE 3. POWER SUPPLY DECOUPLING



Note:
If offset trim pot is not used, offset adjust (pin 24) must be connected to analog ground (pin 16).

FIGURE 4. OFFSET TRIM



Note:
If gain trim pot is not used, gain adjust (pin 14) must be connected to analog ground (pin 16).

FIGURE 5. GAIN TRIM

TABLE 4. ADC-00305II PIN FUNCTIONS

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Bit 8	21	5V Range In
2	Bit 7	22	10V Range In
3	Bit 6	23	−5 V Supply
4	Bit 5	24	Offset Adjust
5	Bit 4	25	Range Offset
6	Bit 3	26	+10V Ref Out
7	Bit 2	27	−10V Ref Out
8	Bit 1 (MSB)	28	−15V Supply
9	Data Ready	29	+15V Supply
10	+5V Input *	30	NC (Factory Test Point)
11	NC (Factory Test Point)	31	MUX Enable
12	+5 V Supply	32	NC (Factory Test Point)
13	Digital Ground	33	NC (Factory Test Point)
14	Gain Adjust	34	Output Data Invert
15	Analog Ground	35	$\overline{\text{Bit 1}}$ ($\overline{\text{MSB}}$)
16	Analog Ground	36	Enable Data
17	Analog Ground	37	Bit 12 (LSB)
18	Encode Command	38	Bit 11
19	NC (Factory Test Point)	39	Bit 10
20	NC (Factory Test Point)	40	Bit 9

*External jumper to pin 12.

ORDERING INFORMATION

ADC- 00305II

Consult factory for ADC-00305-605 evaluation card.
Socket: Broadline SS-120-T-2 (or Samtec equivalent)

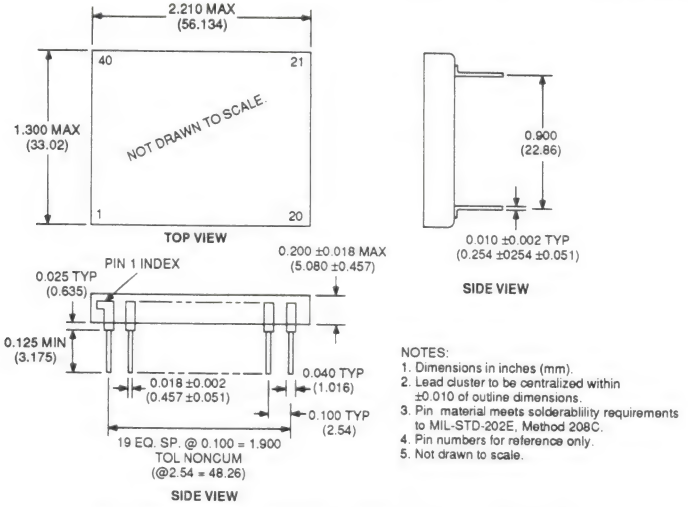
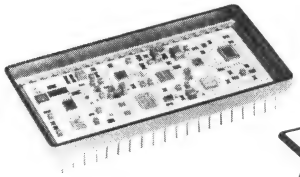


FIGURE 6. ADC-00305II MECHANICAL OUTLINE

ADC-00310

12 BIT 5 MHz T/H + A/D HYBRID
HIGH SPEED, SMALL SIZE, LOW COST



NEW

DESCRIPTION

The ADC-00310 is a 12 bit, 200 nsec (5 MHz) track/hold and A/D converter hybrid packaged in a 40 pin TDIP, following in the footsteps of the industry standard ADC-00300 and ADC-00305.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00310 is the fastest and smallest digitizer of its kind. The ADC-00310 operates over a temperature range of 0°C to +70°C and is ideal for low-cost industrial applications.

The ADC-00310 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00310's technical breakthroughs in speed and size. Foremost among them were the high-speed T/H, DAC, and the gain amplifier. All are DDC proprietary designs and single custom monolithics. In addition, judicious use of thin film and thick film hybrid technology resulted in minimum layout area.

With its high speed, small package, and wide operating temperature range, the ADC-00310 is ideal for the most demanding commercial data conversion applications. Typical of these applications are radar, IR, and NMR digitizing; vibration and FFT analysis; medical and scientific instrumentation; and high-speed data-acquisition systems.

FEATURES

- *INCLUDES:*
  - *–TRACK/HOLD*
  - *–A/D CONVERTER*
  - *–TRI-STATE OUTPUT REGISTERS*
  - *–TIMING CIRCUITS*
- *5 MHz WORD RATE*
- *PIN-FOR-PIN ADC-00305*
- *SMALL 40 PIN TDIP HERMETIC HYBRID*
- *LOW COST*

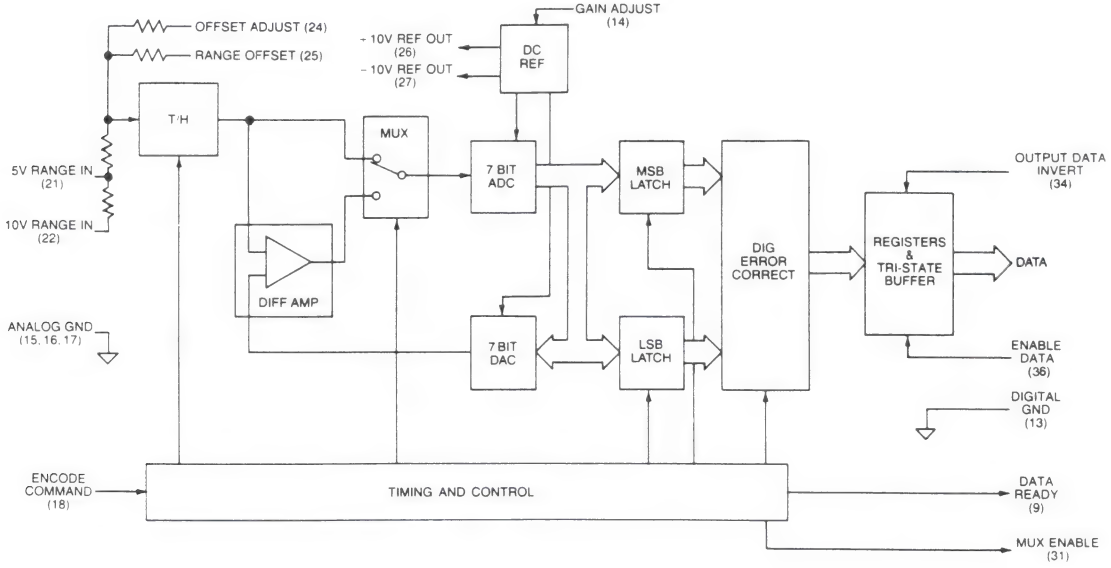


FIGURE 1. ADC-00310 BLOCK DIAGRAM

TABLE 1. ADC-00310 SPECIFICATIONS (T/H and A/D)
Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
RESOLUTION	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.012 typ, ±0.025 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff Linearity Error	LSB	±1 max
Gain Error(1)	%FSR	±0.3 max
Gain Error Tempco	ppm FSR/°C	40
Offset Error(1)	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	20 max
DYNAMICS		
Conversion Rate(2)	MHz	DC to 5 min
Harmonics(3)	db below FSR	72 typ, 68 min
Signal to Noise Ratio(2)(4)	db	68 typ, 65 min
Input Bandwidth(2)		
Small Signal(5)	MHz	10 min
Large Signal(6)	MHz	10 min
Flat to 0.25 db	MHz	DC to 1
Aperture Jitter	psec	25 max
Aperture Delay	nsec	25 max
Overvoltage Recovery(7)	µsec	5 max
ANALOG INPUT		See table 2
DIGITAL INPUTS		
Encode Command(8)		
Width	nsec	50 min, 150max
Rise/Fall Time	nsec	25 max
Frequency	MHz	DC to 4 min
Output Data Invert Loading	Ohms	50K
DIGITAL OUTPUTS		
Parallel Data		
Format	Bits	12(tri-state)
Drive	TTL Loads	3
Coding		See table 3
Data Ready(9)		
Rise/Fall Time	nsec	25 max
Drive	TTL Loads	3
INTERNAL REFERENCE		
Pos Voltage Output	V	+10±0.65%
Pos Current Output(10)	mA	±2
Pos Voltage Tempco	ppm/°C	±25 max
Neg Voltage Output	V	-10±0.3%
Neg Current Output(10)	mA	±2
Neg Voltage Tempco	ppm/°C	±20 max
POWER SUPPLIES		
+15 Volt Supply	V	+15±5%
Current Drain	mA	55 typ, 75 max
-15 Volt Supply	V	-15±5%
Current Drain	mA	15 typ, 25 max
+5 Volt Supply	V	+5±5%
Current Drain	mA	165 typ, 200 max
-5 Volt Supply	V	+5±10%
Current Drain	mA	85 typ, 130 max
PSRR	%FSR/V	0.1

TABLE 1. ADC-00310 SPECIFICATIONS (T/H and A/D) (continued)

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	2.3 typ, 3.4 max
TEMPERATURE RANGE		
Operating (Case)	°C	0 to +70
PACKAGE		
Type		40 pin TDIP
Size	in(mm)	1.3 x 2.2 x 0.25 (33 x 56.0 x 6.4)

Notes:
(1) Trimmable to zero with external potentiometer.
(2) Value specified over operating temperature range.
(3) For DC to 1MHz input with 5 MHz encode rate.
(4) RMS signal to RMS noise ratio with 200 kHz analog input.
(5) 3 db bandwidth with analog input 40 db below full scale.
(6) 3 db bandwidth with full scale analog input.
(7) Recovery to rated accuracy from twice full scale input step.
(8) LOW to HIGH transition initiates encoding.
(9) LOW to HIGH transition indicates start of valid data interval.
(10) Current load for no performance degradation.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00310 sampling A/D converter following in the footsteps of the industry standard ADC-00305. Its major elements are a track/hold amplifier, a 7-bit flash A/D converter, a 7-bit D/A converter, a differential amplifier, and a 2-channel multiplexer. The remaining functions are timing and control circuits, digital buffers and registers, and DC voltage references.

These components implement a 2-step A/D conversion algorithm, whose operation is quite straight-forward. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. Then, the flash A/D converter generates a coarse encode of the sampled voltage. Its 7-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 7-bit word is input to the DAC, which converts it to an analog voltage. The differential amplifier subtracts the voltage representing the coarse encode from the sampled input and scales it up to the correct full scale range. Next, the flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 7-bit word is stored in the LSB register. Finally, the contents of the 7-bit MSB and LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffers.

The entire 2-step conversion can be accomplished in as little as 250 nsec. Since the ADC-00310 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

The ADC-00310 may be configured for any of six (6) different input signal ranges by means of jumper wires between pins. Two bipolar ranges, two positive unipolar, and two negative unipolar input ranges are implemented by using the 2 internal references, along with precision resistors, to scale and offset the input signal.

The positive and negative internal references are made available to the user at output pins. If they are used, care must be taken not to load them beyond their rated outputs, or else converter performance will deteriorate. Residual gain and offset errors may be trimmed to zero, with the addition of external potentiometers.

A number of digital output codes are available from the ADC-00310 (see Table 3). For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

Care must be taken when designing with the ADC-00310, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power-supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line and both internal references. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00310. Conductor lengths should be kept to a minimum, and a large-area ground-plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A diagram of typical ADC-00310 timing is shown in figure 2. It is to be noted that the diagram shows the Encode Command repeating at 250 nsec intervals which does not correspond with the minimum conversion time. The Encode Command may be repeated at intervals ≥ 200 nsec and is independent of internal timing.

A conversion cycle is initiated by the application of a positive pulse (50 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. The internal track/hold is placed in the HOLD mode and MUX Enable makes a LOW to HIGH transition 25 nsec max after the Encode Command leading edge. This delay reflects the aperture delay of the internal track/hold. MUX Enable remains HIGH for approximately 160 nsec before making a transition to LOW. This coincides with the track/hold going into the TRACK mode.

At this point the internal flash A/D converter has completed its second encode and the track/hold can begin to acquire a new analog input. The remaining time in the conversion cycle is associated with delays through the digital sections that follow the flash A/D converter. Approximately 100 nsec after the HIGH to LOW transition of the MUX Enable signal the Data Ready signal makes a HIGH to LOW transition. The Data Ready line stays LOW for 100 nsec, during which time the output register is updated with the new data word. Updating the output data register is accomplished during the first 30 nsec of the interval

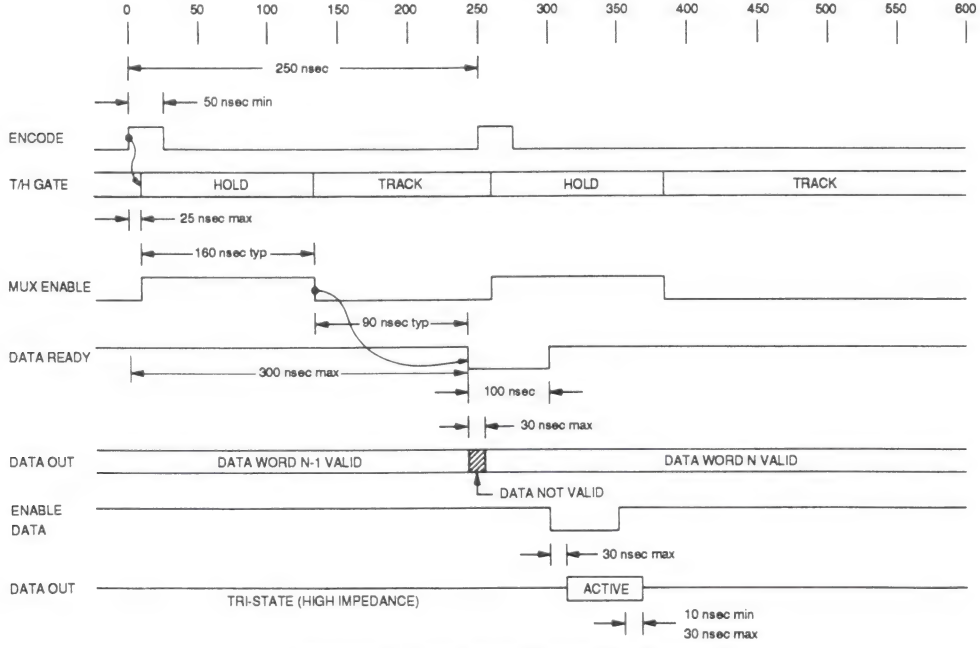


FIGURE 2. ADC-00310 TIMING DIAGRAM

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Note: (1) ±1.1% at 25°C, ±50 ppm/°C

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+½FS	0011 1111 1111	1011 1111 1111	0111 1111 1111	–
+1LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110	–
0	0111 1111 1111	1111 1111 1111	1111 1111 1111	0000 0000 0000
−1 LSB	1000 0000 0000	0000 0000 0000	–	0000 0000 0001
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−¾FS	1101 1111 1111	0111 1111 1111	–	1100 0000 0000
−FS+1LSB	1111 1111 1110	0111 1111 1110	–	1111 1111 1111
−FS	1111 1111 1111	0111 1111 1111	–	–
	B1 thru B12	$\overline{B1}$, B2 thru B12		

Note:
(1)Codes shown for pin 34 (Output Data Invert) open or tied to Ground. When Pin 34 is tied to +5V, all of the above codes are inverted.

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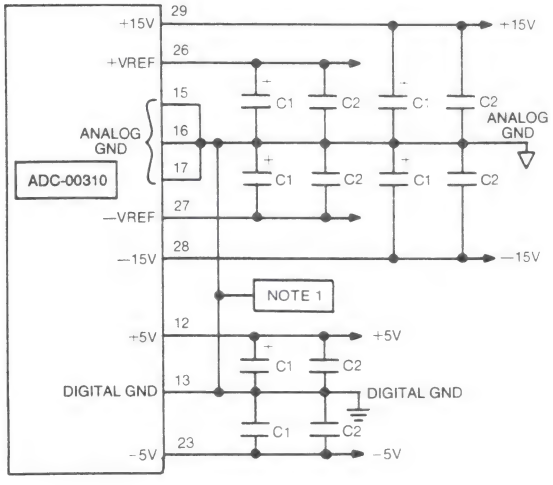
OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00310 are factory trimmed to be less than the values listed in Table 1, Specifications. Both gain and offset errors are trimmable to zero, with the use of external potentiometers. This affords the user with flexibility for maximizing performance for critical applications. Figures 4 and 5 show the external trim pot circuit required to trim gain and offset errors to zero. Multi-turn trim pots, with a temperature coefficient of less than 100 ppm/°C, are recommended for best results. If trim pots are not used, gain and offset adjust pins must be connected to analog ground.

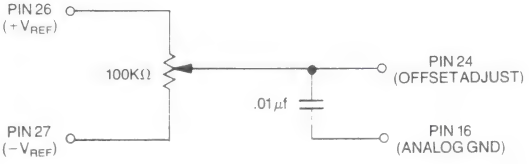
INTERNAL REFERENCE

The ADC-00310 contains +10V and -10V precision internal references, which are made available to the user. Care must be taken to observe the loading limitations on these references, to maintain rated performance. If the external load on either reference exceeds 2 mA, gain and linearity errors will increase. Damage will result from excessive loading.



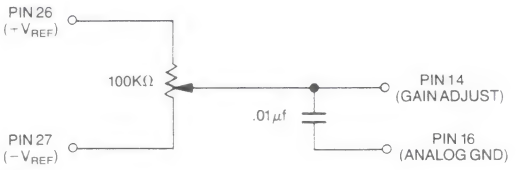
Notes:
(1) Analog ground and digital ground pins are to be connected together with a single short connection very close to the hybrid package.
(2) C1 is a 10µf or larger tantalum capacitor.
(3) C2 is a 0.01µf ceramic capacitor.

FIGURE 3. POWER SUPPLY DECOUPLING



Note:
If offset trim pot is not used, offset adjust (pin 24) must be connected to analog ground (pin 16).

FIGURE 4. OFFSET TRIM

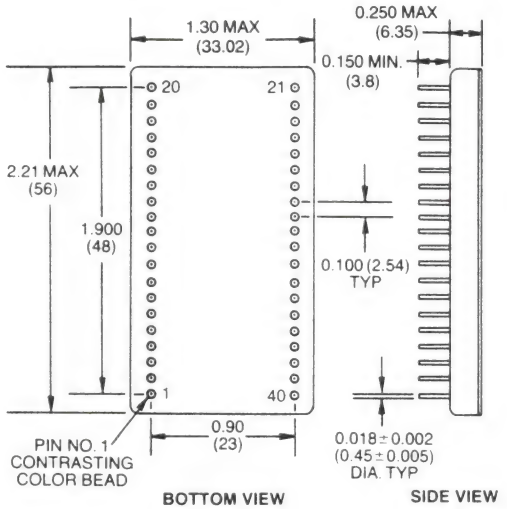


Note:
If gain trim pot is not used, gain adjust (pin 14) must be connected to analog ground (pin 16).

FIGURE 5. GAIN TRIM

TABLE 4. ADC-00310 PIN FUNCTIONS			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Bit 8	21	5V Range In
2	Bit 7	22	10V Range In
3	Bit 6	23	−5 V Supply
4	Bit 5	24	Offset Adjust
5	Bit 4	25	Range Offset
6	Bit 3	26	+10V Ref Out
7	Bit 2	27	−10V Ref Out
8	Bit 1 (MSB)	28	−15V Supply
9	Data Ready	29	+15V Supply
10	+5V Input *	30	NC (Factory Test Point)
11	NC (Factory Test Point)	31	MUX Enable
12	+5 V Supply	32	NC (Factory Test Point)
13	Digital Ground	33	NC (Factory Test Point)
14	Gain Adjust	34	Output Data Invert
15	Analog Ground	35	$\overline{\text{Bit 1 (MSB)}}$
16	Analog Ground	36	Enable Data
17	Analog Ground	37	Bit 12 (LSB)
18	Encode Command	38	Bit 11
19	NC (Factory Test Point)	39	Bit 10
20	NC (Factory Test Point)	40	Bit 9

*External jumper to pin 12.



Notes:
(1) Dimensions in inches (mm).
(2) Lead identification numbers are for reference only.
(3) Lead spacing dimensions apply only at seating plane.
(4) Lead cluster to be centralized within ±0.01 of outline dimension.

FIGURE 6. ADC-00310 MECHANICAL OUTLINE

ORDERING INFORMATION

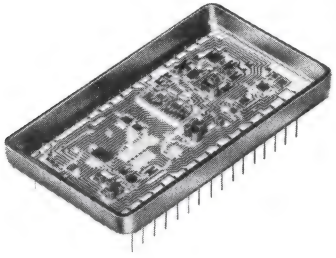
ADC- 00310

Consult factory for ADC-00305-605 evaluation card.
Socket: Broadline SS-120-T-2 (or Samtec equivalent)

B

ADC-00403 AND ADC-00404

12 BIT 2μSEC HYBRID A/D CONVERTERS
Low cost, military, standard pin out



FEATURES

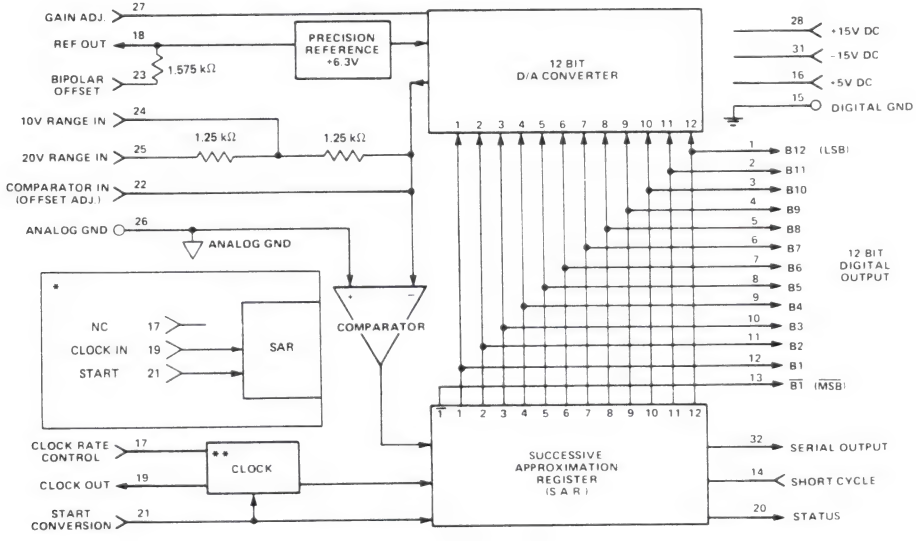
- *2 μSEC CONVERSION TIME*
- *12 BIT RESOLUTION AND LINEARITY*
- *LOW COST*
- *HIGHER SPEED PIN FOR PIN REPLACEMENT FOR ADC87 TYPES (NO BUFFER)*
- *32 PIN TDIP HERMETIC HYBRID*

DESCRIPTION

The ADC-00403 is a 12 bit 2 microsecond hybrid A/D converter packaged in a hermetic 32 pin TDIP. It offers a low cost higher speed pin for pin replacement for ADC87 and ADC85 types. Offered in models with internal (ADC-00404) or external (ADC-00403) clock, it also features precision internal reference, 6 pin programmable input voltage ranges, and both serial and parallel data output.

APPLICATIONS

With its low cost, high speed and small hermetic package, the ADC-00403 is ideal for most military and industrial data conversion applications. Typical of these applications are vibration and FFT analysis, sonar and radar digitizing, medical and nuclear instrumentation, and multiplexed data acquisition systems.



*Function for ADC-00403 model only.
**Function for ADC-00404 model only.

FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS Typical values at + 25°C case temperature and nominal power supply voltages				
PARAMETER	UNITS	VALUES 10 BIT LIN	 12 BIT LIN	
RESOLUTION	**Bits**	**12**	**12**	
ACCURACY AND DYNAMICS				
Linearity Error	% of F.S.R.	±0.048 max	±0.012 max	
Linearity Error Tempco	ppm/°C	±5 max	±2 max	
Gain Error (Trimmable to zero)	% of F.S.R.	±0.1	±0.1	
Gain Error Tempco	ppm/°C	±25	±15	
Offset (Trimmable to zero)				
Unipolar	% of F.S.R.	±0.05 typ	±0.05 typ	
Bipolar	% of F.S.R.	±0.1 typ	±0.1 typ	
Offset Tempco				
Unipolar	ppm/°C	±3 max	±3 max	
Bipolar	ppm/°C	±10 max	±7 max	
Diff. Linearity Error	LSB	±1	±1	
Conversion Time*	µs	1.5 max	2.0 max	
Cycle Time*	µs	1.7 max	2.2 max	
* The internal clock frequency is controlled by the applied Clock Rate Control voltage. See figure 4.				
ANALOG INPUTS				
Input Ranges				
Unipolar	V	0 to +5; 0 to +10; 0 to +20		
Bipolar	V	±2.5; ±5; ±10		
Max Voltage Without Damage		See figure 6.		
Impedance				
0 to +5V and ±2.5V	KΩ	0.625		
0 to 10V and ±5V	KΩ	1.25		
±10V	KΩ	2.50		
DIGITAL INPUTS				
Start Convert	nsec	50 min positive pulse. Trailing edge initiates conversion		
Loading	TTL loads	1		
DIGITAL OUTPUTS				
Parallel Data		Bit 1 through Bit 12 plus $\overline{MSB}$		
Drive	TTL loads	5		
Unipolar Coding		Complementary binary		
Bipolar Coding		Complementary offset binary or Complementary two's complement		
Serial Data		Non return to zero (NRZ)		
Drive	TTL loads	5		
Coding		Same as parallel data		
Status		Logic "1" during conversion. Logic "0" indicates valid parallel data.		
Drive	TTL loads	2		
Clock		13 positive pulses		
Period*	nsec	166 min		
Drive	TTL loads	2		
INTERNAL REFERENCE				
Voltage Output	V	+6.2 ±5%		
Current Output	mA	5 max for no degradation of specifications		
Voltage Tempco	ppm/°C	±20 max		
POWER SUPPLIES				
Voltages	V	+15 ±5%	−15 ±5%	+5 ±5%
Max Voltage Without Damage	V	+18	−18	+7
Current (Including Internal Clock)	mA	50 typ 60 max	65 typ 80 max	165 typ 220 max
Sensitivity	%FSR/%PS	±0.002	±0.002	±0.002
TEMPERATURE RANGE				
Operating (Case)				
-1 Option	°C	−55 to +125		
-2 Option	°C	−25 to +85		
Storage	°C	−65 to +135		
PACKAGE				
Type		32 pin TDIP		
Size	Inch (mm)	1.16 x 1.95 x 0.2 (29.34 x 49.4 x 5.0)		
Weight	Oz. (g)	0.67 (19)		

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the ADC-00403. Since the ADC-00403 is a successive approximation A/D converter, its main elements are a D/A Converter, a Comparator and a Successive Approximation Register. An Internal Precision Reference and internal or external Clock, depending on model selected, complete the functional elements of the ADC-00403.

The successive approximation algorithm is initiated by a Start Conversion pulse input. This results in a change of the Status output signal, indicating that a conversion is in progress and output data is invalid. In a sequence starting with Bit 1, the D/A input is set to "1" and the comparator detects whether the resulting D/A output is larger or smaller than the analog input signal. If the D/A output is larger than the analog input signal, Bit 1 is reset to "0". If not, then Bit 1 remains a "1". In succession, Bit 2 through Bit 12 are individually tested by the comparator. After 12 trials, and 13 clock pulse edges have occurred, the Successive Approximation Register (SAR) output is a digital representation of the analog input. At this time, the Status output signal changes to indicate that conversion has been completed and output data is valid.

The ADC-00403 is available in both internal clock or external clock models. The internal clock model makes the clock signal available to the user on the Clock Output pin. In addition, the Clock Rate Control input pin may be used to make fine adjustments of the internal clock frequency. The ADC-00403 may be short cycled for less than 12 bit resolution with a resulting decrease in its conversion time.

Both parallel data and serial data are provided as digital outputs from the converter. For bipolar analog input signals the digital output data is coded in Complementary Two's Complement or Complementary Offset Binary. Both Bit 1 and Bit 1 complement ($\overline{B1}$) are provided as outputs, so either of these codes may be selected. For unipolar analog input signals, the digital output data is coded in Complementary Binary.

The ADC-00403 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are implemented with combination of the two precision scaling resistors and the precision bipolar offset resistor. Inherent offset and gain errors of the A/D converter may be trimmed to zero with the addition of potentiometers.

The ADC-00403 contains an internal precision +6.2 volt reference. This reference voltage is provided for the user at an output pin. In order to avoid affecting converter performance, care must be taken not to load the reference beyond its output capability.

To achieve the optimum performance available from the ADC-00403, it is recommended that decoupling capacitors be used on the supply lines. In addition, high frequency layout considerations should be kept in mind when designing a printed circuit board to accomodate the A/D converter. This includes minimum conductor lengths on signals, and a low impedance ground plane where possible.

TIMING DIAGRAM

A diagram of typical A/D converter timing is shown in Figure 2. A conversion is initiated by the application of a positive (50 nsec min) pulse to the Start Convert pin. A delayed (25 nsec min) clock must be applied to the Clock In pin for model ADC-00403. For model ADC-00404 the Clock Output appears after the falling edge of the Start Convert pulse. The rising edge of the clock causes the status signal to change to a "1", indicating that a conversion is in progress and parallel output data is not valid. Also in response to the clock rising edge, the MSB of the Successive Approximation Register (SAR) is reset to "0" and all other bits are set to "1". During clock period 1, the MSB trial takes place, and the MSB bit weight is compared to the analog input. The rising edge of clock pulse 2 causes the decision of the MSB trial to be stored, and simultaneously initiates the Bit 2 trial. In a successive manner, the rising edge of clock pulses 3 through 13 cause the storage of decisions on Bit 2 through Bit 12. The rising edge of clock pulse 13 causes the status signal to change to a "0", since the SAR now contains the valid 12 bit representation of the analog input. Parallel output data is valid during the interval that status signal is "0".

Serial Data is available as an output in non return to zero (NRZ) format. Data for each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically, Serial Data is shifted into an external 12 bit shift register, using the falling edges of the clock signal. The falling edge of clock pulse 13 would therefore shift Bit 12 into the register.

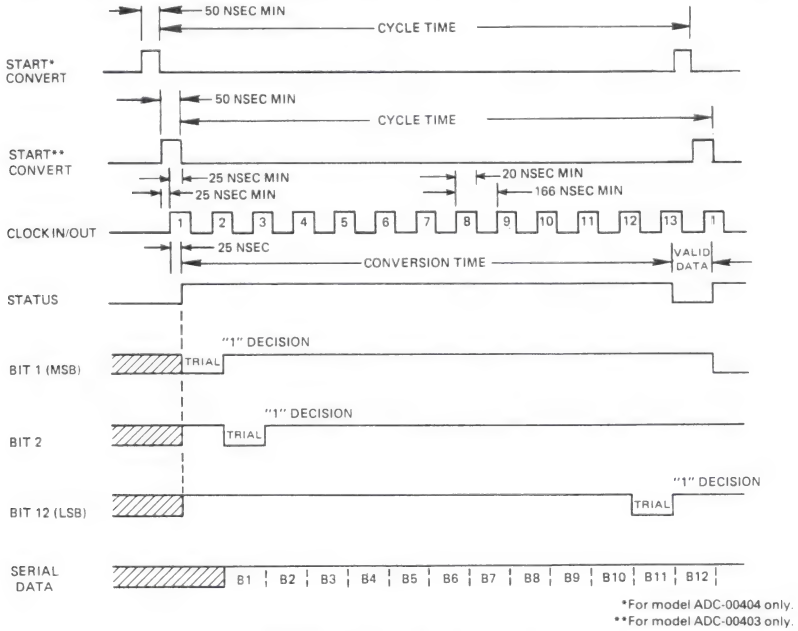
The minimum clock period allowed for rated performance of the ADC-00403 is 166 nanoseconds. This applies to both internal clock and external clock models. Conversion time is defined as the time during which the Status signal is a "1" and parallel output data is not valid. Cycle time, which is slightly longer than conversion time, is defined as the minimum time which must elapse between successive Start Convert pulses.

EXTERNAL CLOCK

The ADC-00403 is available in internal and external clock models. For external clock models the user must provide a clock signal to Clock Input (pin 19). Thirteen positive clock pulses are required to complete the conversion process. For rated A/D performance, the applied clock period must be 166 nanoseconds minimum. Figure 2 shows Clock In timing relationships. Best performance is achieved with a clock "high" duty cycle of between 12% and 33%. This sequence initiates conversions for both gated clock and continuous clock inputs. Care must be taken to comply with the minimum cycle time requirement between successive Start Convert pulses.

SHORT CYCLING AND CONTINUOUS CONVERSION

The ADC-00403 may be short cycled to fewer than 12 bits resolution, with a resulting decrease in conversion time. Figure 3 shows the required jumper connections and the resulting conversion times, with a 6 MHz clock, for 8 bit through 12 bit resolutions. For resolutions of less than 12 bits, it is possible to increase the clock frequency somewhat, since internal settling times are shorter. This may be accomplished by adjusting the Clock Rate Control voltage.



*For model ADC-00404 only.
**For model ADC-00403 only.

FIGURE 2. TIMING DIAGRAM

The ADC-00403 can be simply configured for continuous conversion operation when it is required. The falling edge of the Status (pin 20) signal is used to trigger a one shot. The one shot output, a 50 nsec minimum positive pulse, is connected to the Start Convert (pin 21) input to yield continuous conversion operation.

CLOCK RATE CONTROL

The Clock Rate Control line is made available in the internal clock model of the ADC-00404 to make small adjustments of the internal clock frequency. Figure 4 shows a typical circuit using a potentiometer to generate the Clock Rate Control voltage, and the resulting clock frequencies. For 12 bit operation, care must be taken to comply with the 166 nanosecond minimum clock period requirement. For short cycled operation, the Clock Rate Control voltage may be set greater than 5 volts, resulting in a clock frequency greater than 8 MHz.

PARALLEL DATA

Bit 1 through Bit 12 plus $\overline{\text{MSB}}$ are the parallel output data lines provided by the ADC-00403. Each signal can drive a minimum of 5 standard TTL loads. Parallel output data is valid during the time that the Status signal is a "0". If a strobe signal is required to read the parallel data into a register a "one-shot" can be triggered by the falling edge of the Status signal, or the falling edge of clock pulse 13 can be isolated by gating the Clock and Status signals together.

SERIAL DATA

Serial Data is provided by the ADC-00403 in non return to zero (NRZ) format with the MSB first. The Serial Data output line can drive a minimum of 2 standard TTL loads.

Each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically an external 12 bit shift register is used to store the serial data, after it has been shifted into the register using the falling edges of the clock signal. The LSB would be shifted into the register by the falling edge of clock pulse 13.

OUTPUT CODING

The ADC-00403 provides Complementary Binary coded output data for unipolar analog inputs, and either Complementary Offset Binary or Complementary Two's Complement coded output data for bipolar analog inputs. Figure 5 illustrates the output data for various analog inputs for each of the three code configurations. For bipolar analog inputs, the 2 choices of output code are available since both MSB and $\overline{\text{MSB}}$ signals are provided as outputs.

ANALOG INPUT RANGES

The ADC-00403 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are possible. Figure 6 shows these six choices of analog input range, along with the jumper connections required to implement each range. The chart also shows, for each input range, which pin is to be used for the input signal, and what impedance will be presented at that pin. Absolute maximum input voltage is also shown for each configuration.

RESOLUTION	CONNECT PIN 14 TO	CONVERSION TIME
8 BIT	PIN 4	1.3 μsec
9 BIT	PIN 3	1.5 μsec
10 BIT	PIN 2	1.6 μsec
11 BIT	PIN 1	1.8 μsec
12 BIT	NC	2.0 μsec

FIGURE 3. SHORT CYCLE OPERATION

PIN 17 VOLTAGE	APPROXIMATE CLOCK RATE
+5V	8 MHz
0V	6 MHz

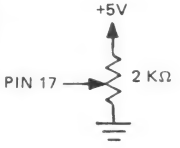


FIGURE 4. CLOCK RATE CONTROL

SCALE	BIPOLAR		UNIPOLAR
	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT	COMPLEMENTARY BINARY
+FS-1 LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000
+3/4 FS	0001 1111 1111	1001 1111 1111	0011 1111 1111
+1/2 FS	0011 1111 1111	1011 1111 1111	0111 1111 1111
+1 LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110
0	0111 1111 1111	1111 1111 1111	1111 1111 1111
− 1 LSB	1000 0000 0000	0000 0000 0000	
−1/2 FS	1011 1111 1111	0011 1111 1111	
−3/4 FS	1101 1111 1111	0101 1111 1111	
−FS	1111 1111 1111	0111 1111 1111	

FIGURE 5. OUTPUT CODING

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE (OHMS)	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±3.75V	0.625 K	PIN 24	PIN 23 TO PIN 22 PIN 25 TO PIN 22
0 to +5V	+7.5V	0.625 K	PIN 24	PIN 23 TO PIN 26 PIN 25 TO PIN 22
±5V	±7.5V	1.25K	PIN 24	PIN 23 TO PIN 22
0 to +10V	+15V	1.25 K	PIN 24	PIN 23 TO PIN 26
±10V	±15V	2.5K	PIN 25	PIN 23 TO PIN 22
0 to +20V	30V	2.5 K	PIN 25	PIN 23 TO PIN 26

FIGURE 6. ANALOG INPUT RANGE

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00403 are factory trimmed to be less than the values listed in the specification table. The converter is externally trimmable to zero gain and zero offset error, providing the user with flexibility for applications requiring maximum performance.

Figure 7 illustrates the external trim potentiometer circuit connections required to adjust the gain and offset errors of the ADC-00403 to zero. Multi-turn trimpots, with temperature coefficient of less than 100 ppm/°C, are recommended for best performance.

If gain adjust pot is not used, connect Gain Adjust pin 27 to Analog Gnd pin 26 to minimize noise.

INTERNAL REFERENCE

The ADC-00403 contains a +6.3 volt precision internal reference, which is made available for external use. A maximum output current of 5 mA will be provided by the internal reference, while maintaining rated performance. If this load is exceeded, gain and linearity error will increase. Damage will result from excessive loading.

LAYOUT PRECAUTIONS

To achieve the optimum performance of the ADC-00403, care must be taken in the printed circuit layout. Analog input lines and digital output lines should be separated from each other, and made as short as possible. To minimize ground noise, analog and digital grounds should be connected together in close proximity to the unit. A low impedance ground plane under the converter will yield the best results.

POWER SUPPLY DECOUPLING

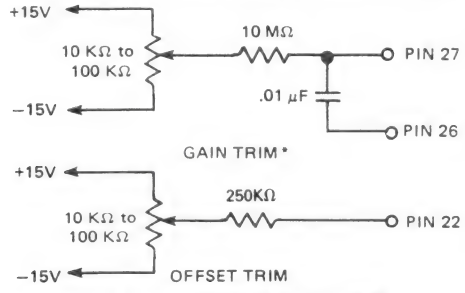
Capacitive decoupling of all power supplies is required to minimize noise. Figure 8 shows the recommended power supply decoupling configuration. Tantalum or electrolytic capacitors of 1 μF or greater are used for low frequency decoupling. Ceramic capacitors of 0.01 μF or greater are used for high frequency decoupling. For best results, all capacitors should be placed as close to the unit as possible.

ACCURACY TESTING

Testing of the accuracy of the ADC-00403 consists of measurement of its gain, offset and linearity errors. Figure 9 shows a simple test circuit for making these measurements. A precision DC voltage source is used to provide the analog input signal, and the digital outputs are monitored by a string of light emitting diodes (LED).

The offset error can be measured by adjusting the DC voltage source until the LEDs indicate the zero code transition. The difference between the voltage input and zero volts is the offset error. After the offset error has been measured, the circuit shown in Figure 7 should be used to trim the offset error to zero.

With the offset error trimmed to zero, the gain error can be measured by adjusting the DC voltage source until the LEDs indicate the full scale code transition. The difference between the input voltage and the theoretical full scale input is the gain error. After the gain error has been measured, the circuit shown in Figure 7 should be used to trim the gain error to zero.



*If gain trim is not used, connect pin 27 to pin 26.

FIGURE 7. OFFSET AND GAIN TRIM

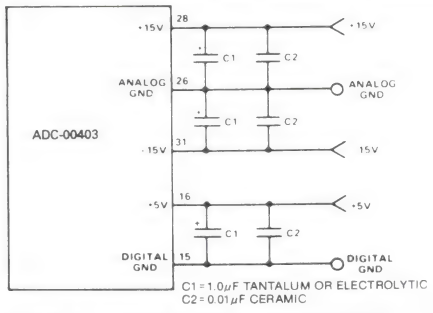


FIGURE 8. POWER SUPPLY DECOUPLING

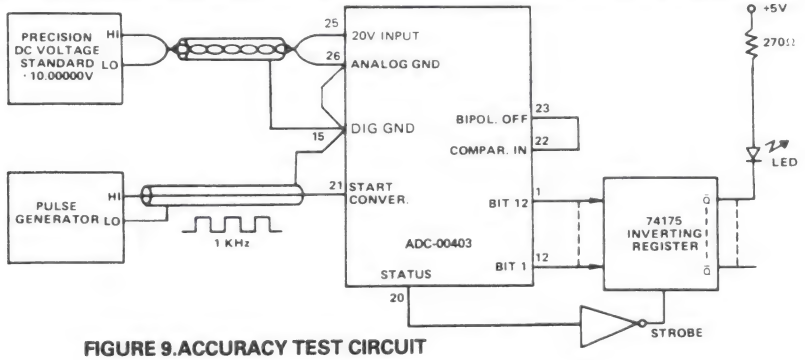


FIGURE 9.ACCURACY TEST CIRCUIT

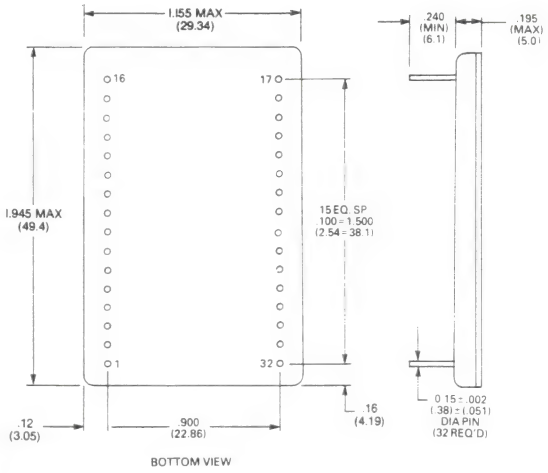
With the offset and gain errors trimmed to zero, any remaining error is a linearity error. Linearity error should be measured at the code transitions corresponding to each individual bit weight, and also at each of the major carry code transitions which occur at one count less than the individual bit weights.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 12 (LSB)	17	NC*/Clk Rate Control**
2	Bit 11	18	Ref. Out (+6.2V)
3	Bit 10	19	Clock In*/Clock Out**
4	Bit 9	20	Status
5	Bit 8	21	Start Convert
6	Bit 7	22	Comparator In
7	Bit 6	23	Bipolar Offset
8	Bit 5	24	10V Range In
9	Bit 4	25	20V Range In
10	Bit 3	26	Analog Gnd
11	Bit 2	27	Gain Adjust
12	Bit 1 (MSB)	28	+15V Supply
13	$\overline{\text{Bit 1 (MSB)}}$	29	NC
14	Short Cycle	30	NC
15	Dig. Gnd	31	−15V Supply
16	+5 V Supply	32	Serial Out

*Function for ADC-00403 model only.
**Function for ADC-00404 model only.

MECHANICAL OUTLINE
32 PIN TRIPLE DIP



NOTES:
1. Dimensions shown are in inches, (millimeters)
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply only at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

ORDERING INFORMATION

ADC-00403-103

Linearity Grade:
3 = 12 bit (0.012% FSR)

Reliability Grade:
0 = Standard DDC procedures.
1 = 883B Processing.
2 = 883B Processing but without QCI testing.

Operating Temperature Range (Case)
1 = −55°C to +125°C
2 = −25°C to +85°C

Clock Option
3 = External Clock
4 = Internal Clock

SECTION B
DIGITAL TO ANALOG (D/A) CONVERTERS

PRODUCT SUMMARY TABLE

MODEL	RESOLUTION	F.S. SETTLING TIME		LINEARITY ERROR	PACKAGE	OPERATING TEMP. RANGE	POWER DISSIPATION	DESCRIPTION/ FEATURES	PAGE
		VOLTAGE	CURRENT						
ADH-030 II	12 Bit	—	35 nsec	±1/2LSB	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.2"	-55°C to +125°C	1.2 W	Low glitch energy 2.5mA • nsec . One monolithic active component. Very fast settling. ECL	B-4
DAC-02306 **DAC-02307**	14 Bit	— 350ns	50 nsec —	±0.01% FSR	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.2"	-55°C to +125°C	1.8W	14 bit latched DAC with fast settling voltage output. Pin programmable output voltage, wtih trimmable gain and offset.	B-10
DAC-02310 **DAC-02311**	14 Bit	1.5µsec	—	±0.01% FSR	32 Pin TDIP 1.16 x 1.75 x 0.21" 32 Pin Flatpack 1.10 x 1.8 x 0.18"	-55°C to +125°C	1.7W	14 bit deglitched D/A converter with 10MHz update rate, pin programmable output ranges, and 50mV • nsec differential glitch energy.	B-14
DAC-02315 **DGL-02316**	12 Bit	35ns	—	±0.01% FSR	24 Pin DDIP Hybrids 1.4 x 0.8 x 0.2"	-55°C to +125°C	3.3W	Deglitching D/A converter with 35 MHz update. 14mVpp glitch and 38ns glitch duration.	B-18
* **DAC-02320**	12 Bit	200 nsec	—	±0.01% FSR	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.2"	-55°C to +125°C	2.2W	12 bit deglitched D/A converter with 15MHz update rate, pin programmable output ranges	B-28

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

* New Product

BACKGROUND INFORMATION

INTRODUCTION

DDC's digital to analog converters are divided into two categories. The Fixed Reference D/A Converters are calibrated with a fixed internal reference voltage, and provide a current output and/or voltage output determined by the digital input word. The Multiplying D/A converters listed in this catalog will accept an external reference, and provide a voltage output equal to the product of the reference voltage and the fraction represented by the digital word. In addition to high speed and high resolution, DDC offers fixed reference D/A converters with very low glitch and pin-programmable current and/or voltage ranges. One converter includes a track/hold deglitch and cable driver, and one has a strobed input register. The 13 to 15 bit multiplying D/A converters all have 4 quadrant operation and an output common-mode rejection capability, and will provide full rated accuracy from DC to 400 Hz.

All of DDC's D/A converters include a resistance network and switches which together provide a current output. The simplest concept of a D/A converter is shown in Figure 1. The resistance network produces a series of binary weighted currents. These are connected to the output by switches controlled by the digital input. The summed current is available directly as an output current I_{OUT} or is transformed by an op-amp into a voltage output V_{OUT}. The chief requirements for the converter are linearity (which depends on the bit current ratios), scale factor accuracy and low offset drift.

A difficulty with the arrangement in Figure 1 is that turning the bit currents off and on changes voltages in the resistance network and so may affect stability. This problem is eliminated by an arrangement such as shown in Figure 2 where the resistor currents are constant because they are switched either to actual ground or to the virtual ground of an op-amp.

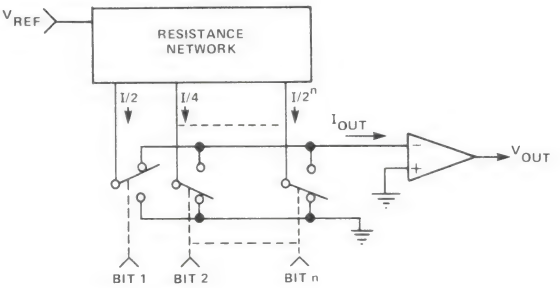


FIGURE 2. ARRANGEMENT WITH CONSTANT RESISTOR CURRENTS

There are many other possible types of resistance networks and switching arrangements. Currents, for instance, can be switched as equal currents before they are given binary weighting by the network, as shown in Figure 3. The method chosen for a particular D/A converter depends on the best compromise of characteristics and cost.

For a multiplying D/A converter, the output current must remain proportional to the reference voltage without saturation effects over an acceptable range of bipolar input voltages (usually ±10V) and frequencies. Otherwise, multiplying and fixed reference D/A converters are quite similiar in basic design concepts.

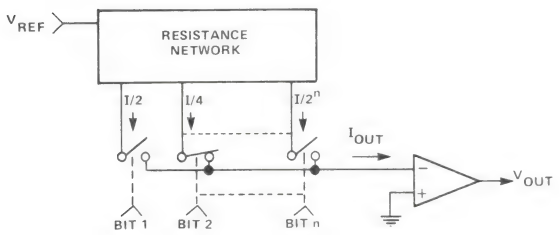


FIGURE 1. BASIC D/A DIAGRAM

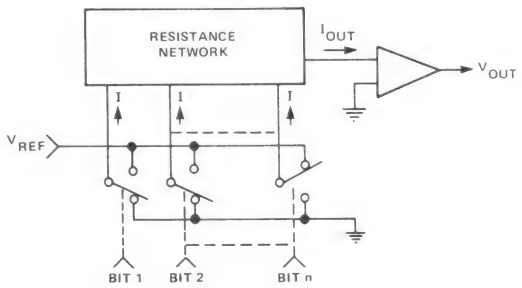


FIGURE 3. ANOTHER D/A ARRANGEMENT

TRANSFER CHARACTERISTICS AND ACCURACY

The transfer characteristics of a D/A converter will be discussed in terms of a 3 bit converter with straight binary and offset binary coding. The difference between these two codings is just an analog offset equal to one half of full scale. This offset is generally pin programmable in converters which offer both unipolar and bipolar coding.

For a D/A converter, analog output values such as 1 LSB, 2 LSB etc. should coincide with the input bit codes. This is shown by the ideal transfer characteristic for a 3 bit D/A converter illustrated in Figure 4. For straight binary coding, for instance, the 0 LSB output level coincides with 000 and the 1 LSB level coincides with 001. Intermediate values of analog output should not exist except as brief transitions while a code change occurs.

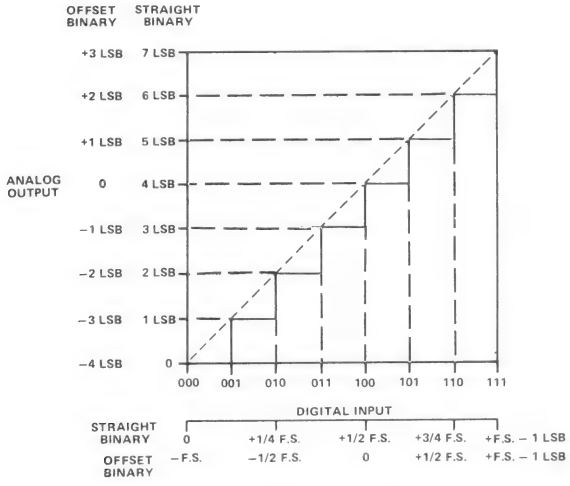


FIGURE 4. IDEAL TRANSFER CHARACTERISTIC FOR A 3 BIT D/A CONVERTER

It can be seen from Figure 4 that the largest analog output obtained in both straight and offset binary coding is F.S. − 1 LSB. In some converters with offset binary coding the output is offset by 1 LSB so that the largest positive value is F.S. and the largest negative value is −F.S. + 1 LSB. The bit table equivalent to the transfer characteristic in Figure 4 is shown in Figure 5.

The accuracy of a D/A converter is measured by determining the analog output for each input digital code. The total error is the sum of the offset error, the gain error, and the linearity error.

For a unipolar converter the offset is usually specified to be at the code for zero analog output, but it could be designated by the manufacturer to be at the code at either end of the range. For a bipolar converter, the offset could also be assigned to the code for zero output near the center of the range. The offset error is the difference between the measured and the theoretical output value at the code designated for offset.

ANALOG OUTPUT		DIGITAL CODE		
Unipolar Straight Binary	Bipolar Offset Binary	(MSB) Bit 1	Bit 2	(LSB) Bit 3
+ F.S. − 1 LSB	+ F.S. − LSB	1	1	1
+ 3/4 F.S.	+ 1/2 LSB	1	1	0
+ 1/2 F.S. + 1/2 LSB	+ 1 LSB	1	0	1
+ 1/2 F.S.	0	1	0	0
+ 1/2 F.S. − 1 LSB	− LSB	0	1	1
+ 1/4 F.S.	− 1/2 F.S.	0	1	0
+ 1 LSB	− F.S. + 1 LSB	0	0	1
0	− F.S.	0	0	0

FIGURE 5. BIT TABLE FOR 3-BIT D/A CONVERTER

The gain error is measured at the codes at opposite ends of the range. The gain is equal to the difference between the measured outputs at these two codes (keeping negative signs for negative output), divided by the theoretical output span between them. For the 3 bit converter just discussed, the input span is F.S. − 1 LSB for unipolar coding, and 1 F.S. − 1 LSB for bipolar coding.

The linearity is obtained by determining the difference between the measured and theoretical output at all other codes. Before substracting the theoretical value, the measured value at each point must be corrected by first substracting the offset error and then multiplying by the gain correction. The calculations are greatly simplified if the converter offset and gain errors are both trimmed to zero before linearity is measured.

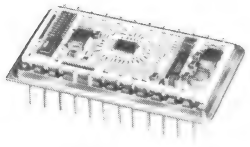
Monotonicity is usually also required. If the converter is monotonic, the analog output will never decrease if the digital code increases, and will never increase if the digital code decreases.

See page N-19 for a list of Application Notes available from DDC.

DDC
ILC DATA DEVICE CORPORATION

MONOBRID® ADH-030 II

12 BIT 35 NSEC HYBRID D/A CONVERTER
High Reliability; One Monolithic Active Component



FEATURES

- *FAST: 35 NSEC SETTLING*
- *HIGH RELIABILITY: 3,000,000 HOUR MTBF*
- *LOW GLITCH: 50 MV • NSEC*
- *–55° to +125°C OPERATING TEMPERATURE*
- *HERMETICALLY SEALED 24 DDIP PACKAGE*

DESCRIPTION

The Monobrid ADH-030 II is a 12 bit 35 nanosecond hybrid D/A converter packaged in a hermetically sealed 24 DDIP. It pin for pin replaces an earlier multiple component design with a single monolithic integrated circuit. Thin film resistors and decoupling capacitors complete the (monolithic-hybrid) Monobrid. Featuring 3,000,000 hour MTBF, 50 mV • nsec glitch, and -55°C to +125°C operating temperature range, the Monobrid ADH-030 II is offered with MIL-STD-883B screening.

APPLICATIONS

With its small size, wide operating temperature range and hermetically sealed package, the Monobrid ADH-030 II is ideal for the most demanding military and industrial requirements. Its high speed and low glitch are well suited for numerous CRT display applications, including TV and radar video reconstruction, and X-Y deflection positioning. Additional applications include digitally controlled frequency agile oscillators and high speed A/D converters.

Note: Monobrid® is a registered trademark of ILC Data Device Corp.

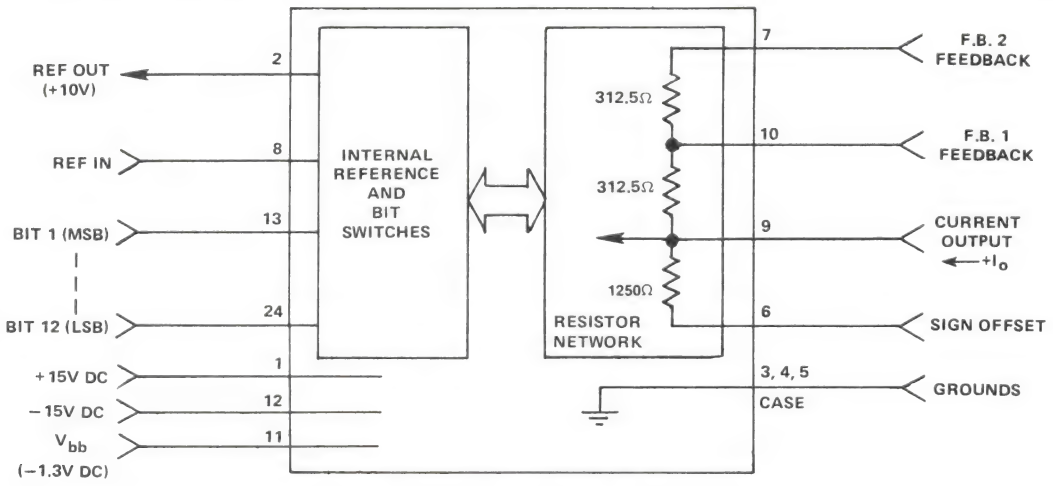


FIGURE 1. ADH-030 II BLOCK DIAGRAM

TABLE 1. ADH-030 II SPECIFICATIONS

Typical values at 25°C and at nominal power supply voltages unless otherwise noted.

PARAMETER	UNIT	VALUE	
		10 BIT LIN	12 BIT LIN
RESOLUTION	Bits	12	12
ACCURACY			
Linearity Error (Max)	% F.S. Range	±0.05	±0.0125
Linearity Tempco*	ppm/°C	±5	±5
Gain Accuracy	% F.S. Range	±0.1	±0.1
Gain Tempco*	ppm/°C	50	25
Zero Offset			
Unipolar Offset (Max)	μA	4	1
Bipolar Offset (Max)	μA	8	4
Offset Tempco	ppm/°C	20	10
Monotonic to	bits	10	12
DYNAMIC CHARACTERISTICS			
Update Rate	MHz	50 min	
Settling Time to 0.01% of Final Value			
For F.S. Input Change	ns	35 typ;, 50 max	
For 1 LSB Change (From 01..11 to 10..00)	ns	20 typ	
Internal Skewing Time	ps	400 typ; 800 max	
Output Time Constant	ns	1.3 typ into 100Ω load	
Glitch Energy	LSB·nsec	200	
	mV·nsec	50 into 100Ω	
DIGITAL INPUT (VALUES GIVEN FOR V_{bb} = −1.30V DC)			
Input Coding		Positive logic. Complementary Binary gives unipolar ouput. Complementary Offset Binary or Complementary Two's Complement (if MBS is provided) give bipolar output.	
		Logic "1"	Logic "0"
Digital Voltage Level	V	−0.81 to −0.96	−1.65 to −1.85
Max Voltage Without Damage	V	0	−6
Current Loading	μA	100 max	1 max
REFERENCE AND SIGN OFFSET		10 BIT LIN	12 BIT LIN
Internal +10.000V Reference Accuracy	% of Ref	±0.2 max	±0.1 max
Max Current Output**	mA	15 max	
External Ref. Requirements (Optional)			
Voltage Range	V	+10±10%	
Current Requirements			
For Ref Input	mA	4.0 typ; 4.4 max	
For Sign Offset	mA	8.0 typ; 8.8 max	
Ref. Input Impedance	KΩ	2.5±1%	
Sign Offset Impedance	KΩ	1.25±1%	
OUTPUT (CURRENT TYPE)			
Unipolar Current	mA	0 to −16	
Bipolar Current	mA	±8	
Compliance	V	−0.5 to +5.0	
Voltage Output Ranges With External Amplifier	V	Full accuracy; 0 to 5 0 to 2.5, ±5, ±2.5, ±1.25 Reduced Accuracy: 0 to 10	
Output Capacitance	pF	20 typ	

TABLE 1. ADH-030 II SPECIFICATIONS (Cont'd)

PARAMETER	UNIT	VALUE		
POWER SUPPLIES				
Voltage	V	+15	−15	−1.3 (V_{bb})
Regulation for Full Accuracy	%	±2	±2	±3
Absolute Max Limit	V	+18	−18	−4
Current Typ	mA	30	57	0.5
Max	mA	35	60	2
TEMPERATURE RANGE (CASE)				
Operating				
−1 Option	°C	−55 to +125		
−3 Option	°C	0 to +70		
Storage	°C	−55 to +125		
THERMAL IMPEDANCE* **				
Junction to Air, θ_{JA}	°C/Watt	20 max		
Junction to Case, θ_{JC}	°C/Watt	2 max		
PHYSICAL				
Package		24 Pin, Double DIP		
Size	inches	1.4 x 0.8 x 0.2		
	(mm)	(36 x 20.3 x 5.1)		
Weight	oz	0.4 (11.3 g) typ		

*Lower Tempco values are available — consult factory.
**If reference is used by external circuits only, load must be 5 mA minimum.
***Max junction temperature is 150°C.
Heat passes through header (case bottom).

TECHNICAL INFORMATION

INTRODUCTION

The ADH-030 II generates analog output currents which are digitally controlled, binary weighted, discrete fractions of a reference voltage. The reference voltage is fixed so that the output current has a single value for each digital input code. A reference is generated internally, as indicated in the block diagram Figure 1, but a properly regulated external reference voltage may be substituted. The analog output is controlled by a ladder network of thin film precision resistors, controlled by bipolar transistor switches turned on and off in accordance with the digital input code.

Figure 2 is an internal schematic for the ADH-030 II showing the 8 mA current generators, the R-2R ladder network, and the external connections. Feedback resistors are provided to assist in converting the current output into a voltage output with an external amplifier, as discussed below. The sign offset (pin 6) is used for bipolar operation, as discussed below. Note that the current direction is defined as positive for currents entering the output, pin 9.

The ADH-030 II accepts complementary binary or complementary offset binary input coding. The MECL/ECL input logic requirements are detailed in the specifications table. Figure 3 shows the current outputs obtained for various bit weights. The values for Full Scale (F.S.) and 1 LSB are as follows:

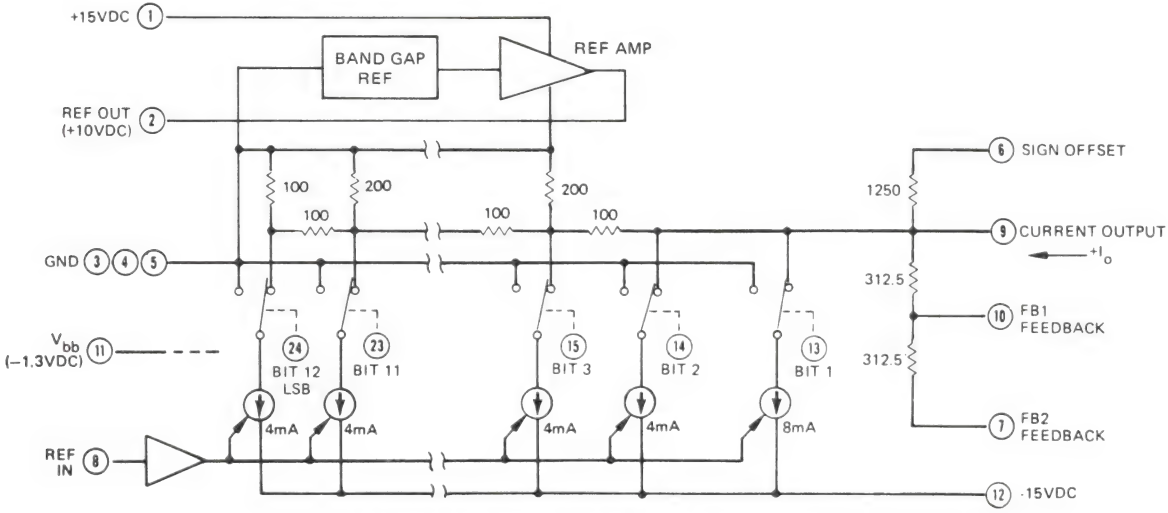


FIGURE 2. ADH-030II INTERNAL SCHEMATIC

ANALOG OUTPUT CURRENT*		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12
+F.S. –1 LSB	+F.S. –1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+¾ F.S.	+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+½ F.S. +1 LSB	+1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+½ F.S. –1 LSB	–1 LSB	1	0	0	0	0	0	0	0	0	0	0	0
¼ F.S.	–½ F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+1 LSB	–F.S. +1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	–F.S.	1	1	1	1	1	1	1	1	1	1	1	1

*Current direction defined as positive for currents entering the output.

FIGURE 3. BIT WEIGHT TABLE

RANGE	FULL SCALE	1 LSB
±8 mA	8.00000 mA	0.00391 mA
0 to –16 mA	16.00000 mA	0.00391 mA
±1.25*	1.25000V	0.00061V
±2.5*	2.50000V	0.00122V
±5V*	5.00000V	0.00244V
0 to +2.5V*	2.50000V	0.00061V
0 to +5V*	5.00000V	0.00122V
0 to +10V*	10.00000V	0.00244V

*With external output amplifier

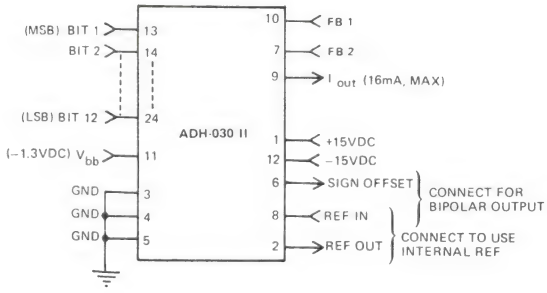


FIGURE 4. INPUT/OUTPUT CONNECTIONS FOR NORMAL OPERATION

NORMAL OPERATION

1. Normal Operation/Current Type Output

The input/output connections for normal operation of the ADH-030 II are shown in Figure 4.

For unipolar current output, the maximum output voltage is limited by the — 16 mA current capability to

$$V_{max} = -0.016R, \frac{1}{R} = \frac{1}{200} + \frac{1}{RL}$$

where RL is the load resistance and 200Ω is the resistance of the ladder network. The compliance limits V_{max} to −0.5V, so the load resistance should be 37Ω or less.

For bipolar operation the sign offset must be connected to the REF IN. The 1250Ω sign offset resistor (see Figure 2) is in parallel with the 200Ω ladder network, reducing the internal impedance at the output to 172.4Ω. The maximum output voltage is limited by the ±8mA current to

$$V_{max} = \pm 0.008R, \frac{1}{R} = \frac{1}{172.4} + \frac{1}{RL}$$

Since the compliance is −.5 V to +5 V, the load resistance should be 98Ω or less.

2. Normal Operation/Voltage Type Output

The ADH-030 II provides up to −0.5V to +5.0V compliance, so external circuitry must be added if a larger voltage swing is required.

Figure 5 shows an optional circuit for converting the ADH-030 II current output to a voltage type output. The voltage range is determined by connections to the feedback pins FB1 and FB2 on the ADH-030 II. Adding a jumper between pins 6 and 8 provides offset for bipolar operation. The following table shows jumper and feedback connections for all voltage ranges.

VOLTAGE RANGE	JUMPER CONNECTIONS	FEEDBACK CONNECTIONS
±1.25V	Sign to Ref In, FB2 to current out	FB1
±2.5V	Sign to Ref In	FB1
±5V	Sign to Ref In	FB2
0 to +2.5V	FB2 to current out	FB1
0 to +5V	None	FB1
Reduced Accuracy:		
0 to +10V	None	FB2

Note that on the 0 to +10 voltage range, the overall accuracy of the ADH-030 II is reduced to 0.2% F.S. range for all linearity grades.

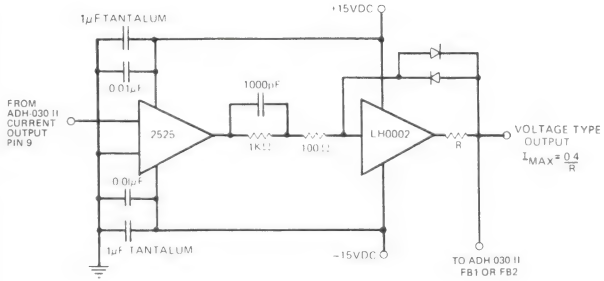


FIGURE 5. EXTERNAL CIRCUIT FOR VOLTAGE TYPE OUTPUT

3. Trimmed Operation

Without external trimming, the output accuracy of the ADH-030 II is affected by the gain accuracy and zero offset error listed in the specifications. Using external trim resistors the gain and offset errors can be trimmed to zero so that the overall accuracy is equal to the linearity.

Figure 6 shows input/output connections for trimmed operation. The zero offset adjustment range is approximately ±20 LSB. The gain adjustment is provided by a resistor which replaces the direct connection between REF OUT and REF IN. The gain adjustment range is 3% in the direction of *decrease* only. To provide for adjustments in the opposite direction, the gain must be offset. This can be accomplished in conjunction with the voltage output circuit of Figure 5 by inserting a 10 or 5Ω resistor in the feedback path, as indicated at pins 7 and 10 in Figure 6.

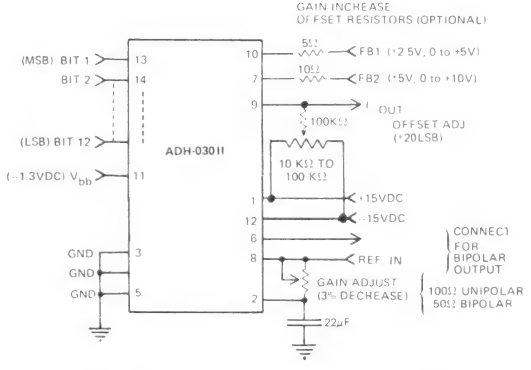


FIGURE 6. INPUT/OUTPUT CONNECTIONS FOR TRIMMED OPERATION

LINEARITY AND ACCURACY TESTS

Accuracy may be tested as follows: Connect pins 2, 6, and 8 together. Install the voltage output circuit of Figure 5 with direct feedback to FB2 (±5.0V output). The table in Figure 3 can be used to calculate the appropriate bit weights. A voltmeter with ±0.001V accuracy is required to measure the output. Unless a computer program is available to analyze the data, the most convenient test procedure is as follows:

(1) Measure the offset at the code 4 zero voltage.

(2) Install offset trim resistors and trim the offset error to zero. Determine the gain by measuring the output at both the +F.S. −1 LSB and −F.S. The gain is the sum of the magnitudes of the two end point voltages divided by 2 F.S. −1 LSB = 9.99756V.

(3) Install gain trim resistors and trim the gain to unity. Measure the output at all other codes to determine the linearity error.

The measured errors shall all be within the limits listed in the specifications table.

DYNAMIC CHARACTERISTICS

Skew is the difference in delay between individual bit transitions. When data changes, internal or external differences in delays between 0-1 and 1-0 transitions can cause the output to swing to intermediate states. For instance, if the input changes from 100 . . . 0 to 011 . . . 1 and the MSB changes before the lower order bits change, the output will swing to an intermediate state of 00 . . . 0. Internal skew is very low (400 ps typical) in the ADH-030 II because current mode switching is utilized. The MECL/ECL logic required by the digital input has inherently low skew properties, but to eliminate the last nanoseconds of skew it is necessary to clock the input with a register and match external circuit delays and line length differences. To maintain minimum skew with variations in temperature and power supplies, it is recommended that ADH-030 II pin 11 be connected to the V_{bb} output pin of an ECL logic circuit such as the MC10115.

Glitch energy is only 50 mV • nsec typ. Figure 7 shows glitch shape at major carry from 01 . . . 11 to 10 . . . 00 when the output is terminated by a 5 MHz filter and a 100 ohm resistor.

Settling time may be tested using the circuit shown in Figure 8. For a maximum output swing between −0.5V and +0.5V, the output will settle to 0.01% of final value within 50 ns (35 ns typical). For a swing of 1 LSB, the settling time depends on the skew and resulting glitch. For a 1 LSB change at major carry from 01 . . . 11 to 10 . . . 00, the settling time is 20 ns typical.

Ringing caused by long lead lengths or unterminated transmission line effects in the bit drives may lead to increased settling time or cause oscillation. If the lead length can not be shortened, the effect may be reduced or eliminated by placing RF beads on every other digital input lead.

REFERENCE

The ADH-030 II has an internal reference supply and is factory calibrated with this supply. Fixed external references of +10VDC ±10% can be accommodated and the output current will be linearity proportional to the reference voltage over this range.

RELIABILITY

The use of a single monolithic I.C. and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

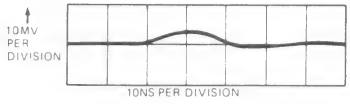


FIGURE 7. TYPICAL GLITCH SHAPE FOR 1 LSB CHANGE AT MAJOR CARRY (INTO 100Ω LOAD)

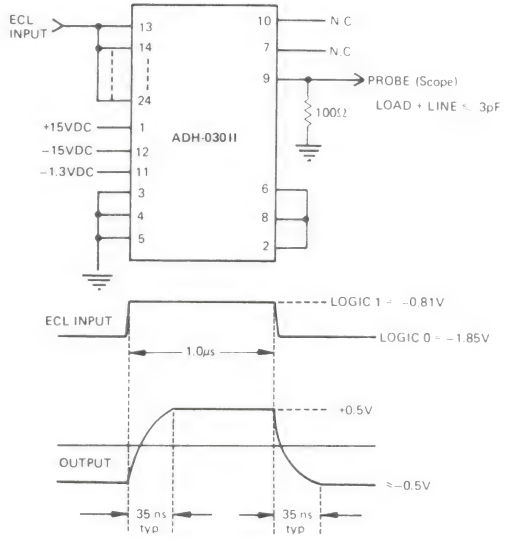


FIGURE 8. SETTLING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

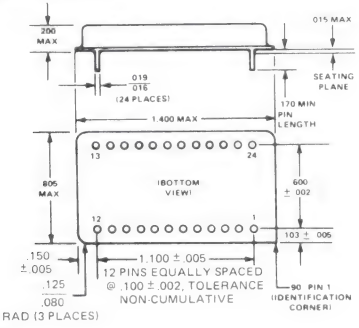
B

PIN CONNECTION TABLE

PIN No.	FUNCTION	PIN No.	FUNCTION
1	+15VDC	13	Bit 1 (MSB)
2	Ref. Out	14	Bit 2
3	Gnd*	15	Bit 3
4	Gnd*	16	Bit 4
5	Gnd*	17	Bit 5
6	Sign Offset	18	Bit 6
7	Feedback 2	19	Bit 7
8	Ref. In	20	Bit 8
9	Output	21	Bit 9
10	Feedback 1	22	Bit 10
11	$-1.3VDC = V_{bb}$	23	Bit 11
12	−15VDC	24	Bit 12 (LSB)

*All grounds are tied to the case.

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

ORDERING INFORMATION

ADH-030 II–12–1–883B

Reliability Grade:
- 883B = Fully compliant with MIL-STD-883
- B = Screened to MIL-STD-883 but without QCI testing.
- Blank = Standard DDC procedures.

Operating Temperature Range (Case)
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

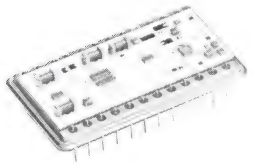
Linearity:
- 10 = ±.05%
- 12 = ±.0125%

E

DDC
ILC DATA DEVICE CORPORATION

DAC-02306 AND DAC-02307

14 BIT LATCHED D/A CONVERTER
Fast Settling Times: 50 ns Current Output 350 ns Voltage Output



DESCRIPTION

The DAC-02306 and DAC-02307 family is one of the fastest D/A converters available. Both units offer transparent input latches. The voltage output device settles to within 1 LSB of final value for a full scale step change in 350 nsec. Settling time for the current output device is 50 ns.

The DAC-02307 offers pin programmable output voltages of ±2.5V, ±5V, or ±10V at 10mA and the DAC-02306 provides a ±2mA current output. Linearity is ±0.012% of full scale and gain accuracy is ±0.075% of full scale.

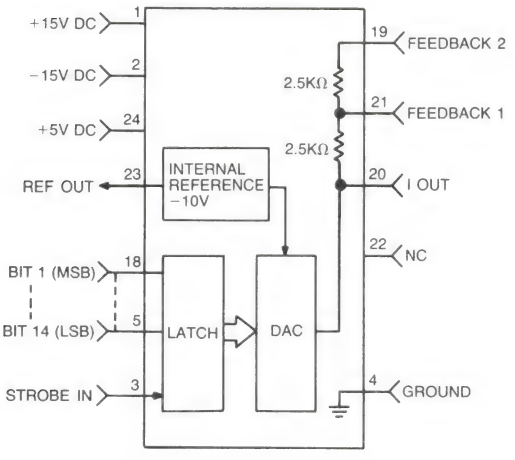
Both converters are calibrated with their own internal references, operate over a −55°C to +125°C temperature range, have trimmable gain and offset, and are available screened to MIL-STD-883.

Packaged in hermetically sealed 24 pin DDIPs, the DAC-02306 and DAC-02307 combine custom monolithic technology with thick and thin film fabrication techniques to provide both superior performance and high reliability.

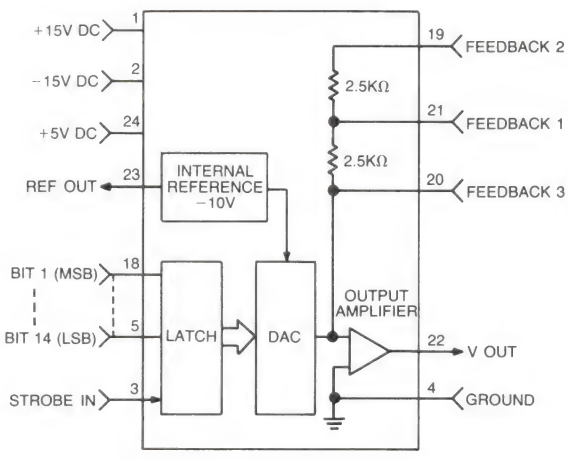
With their small size and a high MTBF, DDC's DAC-02306 and DAC-02307 are exceptionally well-suited for high reliability military and industrial applications. These converters offer outstanding performance in aircraft or shipboard displays, computer interfaces, sonar systems, and automated processing plants.

FEATURES

- *DAC-02306 HAS CURRENT OUTPUT: ±2mA*
- *DAC-02307 HAS VOLTAGE OUTPUT: ±2.5V, ±5V, AND ±10V AT 10mA*
- *TRANSPARENT INPUT LATCH*
- *WIDE OPERATING TEMPERATURE RANGE: −55°C TO +125°C*
- *MIL-STD-883 SCREENING AVAILABLE*



DAC-02306
CURRENT OUTPUT



DAC-02307
VOLTAGE OUTPUT

FIGURE 1. BLOCK DIAGRAM

TABLE 1. DAC-02306 AND DAC-02307 SPECIFICATIONS
Typical valves at +25° C and nominal power supply voltages unless otherwise noted.

PARAMETER	UNITS	VALUE	
		13 BIT LIN	12 BIT LIN
RESOLUTION	**Bits**	**14**	**14**
ACCURACY			
Linearity Error	% FS range	±0.006 max	±0.012 max
Linearity Tempco	ppm/°C	0.5 max	1 max
Gain Error	% FS range	±0.075 max	±0.150 max
Gain Tempco	ppm/°C	±25 max	±25 max
Current Output (DAC-02306)			
Current Offset	μA	4.0 max	8.0 max
Current Offset Tempco	μA/°C	0.04	0.04
Voltage Output (DAC-02307)			
Voltage Offset	mV	5.0 max	10.0 max
Voltage Offset Tempco	μV/°C	100	100
Monotonicity	bits	13	12
DYNAMIC CHARACTERISTICS			
Settling Time to ±0.01% FSR (for F.S. Input Change)			
Current Output	ns	50 typ for RL ≤ 100 Ohms	
Voltage Output			
±2.5V Scale	ns	300 max	
±5V Scale	ns	350 max	
±10V Scale	ns	350 max	
Output Capacitance (Current Output)	pF	20	
DIGITAL INPUTS			
Logic Type		TTL Compatible, parallel positive logic.	
Coding		Complementary Offset Binary.	
Loading		1 Standard HCT Load	
V_{IH} (High Level Input Voltage)	V	2.0 min	
V_{IL} (Low Level Input Voltage)	V	0.8 max	

TABLE 1. DAC-02306 AND DAC-02307 SPECIFICATIONS (Cont.)
Typical valves at +25° C and nominal power supply voltages unless otherwise noted.

PARAMETER	UNITS	VALUE		
		13 BIT LIN	12 BIT LIN	
RESOLUTION	**Bits**	**14**	**14**	
REFERENCE				
Internal Reference				
Voltage	V	−10±1%		
Current	mA	±3 max		
OUTPUT				
Voltage Output				
Voltage Ranges (Pin Programmable)	V	DAC-02307 ±2.5, ±5, or ±10		
Current Output	mA	10 max		
DC Impedance	Ohms	0.1		
Current Output		DAC-02306		
Current Range	mA	±2		
Output Impedance	Ohms	830		
Compliance	V	−1 to +1		
POWER SUPPLIES				
Voltage	V	+15	−15	+5
Voltage Tolerances	%	±2	±2	±5
Max Voltage w/o Damage	V	+18 max	−18 max	+7 max
Current Drain				
DAC-02306	mA typ/max	30/40	20/25	1.5/2.5
DAC-02307	mA typ/max	65/85	55/65	1.5/2.5
TEMPERATURE RANGES				
Operating (Case)				
-3 Option	°C	0 to +70		
-1 Option	°C	−55 to +125		
Storage	°C	−65 to +150		
PHYSICAL CHARACTERISTICS				
Size (24 Pin DDIP)	in. (cm)	0.8 x 1.4 x 0.2 (2.0 x 3.6 x 0.5)		
Weight	oz (gm)	0.38 (10.8)		

B

TECHNICAL INFORMATION

INTRODUCTION

Figure 1 illustrates the block diagrams for the DAC-02306 and DAC-02307. On the DAC-02306, there is no connection to pin 22 and the current output connection is pin 20. These converters generate current or voltage outputs which are binary weighted fractions of the reference voltage. The gain and offset are factory trimmed to very tight tolerances so that external trimming is not required. The outputs are bipolar with complementary offset binary coding as listed in table 2.

DAC-02307 VOLTAGE OUTPUT CONNECTIONS

Output connections for all three output voltage ranges are listed in table 3. The feedback connection should be made as close to the load as possible to minimize the effects of line and contact impedance. Output drive capacity is ±10mA for all voltage ranges.

DAC-02306 CURRENT OUTPUT CONNECTIONS

The current output of the DAC-02306 is taken directly from pin 20. The feedback pins 19 and 21 may be left floating or may be used as feedback from an external amplifier. Pin 22 is left unconnected for current output.

TABLE 2. COMPLEMENTARY OFFSET BINARY

OUTPUT	DIGITAL BIT INPUTS													
	MSB													LSB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
+F.S. −1 LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1	1
+1 LSB	0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
−1 LSB	1	0	0	0	0	0	0	0	0	0	0	0	0	0
−½ F.S.	1	0	1	1	1	1	1	1	1	1	1	1	1	1
−F.S. +1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1	0
−F.S.	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TABLE 3. DAC-02307 FEEDBACK CONNECTIONS

VOLTAGE RANGE	CONNECT V OUT (PIN 22) TO PIN	OTHER CONNECTIONS
±2.5V	21 (FB1)	19-20
±5V	21 (FB1)	—
±10V	19 (FB2)	—

INTERNAL REFERENCE

The DAC-02306 and DAC-02307 have an internal reference output and are factory calibrated with this internal reference. REF OUT is rated for ±3mA, max at −10V±1%.

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DAC-02306 and DAC-02307, high frequency layout considerations must be taken when laying out their printed circuit boards.

All analog conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedance as low as possible. Digital inputs and analog output must be kept separated from each other to minimize crosstalk. Circuits connected to the analog output and any FEEDBACK pins must be kept as close as possible to the hybrid.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each power supply for minimum noise operation. Each power supply should have a 1 uF or larger tantalum capacitor in parallel with a 0.01 uF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

CODING

Offset binary coding for the DAC-02306 and DAC-02307 is illustrated by the bit weight in table 4. Values for full scale voltage (F.S.) and 1 LSB are given.

TABLE 4. OFFSET BINARY CODING

RANGE	FULL SCALE	1 LSB
±2.5V	2.50000V	0.00031V
±5V	5.00000V	0.00061V
±10V	10.00000V	0.00122V
±2mA	2.00000mA	0.00024mA

TIMING

Upon application of a STROBE IN signal, the input registers are updated and DAC-02306 and DAC-02307 outputs settle to their new values. As shown in figure 2, the rising edge of STROBE IN latches the input date. Setup and hold times are also illustrated.

The input latches may be made transparent by keeping STROBE IN at a logic "1". Since STROBE IN has an internal pull-up resistor, it may be left unconnected for transparent latch operation.

EXTERNAL TRIMS

The gain and offset errors are trimmed at the factory to within the limits listed in the specifications table. With the optional trim adjustment circuits shown in Figures 3, 4 and 5, both errors can be trimmed to zero, making the overall accuracy equal to the linearity. The fixed resistors shown in Figures 3, 4 and 5 should be located close to the converter pins to reduce noise, and the potentiometers should have a tempco of 100 ppm/°C or less to minimize drift.

To trim the offset, apply the all zero's digital code. As shown in the bit table, Table 2, this corresponds to +F.S. −1 LSB for current and voltage output. Adjust the offset trim potentiometer for the proper current or voltage output value in each case.

After trimming the offset, apply the all one's code to trim the gain. This corresponds to −F.S. for current and voltage output. Adjust the output to this value with the gain potentiometer.

RELIABILITY

The use of custom monolithic technology, thick and thin film networks, as well as careful thermal design results in very high MTBF values. All DAC-02306 and DAC-02307 hybrids are built in accordance with MIL-STD-883.

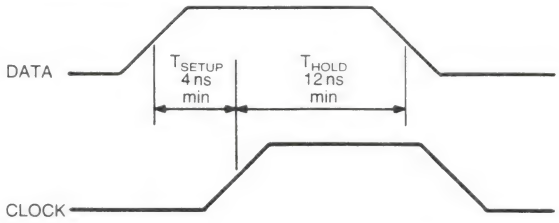


FIGURE 2. SETUP AND HOLD TIMING

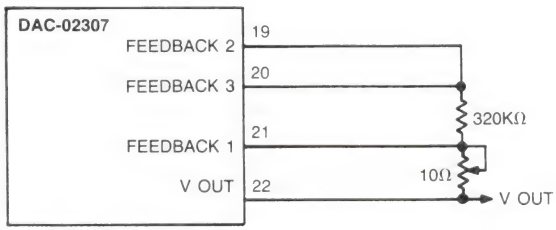
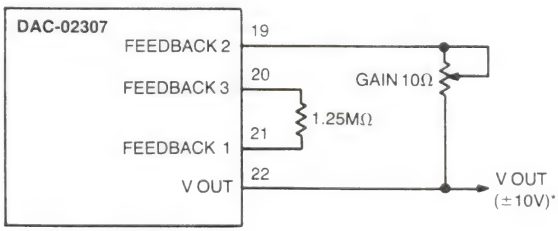


FIGURE 3. DAC-02307 GAIN ADJUST CIRCUIT FOR ±2.5V OUTPUT



*For ±5V output, refer to table 3.

FIGURE 4. DAC-02307 GAIN ADJUST CIRCUIT FOR ±5V AND ±10V OUTPUTS

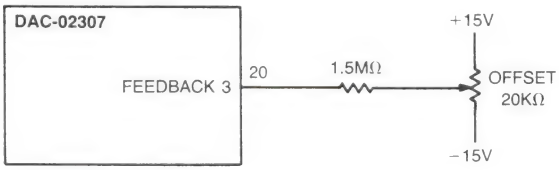


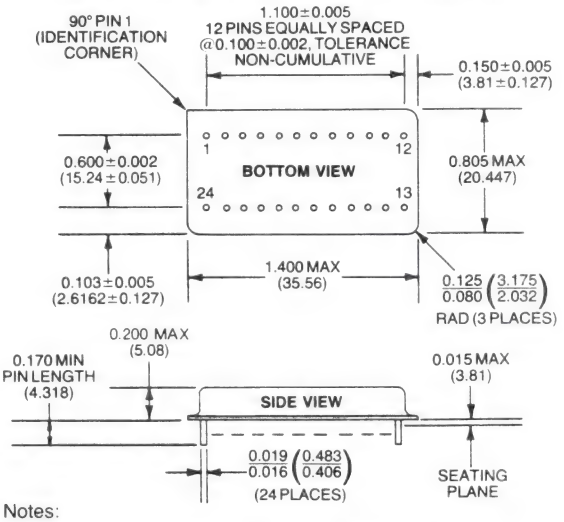
FIGURE 5. DAC-02307 OFFSET ADJUST CIRCUIT

TABLE 5. DAC-02306 PIN FUNCTIONS

PIN	FUNCTION
1	+15VDC Input
2	−15VDC Input
3	STROBE IN
4	Ground
5	Bit 14 (LSB)
6	Bit 13
7	Bit 12
8	Bit 11
9	Bit 10
10	Bit 9
11	Bit 8
12	Bit 7
13	Bit 6
14	Bit 5
15	Bit 4
16	Bit 3
17	Bit 2
18	Bit 1 (MSB)
19	FEEDBACK 2
20	I OUT
21	FEEDBACK 1
22	NC
23	REF OUT
24	+5VDC Input

TABLE 6. DAC-02307 PIN FUNCTIONS

PIN	FUNCTION
1	+15VDC Input
2	−15VDC Input
3	STROBE IN
4	Ground
5	Bit 14 (LSB)
6	Bit 13
7	Bit 12
8	Bit 11
9	Bit 10
10	Bit 9
11	Bit 8
12	Bit 7
13	Bit 6
14	Bit 5
15	Bit 4
16	Bit 3
17	Bit 2
18	Bit 1 (MSB)
19	FEEDBACK 2
20	FEEDBACK 3
21	FEEDBACK 1
22	V OUT
23	REF OUT
24	+5VDC Input



Notes:
(1.) Dimensions are shown in inches (millimeters).
(2.) Lead identification numbers are for reference only.
(3.) Lead spacing dimensions apply only at seating plane.
(4.) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
(5.) Case tied to analog ground.

FIGURE 6. DAC-02306/DAC-02307 MECHANICAL OUTLINE

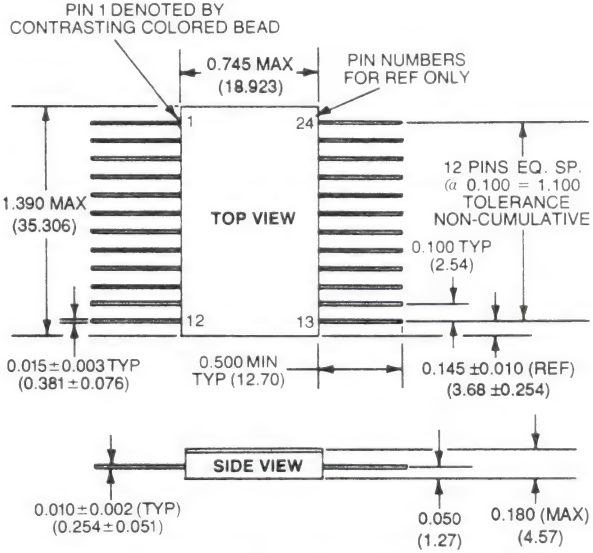


FIGURE 7. DAC-02308/DAC-02309 MECHANICAL OUTLINE

ORDERING INFORMATION

DAC-02306-1 1 3

- Linearity Grade:
  - 3 = 13 bit
  - 2 = 12 bit
- Reliability Grade:
  - 0 = Standard DDC procedures.
  - 1 = Fully compliant with MIL-STD 883.
  - 2 = Screened to MIL-STD-883 but without QCI testing.
- Temperature Range (Case):
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Model:
  - 6 = Current Output, DDIP*
  - 7 = Voltage Output, DDIP*
  - 8 = Current Output, Flatpack
  - 9 = Voltage Output, Flatpack

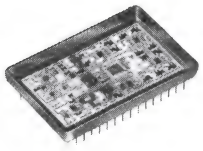
**Socket: Augat 324-AG2D or equivalent

F

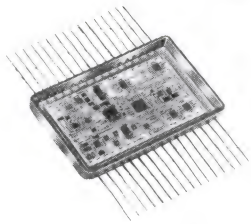
DDC
ILC DATA DEVICE CORPORATION

DAC-02310® AND DAC-02311®

14 BIT DEGLITCHED D/A CONVERTER
10MHz Update Rate; Voltage Output



DAC-02310



DAC-02311

DESCRIPTION:

The DAC-02310 is a 14 bit, 10 MHz update rate, deglitched hybrid D/A converter with a low impedance voltage output. Its input registers, precision DC voltage reference and track/hold deglitcher output provide the complete solution to low noise DAC requirements. Packaged in a small 32 pin TDIP hybrid, the DAC-02310 operates over the full -55° C to +125° C temperature range and is available with military processing.

DAC-02310 is available in linearity grades of 13 bits (±0.006%) and 12 bits (±0.012%). It can be pin programmed for 5 different output voltage ranges; and offset, gain, and pedestal errors can be trimmed to zero with external potentiometers.

With its 14 bit resolution, low glitch voltage output and small hermetic package, the DAC-02310 is ideal for the most demanding low noise DAC requirements. It is particularly well suited for applications such as vector-stroke CRT displays, waveform generators and automatic test equipment.

FEATURES

- *FULL FUNCTION: INCLUDES INPUT REGISTERS AND TRACK/HOLD DEGLITCHER OUTPUT*
- *HIGH SPEED: 10MHz UPDATE RATE FOR SMALL STEP CHANGES*
- *LOW GLITCH: 10mVpp GLITCH VOLTAGE*
- *SMALL SIZE: 32 PIN TDIP HYBRID*
- *WIDE OPERATING TEMPERATURE: -55° C to +125° C*

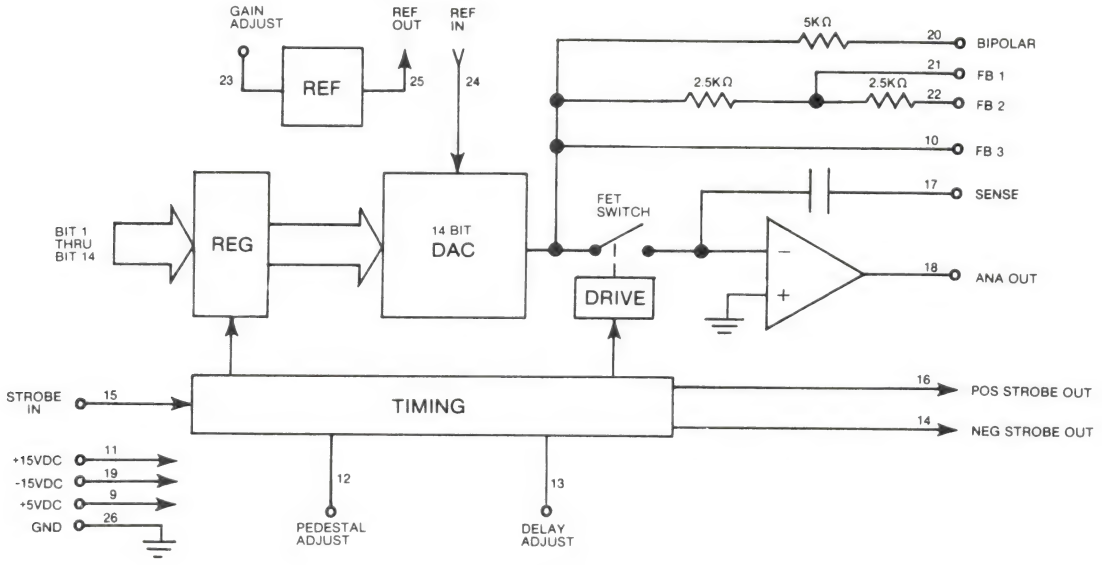


FIGURE 1. DAC-02310 BLOCK DIAGRAM

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TABLE 1. DAC-02310 AND DAC-02311 SPECIFICATIONS
Typical values at +25° and nominal power supply voltages unless otherwise specified.

PARAMETER	UNITS	VALUE	
		13 BIT LIN	12 BIT LIN
RESOLUTION	**Bits**	**14**	**14**
ACCURACY			
Linearity Error	% FSR	±0.006 max	±0.012 max
Linearity Tempco	ppm/°C	±1 max	±2 max
Gain Error (1)	% FSR	±0.1	±0.2
Gain Tempco	ppm/°C	±25 max	±25 max
Offset Error (1)	mV	±10	±20
Offset Tempco	ppmFSR/°C	20 max	20 max
Pedestal Error (1)	mV	±10	±20
Pedestal Tempco (2)	ppmFSR/°C	10	10
Monotonicity	Bits	13	12
DYNAMIC CHARACTERISTICS			
Settling Time to ±½ 0.01% FSR			
±10V Full Scale Change	μsec	1.8 max	
±5V Full Scale Change	μsec	1.1 max	
±2.5V Full Scale Change	μsec	0.6 max	
1 LSB Change	nsec	50 max	
Slew Rate	V/usec	20 typ 15 min	
Glitch (3)			
Voltage	mVpp	10 typ 30 max	
Energy (7)	mV•nsec	250 typ 750 max	
DIGITAL INPUTS			
Logic Compability		TTL	
Data Inputs			
Logic "1" Level	V	+2.0 to +5	
Logic "0" Level	V	0 to +0.8	
Loading		1 standard LS TTL load	
Coding (negative output)		Offset Binary (Bipolar) Binary (Unipolar)	
Strobe Input (4)			
Logic "1" Level	V	+2.0 to 5	
Logic "0" Level	V	0 to +0.8	
Loading		2 standard S TTL loads	
Width	nsec	10 min	
ANALOG OUTPUT			
Voltage Ranges (5)	V	±10, ±5, ±2.5, 0 to -10, 0 to -5	
Current Load	mA	±5 max	
Impedance	Ω	0.1 max	
REFERENCE			
Output Voltage	V	-10 ±0.1	
Output Current (6)	mA	±1 max	
Input Voltage	V	0 to -10	
Input Impedance	Ω	3.3K	
POWER SUPPLIES			
+15V Supply			
Tolerance	%	±5	
Max Voltage	V	+18 max	
Current Drain	mA	40 typ 50 max	
-15V Supply			
Tolerance	%	±5	
Max Voltage	V	-18 max	
Current Drain	mA	25 typ 35 max	
+5V Supply			
Tolerance	%	±5	
Max Voltage	V	+5.5 max	
Current Drain	mA	30 typ 45 max	
TEMPERATURE RANGE			
Operating (Case)			
-1 option	°C	-55 to +125	
-3 option	°C	0 to +70	
Storage	°C	-65 to +150	

TABLE 1. DAC-02310 AND DAC-02311 SPECIFICATIONS (CONT'D)

PARAMETER	UNITS	VALUE	
RESOLUTION	**Bits**	**14**	**14**
PHYSICAL CHARACTERISTICS			
Package		32 pin TDIP	
Size	in (mm)	1.15×1.75×0.21 (29×44×5)	
Weight	oz (g)	0.67 (19)	

NOTES: (1) Gain, offset, and pedestal errors are trimmable to zero.
(2) Pedestal tempco is with no delay adjust capacitor pin 13 to pin 14.
(3) Glitch is at 1 MHz update rate with a 5MHz filter.
(4) Strobe input is a positive pulse. Data transferred on rising edge.
(5) Output voltage ranges are pin programmable.
(6) Measured with REFIN, REFOUT and BIPOLAR pins connected together.
(7) Max Energy valid for 5V power supply ±2% Energy increases at 150mV/%5V power supply.

TECHNICAL DESCRIPTION

GENERAL

DAC-02310 is a completely self-contained deglitched D/A converter. As shown in the block diagram of Figure 1, it contains a 14 bit DAC, input registers, a precision DC reference, a track/hold deglitcher output and timing circuits. Its layout and compatible components provide the complete solution to low noise DAC design problems.

TIMING

Upon application of a STROBE IN signal the input registers are updated and the DAC-02310 output is held constant. As shown in Figure 2, the rising edge of the STROBE IN signal latches the input data. Internal timing circuits generate a POS STROBE OUT pulse which is used to open the FET switch at the op amp summing point. The output remains constant since the op amp feedback capacitor is charged. During this hold mode interval of approximately 40 nanoseconds, the DAC is changing value and its output glitch is settling to zero. At the end of the hold interval, POS STROBE OUT returns to is original track mode level and the FET switch closes. The DAC-02310 then smoothly changes to its new output level. The track/hold has effectively "masked out" the DAC glitch. POS STROBE OUT (pin 16) and NEG STROBE OUT (pin 14) should not be loaded with external circuitry.

DELAY ADJUST

The hold time interval is internally set to approximate 40 nanoseconds. For applications, such as CRT displays, which may require matched delays, an external DELAY ADJUST pin is provided. By adding a capacitor from pin 13 to pin 14, the hold time interval is made longer. This effectively increases the delay of the DAC-02310. Figure 3 illustrates the effect on hold time of adding capacitance to pin 13.

EXTERNAL TRIMS

Factory adjustment of DAC-02310 offset, gain and pedestal errors result in performance that is adequate for most applications. For more critical applications, DAC-02310 provides pins for externally trimming offset, gain and pedestal errors to zero. Figure 4 illustrates trim pot values and circuit connections for external trims.

OUTPUT VOLTAGE PROGRAMMING

DAC-02310 can be programmed for 5 different output voltage ranges by external jumpers between pins. Figure 6 illustrates the jumper connections required to yield ±10V, ±5V, ±2.5V, 0 to -10V, and 0 to -5V output voltage ranges.

OUTPUT CURRENT

The DAC-02310 can drive a load of ±5mA. For applications with higher current loads, the DAC-02310 can be used with a current booster. Figure 5 shows the interconnection of the DAC-02310 and DDC model HCD-13 hybrid cable driver; this allows the use of ±200mA loads.

INTERNAL REFERENCE

DAC-02310 contains a precision -10 volt internal reference which is made available for external use. For normal operation, REF OUT (Pin 25) must be jumpered to REF IN (Pin 24). Under these conditions, a maximum output current of 1 milliamp will be provided by the internal reference, while maintaining rated performance.

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DAC-02310 deglitched D/A converter, high frequency layout considerations must be kept in mind when designing its printed circuit board. All analog conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Digital inputs and analog output must be kept separated from each other to minimize crosstalk. Circuits connected to the analog output must be kept as close to the D/A converter package as possible. Circuit connections to the external adjustment (offset, gain and pedestal) pins must be kept as short as possible, and must be kept separated from digital lines to minimize noise coupling.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each power supply for minimum noise operation. Each of the power supplies should have a 1 microfarad or larger tantalum capacitor in parallel with a 0.01 microfarad ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

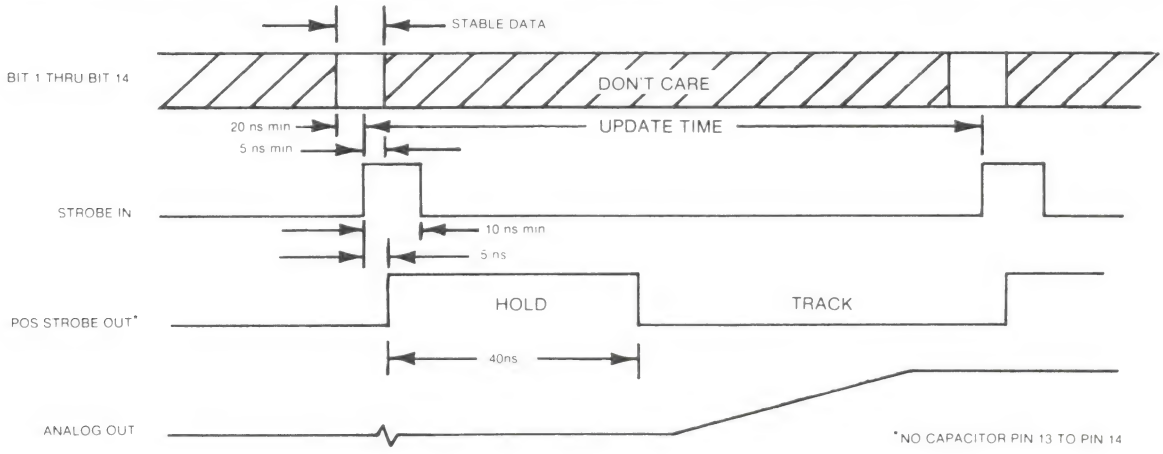


FIGURE 2. TIMING DIAGRAM

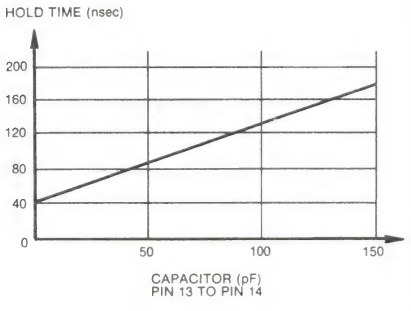


FIGURE 3. DELAY (HOLD) TIME ADJUST

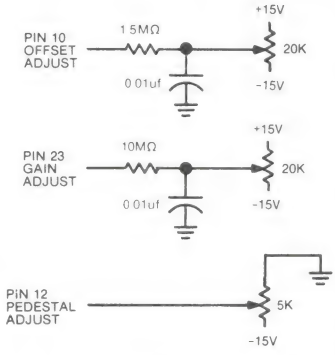


FIGURE 4.
EXTERNAL TRIM CIRCUITS

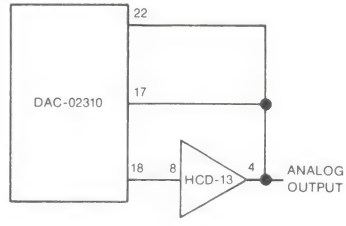


FIGURE 5. DAC-02310 AND CURRENT BOOSTER INTERCONNECTION

	JUMPER CONNECTIONS				
Voltage Range	**Pin 22 to**	**Pin 21 to**	**Pin 20 to**	**Pin 17 to**	**Pin 24 to**
±10V	Pin 18	—	Pin 25	Pin 18	Pin 25
±5V	Pin 18	Pin 22	Pin 25	Pin 18	Pin 25
±2.5V	Pin 10	Pin 18	Pin 25	Pin 18	Pin 25
0 to -10V	Pin 18	Pin 22	—	Pin 18	Pin 25
0 to -5V	Pin 10	Pin 18	—	Pin 18	Pin 25

FIGURE 6. OUTPUT VOLTAGE PROGRAMMING

	OUTPUT VOLTAGE*	
INPUT DATA	BIPOLAR	UNIPOLAR
00 0000 0000 0000	+5.0000V	0
01 1111 1111 1111	+0.0006V	—4.9994V
10 0000 0000 0000	0	-5.0000V
11 1111 1111 1111	-4.9994V	-9.9994V

*10 Volt Full Scale Range

FIGURE 7. INPUT DATA CODING

TABLE 2. PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 8	17	Sense
2	Bit 7	18	Analog Out
3	Bit 6	19	-15 Volts
4	Bit 5	20	Bipolar
5	Bit 4	21	Feedback 1
6	Bit 3	22	Feedback 2
7	Bit 2	23	Gain Adjust
8	Bit 1 (MSB)	24	Reference In
9	+5 volts	25	Reference Out
10	Feedback 3	26	Ground
11	+15 Volts	27	Bit 14 (LSB)
12	Pedestal Adjust	28	Bit 13
13	Delay Adjust	29	Bit 12
14	Neg. Strobe Out	30	Bit 11
15	Strobe In	31	Bit 10
16	Pos. Strobe Out	32	Bit 9

ORDERING INFORMATION

DAC-02310-103

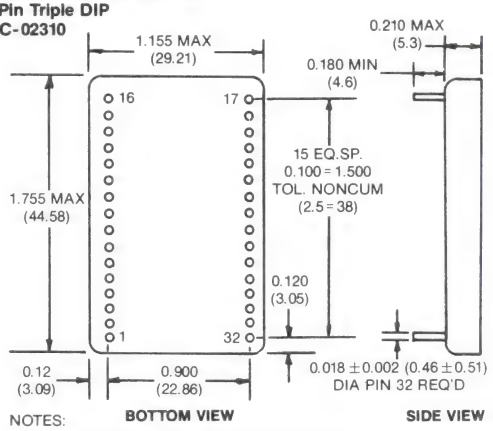
- Linearity Grade:
  - 3 = 13 bit
  - 2 = 12 bit
- Reliability Grade:
  - 0 = Standard DDC procedures
  - 1 = Military processing available.*
  - 2 = Military processing available but without QCI testing.*
- Operating Temperature Range (case):
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Packaging:
  - 0 = 32 pin TDIP
  - 1 = 32 pin flatpack

*Consult factory for details.

For current booster order HCD-13.

MECHANICAL OUTLINE

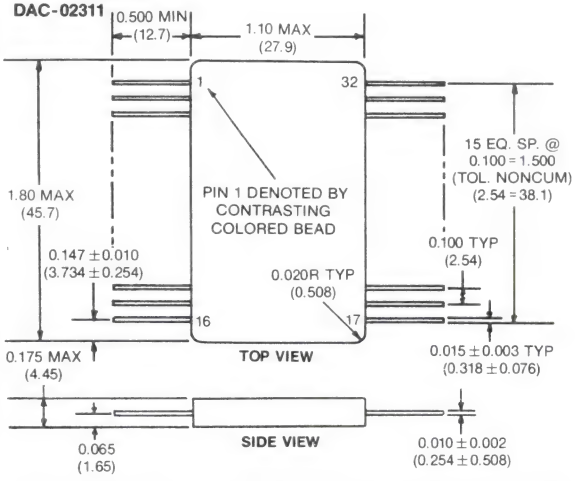
32 Pin Triple DIP
DAC-02310



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply at seating plane (TDIPs only).
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

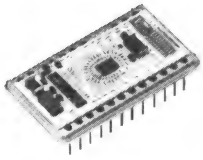
MECHANICAL OUTLINE

32 Pin Flatpack
DAC-02311

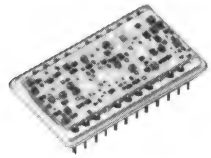


DAC-02315 AND DGL-02316

12 BIT DEGLITCHED D/A CONVERTER
35 MHz Update Rate; Voltage Output



DAC-02315



DGL-02316

DESCRIPTION

The DAC-02315 and DGL-02316 is a 12 bit, 35 MHz update rate, deglitched DAC hybrid pair with a low impedance voltage output. Packaged in small, 24 pin DDIP hybrids, the DAC-02315 and DGL-02316 offer a −55°C to +125°C operating temperature range and screening to MIL-STD-883B, revision C.

The DAC-02315 and DGL-02316 pair offers 35 nsec settling for a full scale change offset and pedestal errors trimmable to zero with external potentiometers.

With its 12 bit resolution, low glitch voltage output and small hermetic packages, the DAC-02315 and DGL-02316 is ideal for the most demanding low noise applications such as vector-stroke CRT display, waveform generators and automatic test equipment.

FEATURES

- *HIGH SPEED – 35 MHz UPDATE RATE FOR FULL SCALE CHANGES*
- *LOW GLITCH – 14mVpp GLITCH VOLTAGE 38ns GLITCH DURATION*
- *SMALL SIZE – 24 PIN DDIP HYBRIDS*
- *−55°C TO +125°C OPERATION*
- *MIL-STD-883 SCREENING AVAILABLE*
- *FULL FUNCTION – EVALUATION CARD AVAILABLE*

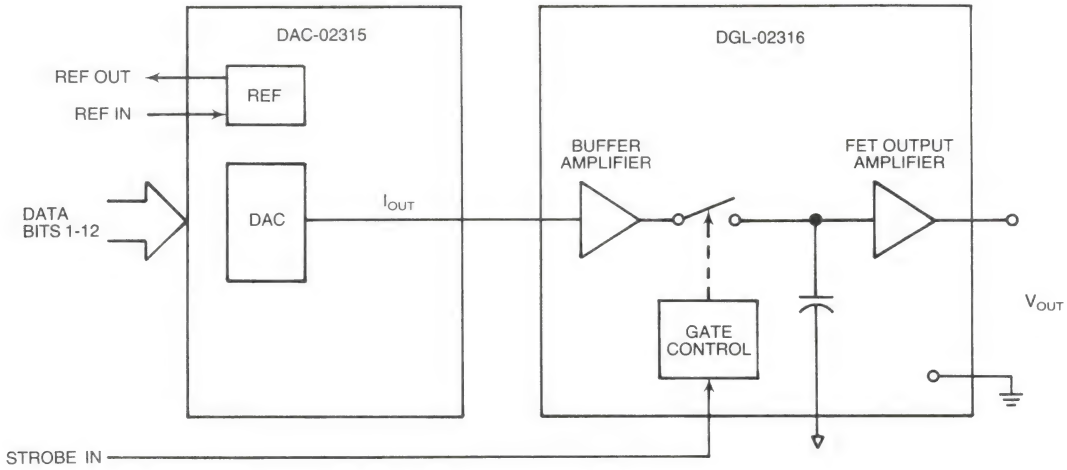


FIGURE 1. DAC-02315/DGL-02316 BLOCK DIAGRAM

TABLE 1. DAC-02315/DGL-02316 SPECIFICATIONS

Typical values at 25°C and nominal power supply voltages unless otherwise specified.

PARAMETER	UNITS	VALUE
ACCURACY		
Linearity Error (2K max load)	% FSR	+0.0125 max
Linearity Tempco	PPM/°C	±5
Offset (trimmable to zero)	mV	25 typ, 100 max
Offset Tempco	mV/°C	0.2 typ, 0.5 max
Pedestal	mV	25 typ, 100 max
Pedestal Tempco	μV/°C	60 typ, 150 max
Monotonicity	bits	12
DYNAMIC CHARACTERISTICS		
Settling Time (½ LSB)		
Full Scale Change	nsec	35 typ, 50 max
1 LSB Change	nsec	20 typ
Update Rate	MHz	35 min
Slew Rate	V/μsec	400 min
Glitch Amplitude (20 MHz Filtered)	mV	14 max
Glitch Duration (20 MHz Filtered)	nsec	38 max
DIGITAL INPUTS		
Logic Compatibility		ECL
Data Inputs		
Logic 1	V	−0.81 to −0.96 (100μA max)
Logic 0	V	−1.65 to −1.85 (1 A max)
Coding		
Unipolar		Complementary Binary
Bipolar		Complementary Offset Binary
ANALOG OUTPUTS		
Voltage Range	V	+0.5 max
Steady State Current	mA	±1 max (for 0.01%)
Transient Current	mA	±50 max
Output Impedance	Ohms	5 typ, 10 max
REFERENCE AND SIGN OFFSET		
Internal +10.000V Ref		
Accuracy	%FS	±0.1 max
Max Current Out	mA	15 max
Optional External Ref	V	+10 ±10%
Ref Current Requirement		
Ref Input	mA	4.0 typ, 4.4 max
Sign Offset	mA	8.0 typ, 8.8 max

POWER SUPPLIES					
Voltage	V	+15	−15	−5.2	−1.3
Regulation for Full Accuracy	%	±2	±2	±5	±3
Current	mA typ	85	112	45	0.5
	mA max	100	125	65	2.0

TEMPERATURE RANGE		
-1 Option (Case)	°C	−55 to +125
-3 Option (Case)	°C	0 to + 70
Storage	°C	−65 to +150
PHYSICAL CHARACTERISTICS		
Package (each hybrid)		24 Pin DDIP
Size	in (mm)	1.4 x 0.8 x 0.2 (35.56 x 20.32 x 5.08)
Weight	oz (g)	0.4 (11.2)

INTRODUCTION

The DAC-02315 and DGL-02316 is composed of two hybrids: a D/A converter and track/hold deglitcher. These modules may be purchased separately by the user to assemble in his own system. The DAC-04300 evaluation card includes, in addition to the hybrid pair, TTL/ECL translators, input latches, trim potentiometers and a careful layout with distributed capacitors to optimize glitch and settling time characteristics. Figure 2 illustrates the DAC-04300 Evaluation Card schematic as a layout example.

The DAC-02315 generates analog output currents which are digitally controlled, binary weighted, discrete fractions of a reference voltage. Typically, the internal reference of the DAC is used for this purpose, although external regulated references may also be employed. The analog output is controlled by a ladder network of thin film precision resistors, controlled by bipolar transistor switches turned on and off in accordance with the digital input code.

The DGL-02316 track/hold deglitcher includes a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltages are both buffered by amplifiers. The switch is controlled by an ECL logic gate signal which determines whether the holding capacitor voltage and output voltage will track the input signal (switch closed, logic 0) or will be held constant, retaining the value of the input at the moment the switch opens (switch open, logic 1). Figure 3 illustrates output waveforms of the DAC-02315/DGL-02316.

The following applications information includes the characteristics both of the DAC-04300 evaluation card and of the individual modules as part of a D/A converter.

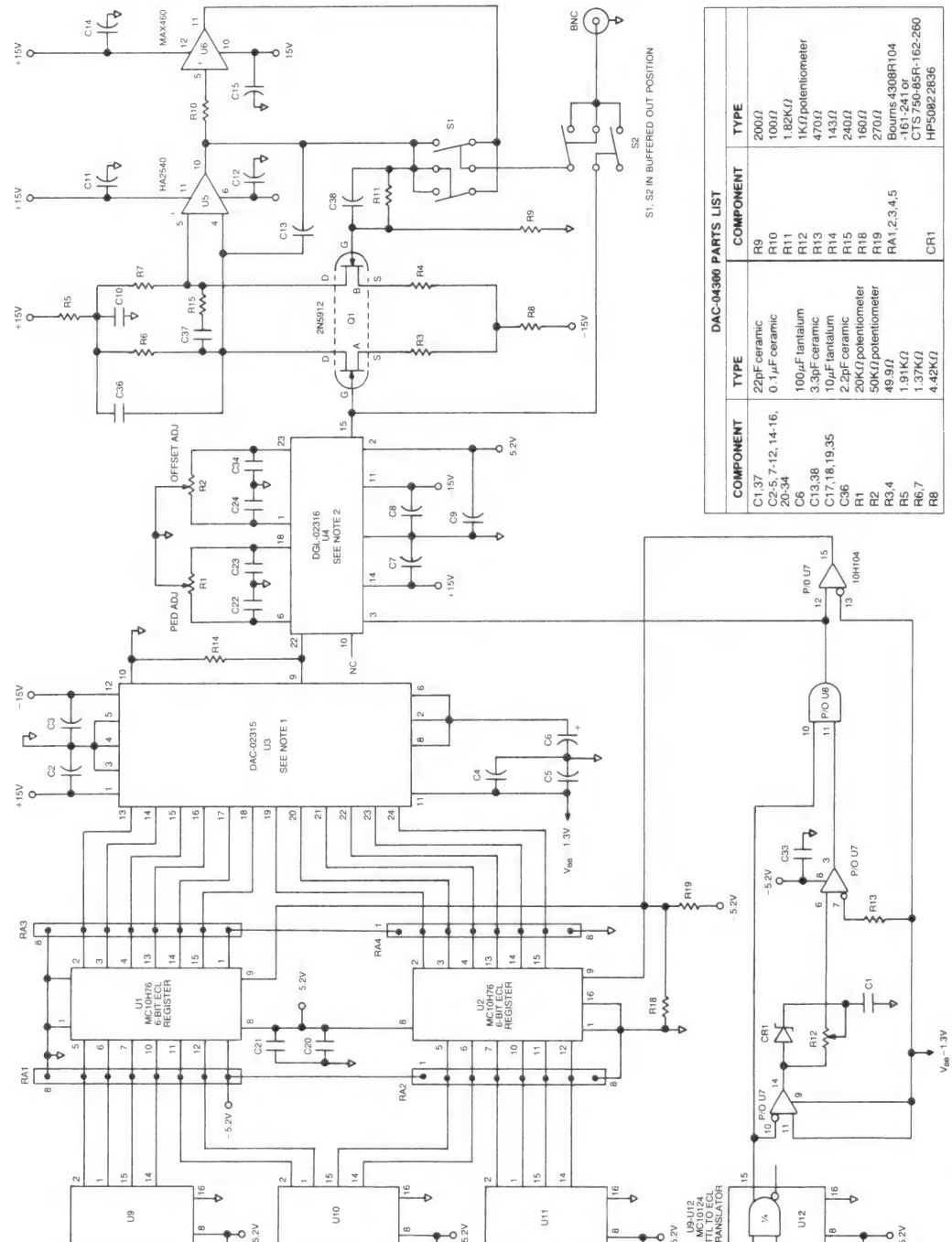
DEGLITCHING

Glitches (voltage spikes) in the output of the conventional D/A converters are primarily caused by data skew and by switches which cause faster turn-on than turn-off times. Thus, whenever a code change occurs, there will be a short period of time (measured in nsec) when some spurious codes will exist. The DAC will attempt to follow these codes, resulting in a transient known as a glitch. The worst case occurs at the major carry point when the input codes are transitioning from 1000...0 to 0111...1. The spurious code may then be 1111...1, and the D/A output will momentarily slew full scale.

The DAC-02315/DGL-02316 minimizes these glitches by using a carefully designed low transient track and hold amplifier (deglitcher) after the D/A. Thus, the deglitcher can be gated into the hold mode during the D/A output transient and released into the track mode after the transients have settled out. The resultant output then makes a very clean transition from one value to another. Using this technique, glitches are not only greatly reduced, but are only a function of deglitcher design, and hence are the same for any transition and can be effectively filtered out.

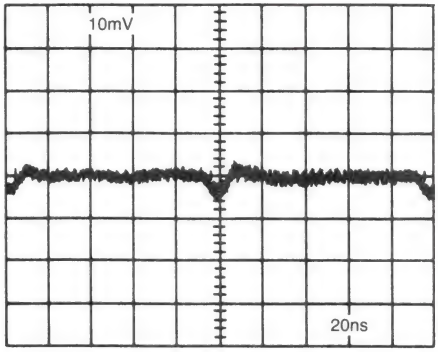
INPUT LATCHES

Input latches must be employed in order to minimize data skew and digital feedthrough errors associated with high speed digital circuitry. ECL MC-10H76 registers are recommended either directly or in tandem with TTL/ECL MC-10124 translators, as shown in the schematic in figure 2. Figure 4 illustrates an appropriate input latch configuration.


DAC-04300 PARTS LIST
COMPONENT | TYPE | COMPONENT | TYPE
C1,37 | 22pF ceramic | R9 | 200Ω
C2-5, 7-12, 14-16, 20-34 | 0.1μF ceramic | R10 | 100Ω
C6 | 100μF tantalum | R11 | 1.82KΩ
C13,38 | 3.3pF ceramic | R12 | 1KΩ potentiometer
C17,18,19,35 | 10μF tantalum | R13 | 470Ω
C36 | 2.2pF ceramic | R14 | 143Ω
R1 | 20KΩ potentiometer | R15 | 240Ω
R2 | 50KΩ potentiometer | R18 | 160Ω
R3,4 | 49.9Ω | R19 | 270Ω
R5 | 1.91KΩ | RA1,2,3,4,5 | Bourns 4308R104-161-241 or CTS 750-85R-162-260
R6,7 | 1.37KΩ | CR1 | HP5082-2836
R8 | 4.42KΩ
S1, S2 IN BUFFERED OUT POSITION
DAC-02315 U3 SEE NOTE 1
DGL-02316 U4 SEE NOTE 2
U1 MC10H476 6-BIT ECL REGISTER
U2 MC10H476 6-BIT ECL REGISTER
U9-U12 MC10124 TTL TO ECL TRANSLATOR
MAX460
HA2540
2N5912
10H104
OFFSET ADJ
PED ADJ
MSB
BNC
+15V
-15V
-5.2V
5.2V
1.3V

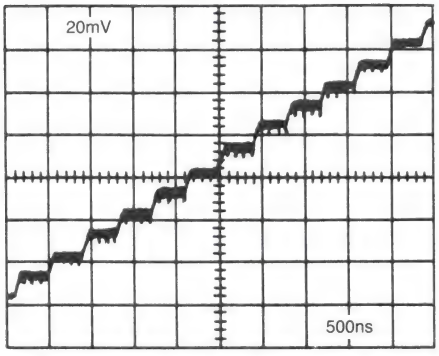
NOTES:
1. DAC-02315 (U3) pins 3,4, and 5 are grounded.
2. DGL-02316 (U4) pins 4,7,8,9,12,13,16,21,24,5,17,19,and 20 are grounded.

FIGURE 2. DAC-04300 EVALUATION CARD SCHEMATIC



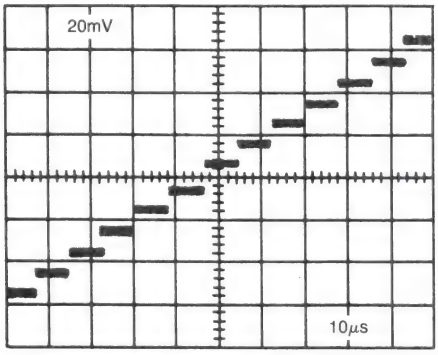
10MHz Clock, 10MHz Filter

MAJOR TRANSITION

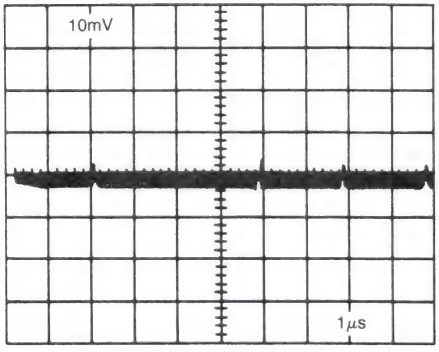


10MHz Clock, 10MHz Filter

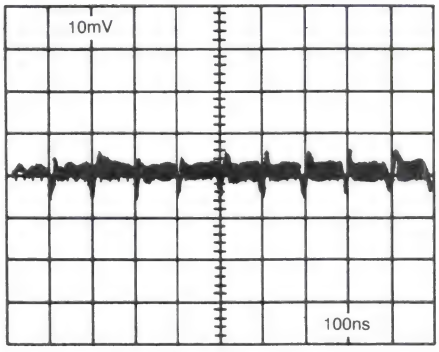
MAJOR TRANSITION



500KHz Clock, 10MHz Filter



500KHz Clock, 10MHz Filter



10MHz Clock, 10MHz Filter

Note: All scope photos referenced to ±5V FSR

FIGURE 3. OUTPUT WAVEFORMS

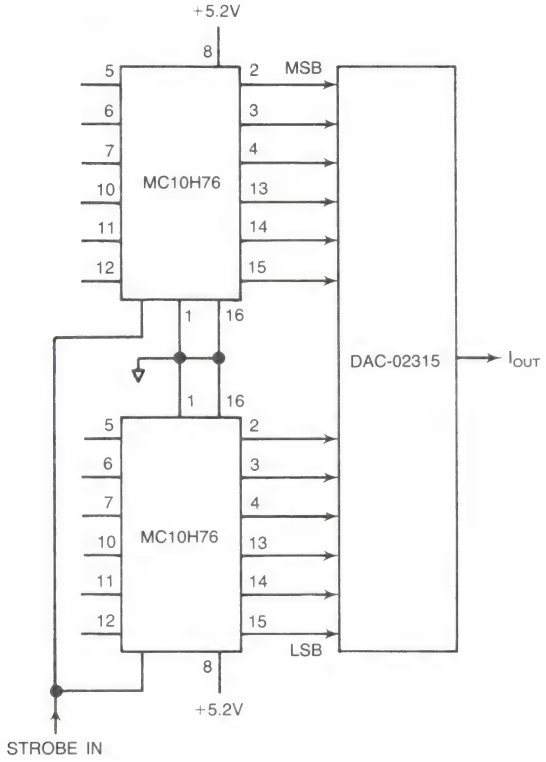


FIGURE 4. INPUT LATCH CONFIGURATION

TIMING

As illustrated in figure 5, the user's strobe pulse activates the timing circuit in the deglitcher. The timing circuit simultaneously opens the T/H amplifier switch so that its output remains constant. The latch is activated so that the input data bits are converted to an analog current by the D/A converter. After the analog current conversion has been completed, the T/H amplifier switch is closed again. The T/H amplifier then tracks the D/A converter, converting the D/A current into a voltage. The system output becomes stable after the T/H settles out.

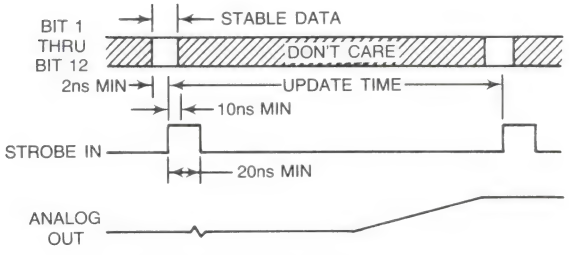


FIGURE 5. DAC-02315/DGL-02316 OUTPUT WAVEFORMS

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DAC-02315/DGL-02316 deglitched D/A converter, high frequency layout considerations must be kept in mind when designing its printed circuit board. All analog conductor lengths must be kept to a minimum; in particular, the DAC-02315 output (pin 9) and DGL-02316 analog input (pin 22).

Figure 6 illustrates a recommended layout with regard to DAC-02315/DGL-02316 and input latch relative positioning. A large area ground plane must be used to keep ground impedances as low as possible. Digital inputs and analog output must be kept separated from each other to minimize crosstalk. Circuits connected to the analog output must be kept as close to the D/A converter package as possible. Circuit connections to the external adjustment (offset, gain and pedestal) pins must be kept separated from digital lines to minimize noise coupling.

Figure 6 illustrates a recommended layout. Figure 12 illustrates the suggested physical positioning of these components to achieve optimal performance.

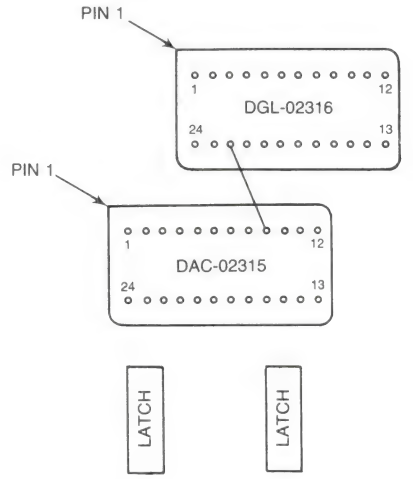


FIGURE 6. RECOMMENDED LAYOUT

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each power supply for minimum noise operation. Figure 7 illustrates a recommended power supply decoupling scheme for the DAC-02315/DGL-02316. All capacitors must be mounted as close as possible to the hybrid packages. Note that the offset and pedestal trim adjustments are also decoupled (see figure 8).

EXTERNAL TRIMS

Factory adjustment of DAC-02315/DGL-02316 gain, offset and pedestal errors result in performance which is adequate for most applications. For more critical requirements, the DGL-02316 provides pins for externally trimming offset and pedestal errors to zero. Figure 8 illustrates trim pot values and circuit connections for external trims. Figure 9 illustrates scope traces during output trim adjustments.

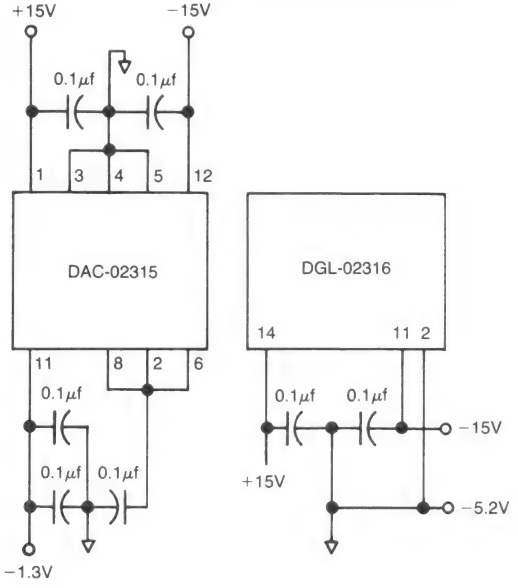


FIGURE 7. POWER SUPPLY DECOUPLING

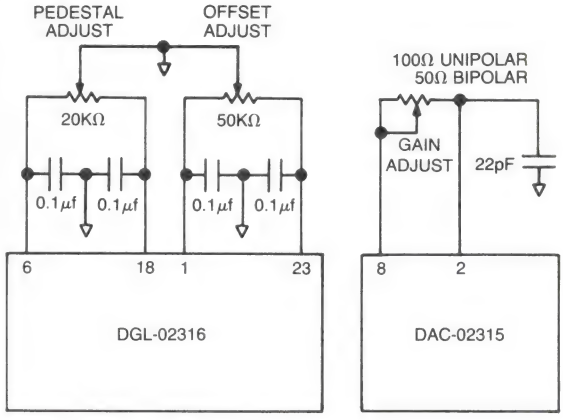


FIGURE 8. PEDESTAL, GAIN AND OFFSET TRIM CIRCUITS

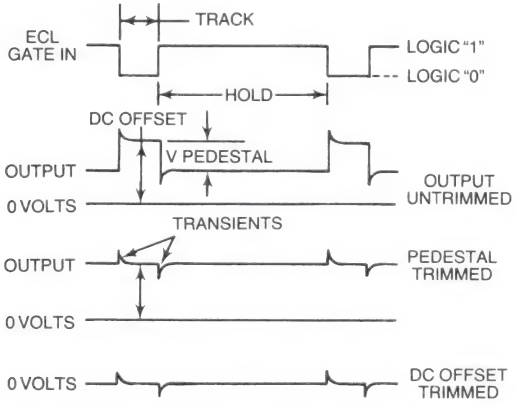


FIGURE 9. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

REFERENCE

The DAC-02315 has an internal reference supply and is factory calibrated with this supply. Fixed external references of +10VDC±10% can be accomodated and the output current will be linearly proportional to the reference voltage over this range.

ANALOG OUTPUT

Figure 10 illustrates a scheme for achieving ±5V output. Since the DAC-02315/DGL-02316 is rated for ±0.5V at ±1mA, an output buffer amplifier must be used to achieve higher output voltage levels and to maintain 12 bit linearity, under heavy load.

OUTPUT CODING

The DAC-02315 accepts either complementary binary input data for unipolar analog output or bipolar complementary offset binary data for bipolar analog output. Table 2 illustrates the Bit Weight Table for the DAC-02315.

DAC-04300 EVALUATION CARD

Figure 11 illustrates the block diagram for the DAC-04300 VME demo card which incorporates TTL/ECL translators, ECL latches, DAC-02315, DGL-02316, output buffer amplifiers, and timing diagram circuitry to achieve 12-bit, 35 MHz performance. Figure 12 illustrates switch configurations for output drive options (±0.5V into 1kΩ and ±5.0V into 50Ω or 1kΩ). Figure 13 illustrates the mechanical outline of the card and Table 3 delineates the DAC-040300 evaluation card pin-out.

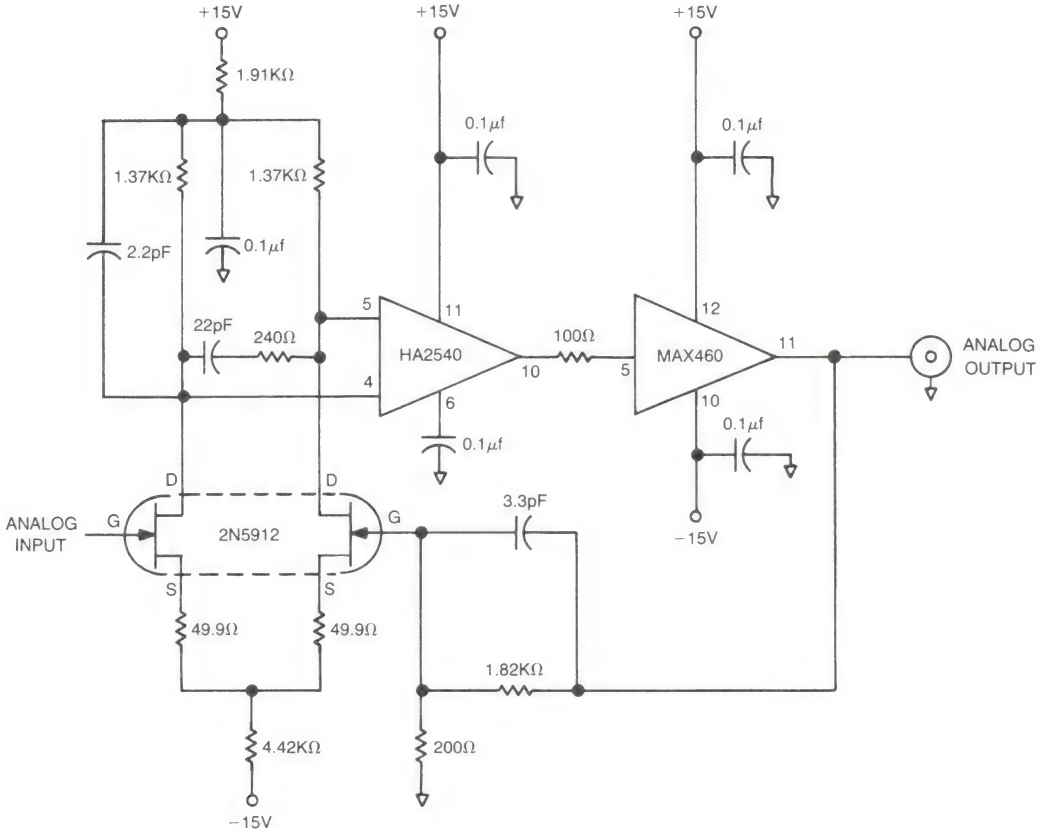


FIGURE 10. +5V ANALOG OUTPUT CIRCUIT

TABLE 2. BIT WEIGHT TABLE												
ANALOG OUTPUT		DIGITAL BIT INPUTS										
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12
+F.S. −1 LSB	+F.S. −1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+¾ F.S.	+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+½ F.S.	+1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+½ F.S. −1 LSB	−1 LSB	1	0	0	0	0	0	0	0	0	0	0	0
+¼ F.S.	−½ F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+1 LSB	−F.S. +1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	−F.S.	1	1	1	1	1	1	1	1	1	1	1	1

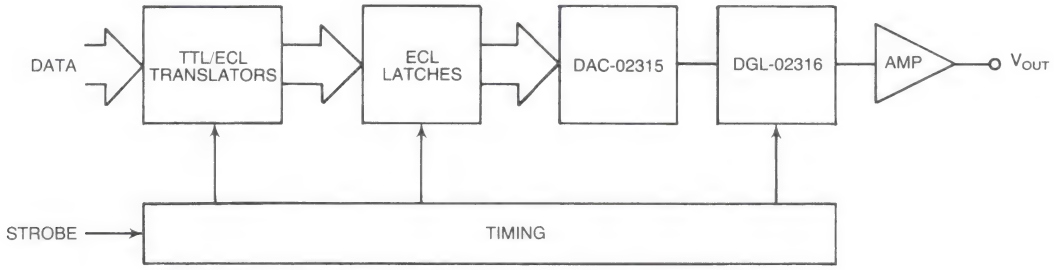
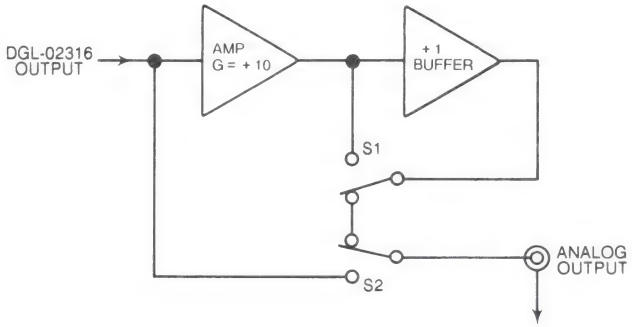


FIGURE 11. DAC-04300 EVALUATION CARD BLOCK DIAGRAM



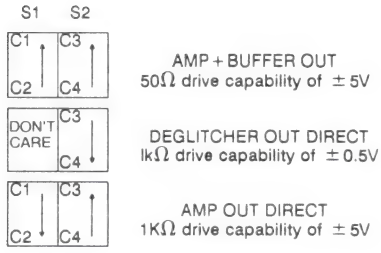
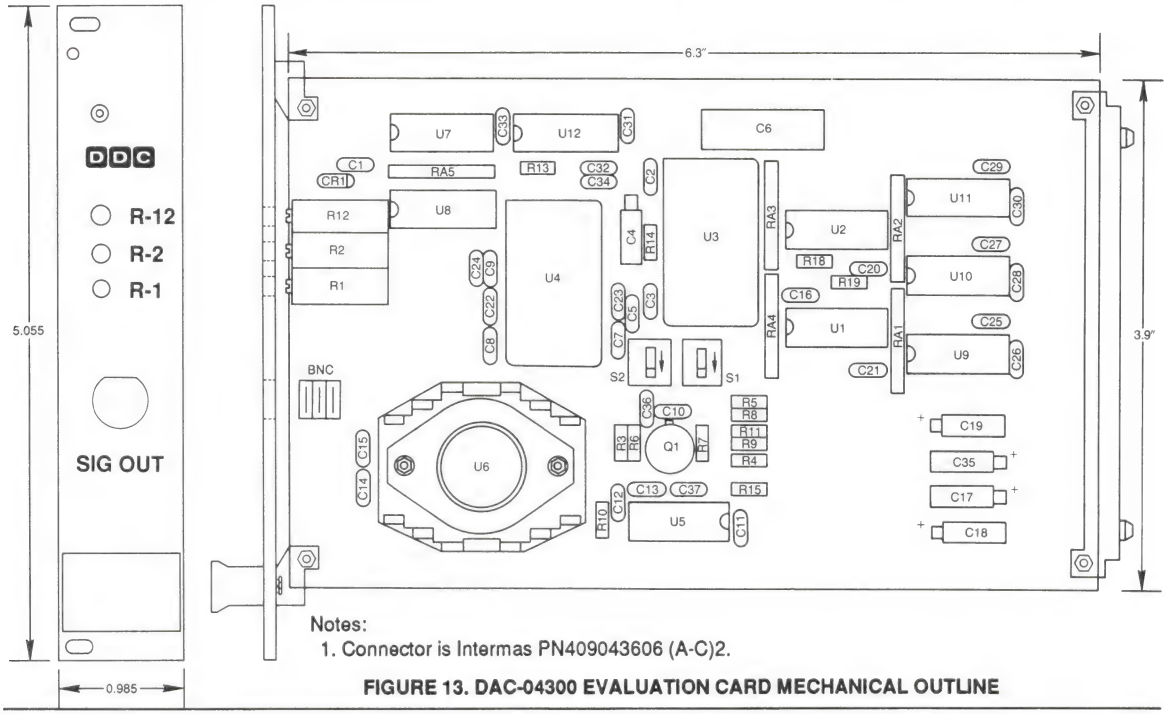


FIGURE 12. DAC-04300 OUTPUT OPTIONS



Notes:
1. Connector is Intermas PN409043606 (A-C)2.

FIGURE 13. DAC-04300 EVALUATION CARD MECHANICAL OUTLINE

TABLE 3. DAC-02315 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15VDC Input	13	Bit 1 (MSB)
2	Ref. Out	14	Bit 2
3	Ground*	15	Bit 3
4	Ground*	16	Bit 4
5	Ground*	17	Bit 5
6	Signal Offset	18	Bit 6
7	Feedback 2	19	Bit 7
8	Ref. In	20	Bit 8
9	Output	21	Bit 9
10	Feedback 1	22	Bit 10
11	$-1.3VDC = V_{bb}$	23	Bit 11
12	−15VDC	24	Bit 12 (LSB)

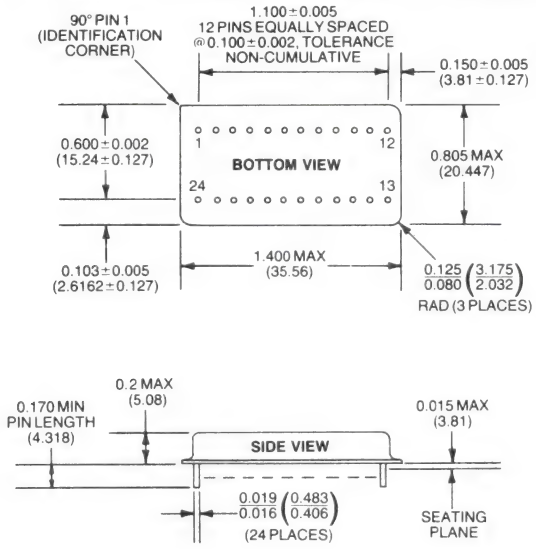
*All grounds are tied to the case.

TABLE 4. DGL-02316 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Offset Adjust	13	Analog Ground
2	−5.2 VDC	14	+15 VDC
3	Gate Input	15	Output
4	Digital Ground	16	Analog Ground
5	NC	17	NC
6	Pedestal Adjust	18	Pedestal Adjust
7	Analog Ground	19	NC
8	NC	20	NC
9	Analog Ground	21	Analog Ground
10	NC	22	Analog Input
11	−15 VDC	23	Offset Adjust
12	Analog Ground	24	Analog Ground

TABLE 5. DAC-04300 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
C1	Strobe	C18	Ground
C2	Ground	C19	Bit 4
C3	Bit 12 (LSB)	C20	Ground
C4	Ground	C21	Bit 3
C5	Bit 11	C22	Ground
C6	Ground	C23	Bit 2
C7	Bit 10	C24	Ground
C8	Ground	C25	Bit 1 (MSB)
C9	Bit 9	C26	Ground
C10	Ground	C27	−5.2 VDC
C11	Bit 8	C28	+5 VDC
C12	Ground	C29	+15 VDC
C13	Bit 7	C30	−15 VDC
C14	Ground	C31	Ground
C15	Bit 6	C32	No Connection
C16	Ground	A1 to	
C17	Bit 5	A32	Ground



Notes:
(1.) Dimensions are shown in inches (millimeters).
(2.) Load identification numbers are for reference only.
(3.) Lead spacing dimensions apply only at seating plane.
(4.) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
(5.) Case tied to analog ground.

FIGURE 14. 24 PIN DDIP MECHANICAL OUTLINE

ORDERING INFORMATION

DAC-02315-112

- Reliability Grade:
  - 0 = Standard DDC procedures.
  - 1 = Fully compliant with MIL-STD 883.
  - 2 = Screened to MIL-STD-883 but without QCI testing.
- Operating Temperature Range (Case):
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Type:
  - DAC-02315
  - DGL-02316

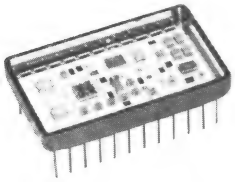
DAC-04300 Evaluation Card

B

D

DAC-02320

12 BIT DEGLITCHED D/A CONVERTER
15 MHz Update Rate; Voltage Output



PRELIMINARY

DESCRIPTION

Continuing DDC's series of leadership display DACs, the DAC-02320 is a 12 bit, 15 MHz update rate, deglitched hybrid D/A converter with a low impedance voltage output. Its input registers, precision dc voltage reference, and track/hold deglitcher output provide the complete solution to low noise DAC requirements. Packaged in a small 24 pin DDIP, the DAC-02320 operates over the full -55°C to +125°C temperature range and military processing is available (consult factory).

DAC-02320 is available in linearity grades of 13 bits (±0.006%) and 12 bits (±0.012%). It can be pin programmed for 3 different output voltage ranges. Offset and gain errors can be trimmed to zero with external potentiometers.

APPLICATIONS

With its 12 bit resolution, low glitch voltage output, and small hermetic package, the DAC-02320 is ideal for the most demanding low noise DAC requirements. It is particularly well suited for applications such as vector-stroke CRT displays, waveform generators, and automatic test equipment.

FEATURES

- *FULL FUNCTION: INCLUDES INPUT REGISTERS AND TRACK/HOLD DEGLITCHER OUTPUT*
- *HIGH SPEED: 15 MHz UPDATE RATE FOR SMALL STEP CHANGES 200 NSEC SETTLING FOR F.S.*
- *SMALL SIZE: 24 PIN DDIP HYBRID*
- *WIDE OPERATING TEMPERATURE: -55°C to +125°C*

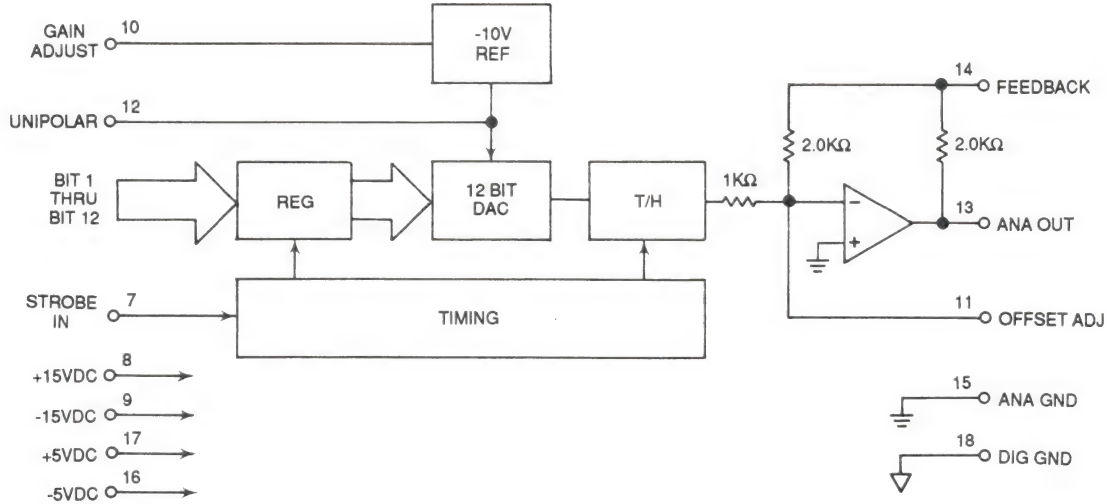


FIGURE 1. DAC-02320 BLOCK DIAGRAM

TABLE 1. DAC-02320 SPECIFICATIONS

Typical values at +25°C case temperature and nominal power supply voltages unless otherwise specified.

PARAMETER	UNITS	VALUES	
		13 BIT LIN	12 BIT LIN
RESOLUTION	Bits	12	12
ACCURACY			
Linearity Error	%FSR	±0.006 max	±0.012 max
Linearity Error Tempco	ppm FSR/°C	±1 max	±2 max
Gain Error(1)	%FSR	±0.1	±0.2
Gain Error Tempco	ppm FSR/°C	±25 max	±25max
Offset Error(1)	mV	±10	±20
Offset Error Tempco	ppm FSR/°C	±20 max	±20max
Monotonicity	Bits	12	12
DYNAMICS			
Settling Time to ±0.01% FSR			
±10V FS Change	nsec	200 max	
±5V FS Change	nsec	180 max	
1 LSB Change	nsec	50 max	
Slew Rate	V/usec	300 typ 200 min	
Glitch (2)			
Voltage	mVpp	10 typ 30 max	
Energy	mV ·nsec	250 typ 750 max	
DIGITAL INPUTS			
Logic Compatibility		TTL	
Data Inputs			
Logic "1" Level	V	+2.0 to +5	
Logic "0" Level	V	0 to +0.8	
Loading		1 standard LS TTL load	
Coding (negative output)		Offset Binary (Bipolar)Binary (Unipolar)	
Strobe Input (3)			
Logic "1" Level	V	+2.0 to 5	
Logic "0" Level	V	0 to + 0.8	
Loading		2 standard S TTL Loads	
Width	nsec	10 min	
ANALOG OUTPUT			
Voltage Ranges (4)	V	±10, ±5, 0 to +10	
Current Load	mA	±20min	
Impedance	ohm	0.1max	
POWER SUPPLIES			
+15 Volt Supply			
Tolerance	%	±5	
Max Voltage	V	+18 max	
Current Drain	mA	70 typ 100 max	
-15 Volt Supply			
Tolerance	%	±5	
Max Voltage	V	-18 max	
Current Drain	mA	35 typ 60 max	
+5 Volt Supply			
Tolerance	%	±10	
Max Voltage	V	+7 max	
Current Drain	mA	70 typ, 100 max	
-5 Volt Supply			
Tolerance	%	±5	
Max Voltage	V	-7 max	
Current Drain	mA	50 typ, 75 max	

TABLE 1. DAC-02320 SPECIFICATIONS (continued)

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	2.2 typ, 3.3 max
TEMPERATURE RANGE		
Operating (Case)		
-1 Option	°C	-55 to +125
-3 Option	°C	0 to +70
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Package		24 pin DDIP hybrid
Size	in	1.300 x 0.790 x 0.210
	(mm)	(33.020 x 20.066 x 5.334)
Weight	oz (g)	0.4 (11.3)

NOTES:

(1) Gain and offset errors are trimmable to zero.

(2) Glitch is at 1 MHz update rate with a 5MHz filter.

(3) Strobe input is a positive pulse. Data transferred on rising edge.

(4) Output voltage ranges are pin programmable.

TECHNICAL DESCRIPTION

GENERAL

DAC-02320 is a complete self-contained deglitched D/A converter. As shown in the block diagram of Figure 1, it contains a precision DAC , input registers, a precision DC reference, a track/hold deglitcher output , and timing circuits. Its layout and compatible components provide the complete solution to low noise DAC design problems.

TIMING

Upon Application of a STROBE IN signal the input registers are updated and the DAC-02320 output is held constant. As shown in Figure 2, the rising edge of the STROBE IN signal latches the input data. Internal timing circuits generate a pulse which is used to open the T/H. The output remains constant since the op amp feedback capacitor is charged. During the hold mode interval of approximately 20 nanoseconds, the DAC is changing value and its output glitch is settling to zero. At the end of the hold interval the T/H returns to its original track mode level. The DAC-02320 then smoothly changes to its new output level. The track/hold has effectively "masked out " the DAC glitch.

EXTERNAL TRIMS

Factory adjustment of DAC-02320 offset and gain errors result in performance that is adequate for most applications. For more critical applications, DAC-02320 provides pins for external trimming offset and gain errors to zero. Figure 3 illustrates trim pot values and circuit connections for external trims.

OUTPUT VOLTAGE PROGRAMMING

DAC-02320 can be programmed for 3 different output voltage ranges by external jumpers between pins: For ±10V range, no external connections ar e required; for ±5V range , pin 14 must be jumpered to pin 13; or for 0 to +10V range , pin 14 must be jumpered to pin 13 and pin 11 must be jumpered to pin 12.

SETTLING

The DAC-02320 settling time of 200 nsec max for a F.S. input and 50 nsec max for a 1LSB change is based on one strobe to the D/A and waiting for settling to ±0.001% FSR. For F.S. settling of the analog output at an update rate of 15MHz the T/H duty cycle must be considered. Since the encode rate is 15MHz, there are a total of 66 ⅔ nsec between strobes. For 20 nsec of this period the T/H is in HOLD where, by definition, the slew rate is zero. The remaining TRACK time of 66 ⅔ nsec slews at 200 V/µsec min. As a consequence the settling time to 0.01% FSR for a full scale change at a 15 MHz update rate is 280 nsec because 4 periods of HOLD, each of 20nsec duration, are added to the overall settling time. The T/H duty cycle must be considered for calculation of settling time at high update frequencies.

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DAC-02320 deglitched D/A converter, high frequency layout considerations must be kept in mind when designing its printed circuit board. All analog conductor lengths must be used to keep ground impedances as low as possible. Digital inputs and analog output must be kept separated from each other to minimize crossstalk. Circuits connected to analog output must be kept close to the D/A converter package as possible. Circuit connections to the external adjustment (offset and gain) pins must be kept separate from digital lines to minimize noise coupling.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each supply for minimum noise operation. Each of the power supplies should have a 1 microfarad or larger tantalum capacitor in parallel with a 0.01 microfarad ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

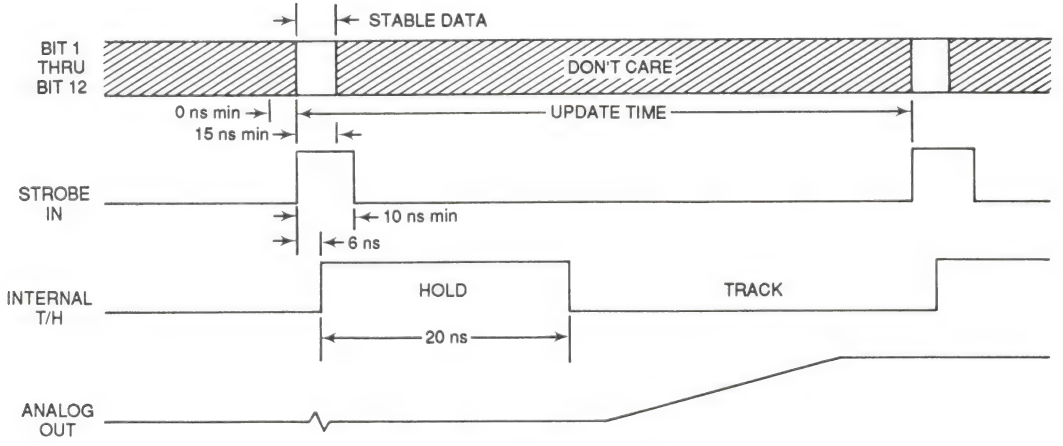


FIGURE 2. TIMING DIAGRAM

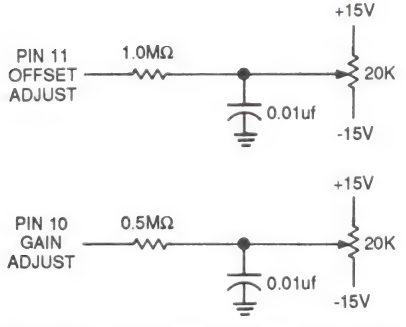
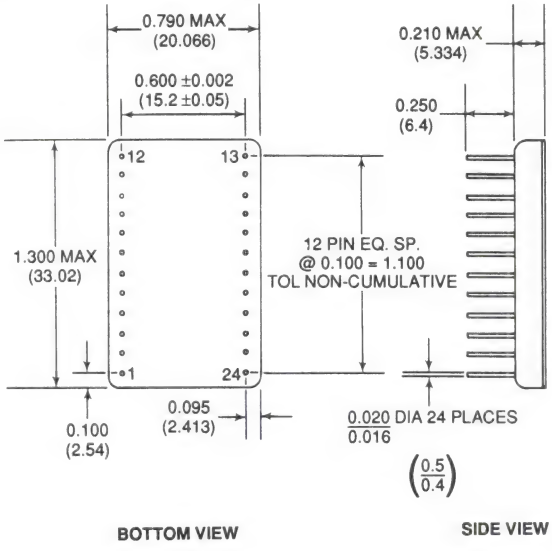


FIGURE 3. EXTERNAL TRIM CIRCUITS

TABLE 2. INPUT DATA CODING		
	OUTPUT VOLTAGE*	
INPUT DATA	BIPOLAR	UNIPOLAR
1111 1111 1111	+4.9976V	+9.9976V
1000 0000 0000	0	+5.0000V
0111 1111 1111	-0.0024V	+4.9976V
0000 0000 0000	-5.0000V	0

TABLE 3. PIN FUNCTION TABLE			
PIN	FUNCTION	PIN	FUNCTION
1	Bit 6	24	Bit 7
2	Bit 5	23	Bit 8
3	Bit 4	22	Bit 9
4	Bit 3	21	Bit 10
5	Bit 2	20	Bit 11
6	Bit 1 (MSB)	19	Bit 12 (LSB)
7	Strobe In	18	Digital Ground
8	+15V supply	17	+5V supply
9	-15V supply	16	-5V supply
10	Gain Adjust	15	Analog Ground
11	Offset Adjust	14	Feedback
12	Unipolar	13	V_{out}



Notes:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

FIGURE 4. DAC-02320 MECHANICAL OUTLINE (24 PIN DDIP)

ORDERING INFORMATION

DAC-02320-XXX

Linearity Grade:
- 3= 13 bit
- 2= 12 bit

Reliability Grade:
- 0= Standard DDC procedures.
- 1= Military processing available.*
- 2= Military processing available but without QCI testing.*

Operating Temperature Range (case):
- 1= -55°C to +125°C
- 3= 0°C to +70°C

*Consult factory for details.

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SECTION C
SAMPLE/HOLD and TRACK/HOLD AMPLIFIERS

C

PRODUCT SUMMARY TABLE

MODEL	ACQUISITION TIME (F.S.CHANGE)	LINEARITY ERROR	PACKAGE	APERTURE JITTER	SMALL SIGNAL BANDWIDTH	DROOP RATE	OPERATING TEMP. RANGE	POWER DISSIPATION	DESCRIPTION/ FEATURES	PAGE
TH-8530	10 nsec	±0.012% FSR	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.2"	20psec	100MHz typ	1.0m V/µs	-55°C to +125°C	1.9W	Includes buffer amplifier, 50 MHz sample rate. -60dB feedthrough.	C-5
THA-05203	150 nsec	±0.005% FSR	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.2"	50 psec	16MHz typ	0.5 µ V/µs	-55°C to +125°C	685mW	High speed and High accuracy. HTC-0300 and TP 4680 pin compatible. 74dB feedthrough.	C-9

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

BACKGROUND INFORMATION

INTRODUCTION

Sample/hold and track/hold amplifiers are used when the voltage level of a signal must be held or stored for a short period of time. A signal which varies rapidly may have to be held constant to allow time for an analog to digital or synchro to digital conversion to take place, or it may have to be stored while multiplexed signal channels are converted sequentially.

DDC's sample/hold and track/hold amplifiers are distinguished for their speed and low jitter. The new TH-8530 track/hold is in fact faster than any other track/hold or even sample/hold amplifier currently available. The DGL-13 track/hold falls into a different category. Designed for deglitching D/A converters, it has exceptionally low glitch and a preprogrammed hold time initated by an external strobe.

The main components of a S/H or T/H amplifier are shown in the simplified diagram of Figure 1. When the switch is closed the output signal follows the analog input, and when the switch is opened the output voltage is ideally fixed at the level of the input because it is stored on the holding capacitor. The difference between a S/H and T/H amplifier is that a sample/hold can only sample the input signal briefly, whereas a track/hold can track the input continuously. In a S/H the gate is AC coupled to the switch, and the switch can remain closed for only a brief time. In a T/H the gate is DC coupled to the switch, and the switch remains closed as long as the gate signal stays in the track mode.

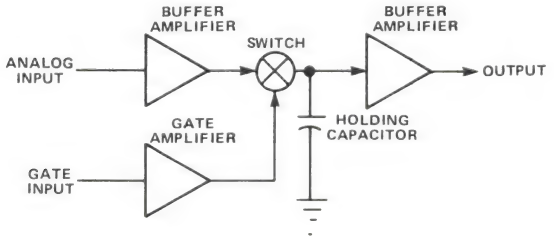


FIGURE 1. SIMPLIFIED DIAGRAM OF TRACK/HOLD OR SAMPLE/HOLD AMPLIFIER

The relationships between the output, input, and gate signals of a S/H or T/H amplifier are complex. In these devices there are delays between the gate signal changes and the opening or closing of the switch. Time is required for the output to settle, the output can have offsets and input signals can feed through to the output even when the switch is open. These effects are illustrated in Figure 2, and are discussed in the following sections.

TERMINOLOGY AND SIGNAL RELATIONSHIPS

The definitions which follow describe the key terms used to characterize S/H and T/H amplifiers. The terminology is depicted graphically in Figure 2.

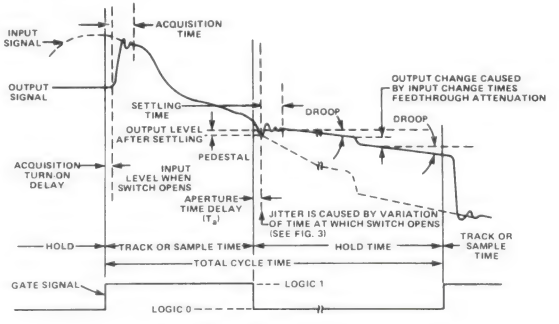


FIGURE 2. RELATIONSHIP OF OUTPUT, INPUT, AND GATE SIGNALS
(Assuming Gate Logic 0 = Hold)

A logic gate signal initiates the track or sample period. After this signal has been applied, the holding capacitor requires an interval of time called the Acquisition Time to charge to the point where it can track the input signal. The acquisition time depends on the magnitude of the voltage change required. It includes the Acquisition Turn-On Delay which is the time interval between application of the logic signal and the switch closure, plus in some cases output buffer activation time. The minimum track or sample period must be at least as long as the Acquisition Time.

When a signal is applied to the gate to initiate the hold period, there is a short delay, the Aperture Time Delay (T_a), before the switch opens to isolate the holding capacitor from the analog input. The delay itself can be compensated for, but the Aperture Time Delay Uncertainty (Jitter) associated with the delay can lead to errors, as shown in Figure 3.

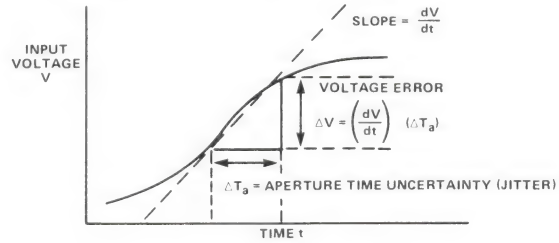


FIGURE 3. APERTURE TIME UNCERTAINTY ERROR (JITTER)

The time needed for the S/H amplifier output to settle out to the holding capacitor voltage after the gate changes from the sample mode to the hold made is the Settling Time, which includes the aperture time delay. Settling time is defined as the time required for an amplifier to settle to its final value ± a specified error band. If the output voltage is used at a shorter time interval after switching to the hold mode, errors will be introduced.

After the switch is opened and the output has settled, the output voltage generally increases or decreases linearly with time. This Droop is caused mainly by the bias current of the output buffer amplifier and by leakage through the switch. The bias current and leakage can be positive or negative. Droop can also be caused by leakage from the holding capacitor. The droop rate will determine how long a hold time can be tolerated to maintain the required accuracy.

When the switch opens after the sample period, any unbalanced charge in the switch is transferred to the holding capacitor, creating a small positive or negative step error, the Pedestal, in the output voltage during the hold period. The SH-8518 has the provision for fine trimming the pedestal error.

There will be a DC Offset or difference in DC voltage level between the input and output voltages of the S/H or T/H because of offset errors in the input and output amplifiers. Such a DC offset is present during both the track and the hold modes.

While the switch is open and the signal is being held, a step change in the input signal will still feed through the open switch capacitance to the output. The small output signal change which results is equal to the input voltage divided by the Feedthrough Attenuation of the open switch circuit.

SAMPLING RATE LIMITATIONS

The sampling rate is the rate at which an entire sample and hold cycle is completed.

$$\text{Sampling rate} = \frac{1}{\text{total cycle time}} = \frac{1}{\text{track (or sample) time + hold time}}$$

The maximum sampling rate is therefore determined by the minimum sample time plus minimum hold time. The minimum sample time is the acquisition time, while the minimum hold time will include the settling time plus whatever additional time is required for information processing.

A sample/hold amplifier has a minimum sampling rate as well as a maximum one. The minimum rate is determined by the maximum sample time plus the maximum hold time. The sample time has a maximum value (which should be specified) because the gate is AC coupled.

The hold time may also have a maximum value, because of droop. The output error will exceed the specified accuracy if the hold time is greater than the maximum error divided by the droop rate.

Droop may eventually cause the output voltage to exceed the limits of the specified output voltage range. The time to acquire a new signal may then exceed the specified acquisition time because of saturation effects.

C

ERROR CAUSED BY APERTURE TIME UNCERTAINTY

The uncertainty in the moment of time at which the signal is acquired and held (the aperture time jitter) causes an error whose magnitude depends on the rate at which the input is changing (Figure 3). The following discussion relates the maximum percent error in the output V caused by this effect with the aperture time uncertainty ΔT_a and the analog signal frequency f.

The error ΔV in the voltage is:

$$\Delta V = \left(\frac{dV}{dt}\right) \Delta T_a$$

For a sinusoidal signal, $V = V_o \sin (2 \pi ft)$

$$\Delta V = 2 \pi f V_o \cos (2 \pi ft) \Delta T_a$$

Since the maximum value of the cosine function is 1, the maximum percent error is:

$$\text{maximum \% error} = 100 \left(\frac{\Delta V}{V_o}\right) = 200 \pi (f)(\Delta T_a) = 628 (f) (\Delta T_a)$$

As an example, if the aperture time uncertainty is 500ps, then at a frequency of 0.5 MHz:

$$\text{maximum \% error} = (628) (0.5 \times 10^6) (500 \times 10^{-12}) = .16\%$$

This % error is the percentage of the maximum input signal amplitude, not the percentage of allowable full scale. Note also that if the input rate dV/dt is constrained only by slew rate limiting, then the maximum % error should be calculated directly as

$$\text{maximum \% error} = \frac{100}{V_o} \left(\frac{dV}{dt}\right)_{\text{max slew}} \Delta T_a$$

The error caused by aperture time uncertainty may be obtained from the nomograph in Figure 4 if the input signal is sinusoidal and the output is not slew rate limited. Any sloping straight line drawn on the nomograph from top to bottom relates the corresponding aperture uncertainty, percent error, and input frequency. As an example, suppose the maximum allowed error caused by aperture time is specified to be 0.1%, and the aperture time is 500 ps. A straight line drawn through these values on the nomograph intersects the frequency scale at about 300 KHz. This would be the highest input frequency consistent with a maximum error of 0.1%.

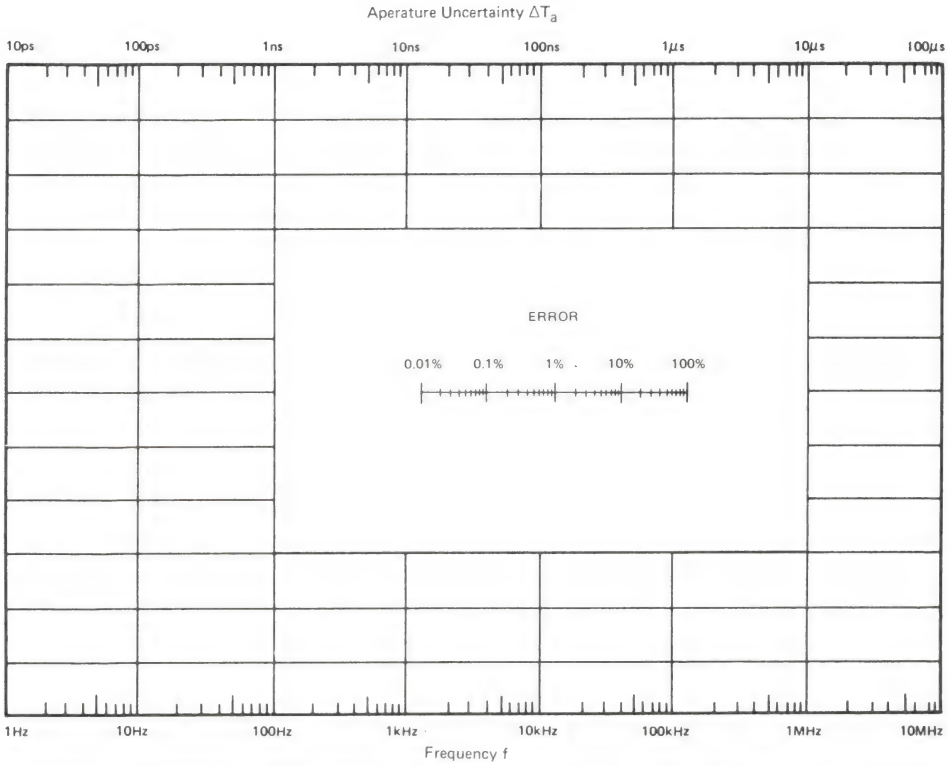


FIGURE 4. NOMOGRAPH FOR ERROR CAUSED BY APERTURE TIME UNCERTAINTY (JITTER)

The nomograph can also be used to show that voltage acquisition errors in the A/D converters can be greatly reduced if a track/hold amplifier precedes the converter. Assume an A/D converter with a conversion time of 2.2μs and an input with a maximum frequency of 20 KHz. In this situation the 2.2μs can be treated as an aperture time uncertainty. Connecting this with the 20 KHz frequency on the nomograph gives a maximum error of 28%. This error can easily be reduced by several orders of magnitude by a T/H or S/H whose aperture time uncertainty is much less than 2.2μs.

MATCHING A T/H OR S/H TO AN A/D CONVERTER

When a S/H or T/H amplifier is used at the input of an A/D converter, the performance of the system will depend on the combined specifications of both units, as well as on their compatibility.

Since the signal should be sampled at a frequency at least twice that of the maximum signal frequency, the maximum signal frequency is equal to one half of the maximum sampling rate of the system. As discussed in the section on Sampling Rate Limitations, the sampling rate of the system depends on the total cycle time. The cycle time is at least as long as the acquisition time + settling time + A/D conversion time, so

$$(f_{SIG})_{MAX} = \frac{1/2}{t_{Acquisition} + t_{Settling} + t_{A/D\ Conversion}}$$

The feedthrough attenuation of the S/H or T/H at f_{SIG} should represent less than 1/4 LSB of the A/D converter. For instance, suppose the converter has 8 bit resolution (1 LSB = 0.4%) and an 18 MHz clock rate. Then f_{SIG} is 9 MHz max, and at this frequency the S/H should have a maximum feedthrough attenuation of 0.1% (60 dB).

The acquisition time of the S/H or T/H is specified both for the magnitude of the input voltage change and for the percentage to which the final value will be accurate. The acquisition time should be specified both for a sufficiently large input voltage and for settling to within at least 1/2 LSB of the A/D converter.

Aperture time uncertainty (jitter) creates a sample to sample ambiguity in the output voltage when the S/H is processing high frequency signals. As shown in the previous section, the jitter time ΔT_a is related to the maximum percent error at a signal frequency f_{SIG} by:

$$\text{maximum \% error} = 628\ (f_{SIG})\ (\Delta T_a).$$

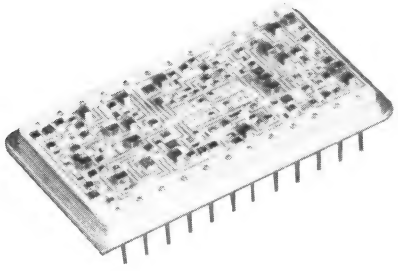
The maximum % error should be less than 1/2 LSB of the A/D converter, so the maximum uncertainty in the aperture time of the S/H or T/H should be:

$$(\Delta T_a)_{max} = \frac{1/2\ \text{LSB (expressed as a \%)}}{628\ (f_{SIG})}$$

See page N-19 for a list of Application Notes available from DDC.

TH-8530

VIDEO TRACK/HOLD HYBRID 10 NSEC ACQUISITION TIME 0.1% LINEARITY ERROR



FEATURES

- *20 PSEC APERTURE JITTER*
- *100 MHz BANDWIDTH*
- *50 MHz SAMPLING RATE*
- *9 NSEC SETTLING TIME*
- *-55°C TO +125° C OPERATING TEMPERATURE RANGE*
- *MIL-STD-883 SCREENING AVAILABLE*
- *ECL COMPATIBLE*

C

DESCRIPTION

The TH-8530 is a video speed track/hold amplifier packaged in a hermetic 24 pin DDIP. Its 10 nanosecond acquisition time to 0.1% of final value makes it the fastest track/hold of its type. With 0.1% linearity error and 100 MHz bandwidth, the TH-8530 is ideal for applications with sampling rates to 50MHz. For military requirements, models are available with -55°C to +125°C operating temperature range and screening in accordance with MIL-STD-883. Additional features include 9 nanosecond track-to-hold mode settling time, 1 millivolt per microsecond droop rate, and a slew rate of 400 volts per microsecond.

With its high speed and accuracy, wide operating temperature range, and small hermetic package, the TH-8530 is ideal for the most demanding military and commercial data acquisition requirements. Typical applications include pulse processing, radar and TV digitizing and very high speed instrumentation.

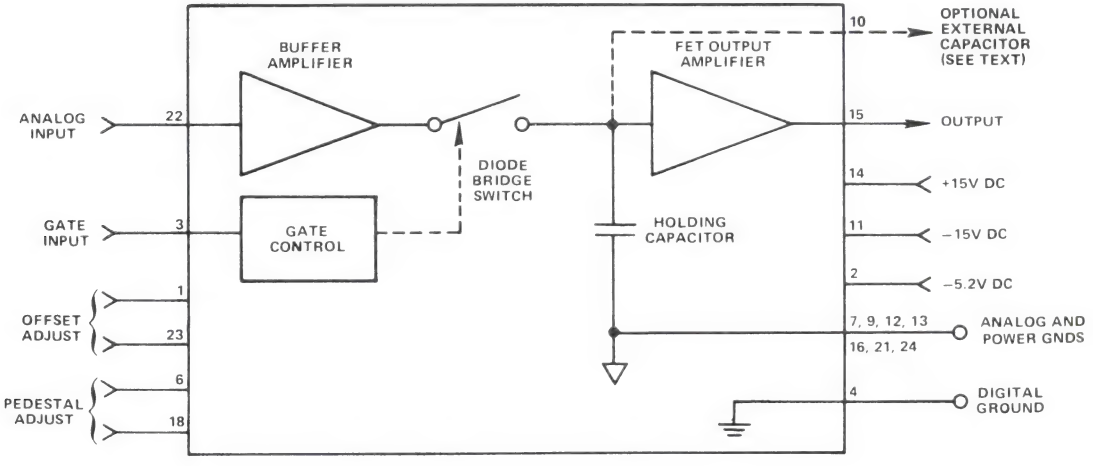


FIGURE 1. TH-8530 BLOCK DIAGRAM

TH-8530 SPECIFICATIONS At 25°C case temperature and rated supplies unless otherwise indicated.		
PARAMETER	**UNITS**	**VALUE**
ACCURACY		
Gain		
No load		+0.97 typ
With 200 Ω Rated Load		+0.95 typ; +0.92 min
Gain Tempco	ppm/°C	25 typ; 50 max
Linearity Error		
1mA max load	% of F.S.	0.012
At Rated Load	% of F.S.	0.2 max
Linearity Tempco	ppm/°C	5 typ; 15 max
Offset (1)	mV	25 typ; 100 max
(Trimmable to Zero)		
Offset Tempco (1)	mV/°C	0.2 typ; 0.5 max
Pedestal	mV	25 typ; 100 max
(Trimmable to Zero)		
Pedestal Tempco	μV/°C	60 typ; 150 max
DYNAMICS		
Small-Signal Bandwidth (f_t)	MHz	100 typ; 80 min
Slew Rate	V/μsec	400 min
Update Change	V	2 max
Max Sampling Rate (2)	MHz	50 typ; 33 min.
Min Cycle Time	ns	20 typ; 33 max
Aquisition Turn-On Delay	ns	3.5 typ; 7 max
Acquisition Time to 0.1% of Final Value		
2V Input Change	ns	10 typ; 15 max
0.2V Input Change	ns	5 typ; 8 max
Aperture Time Delay	ns	3.5 typ; 5 max
Aperture Time Uncertainty (Jitter)	ps	20 typ; 35 max
Feedthrough Attenuation in Hold Mode	dB	60 min through 10 MHz
Settling Time to 0.1% of Final Value (3)	ns	9 typ; 15 max
Droop Rate at 25°C (Case)	mV/μs	1 typ; 10 max
Droop Rate Vs. Temp		Doubles every 10°C
Glitch (From Track to Hold)		
Amplitude	mV	20
Duration	ns	15 (to less than 2mV)

TH-8530 SPECIFICATIONS CONTINUED		
PARAMETER	**UNITS**	**VALUE**
ANALOG INPUT		
Range For Rated Accuracy	V	±1 max
Absolute Max Without Damage	V	±2.5
Input Impedance	KΩ	100 typ; 20 min
Capacitance	pF	5 typ; 8 max
Bias Current	mA	±0.1 typ; ±0.5 max
GATE INPUT		
Type		ECL compatible (external pulldown req'd.)
Logic Levels	V	-0.8 = Logic 1 = Hold -1.6 = Logic 0 = Track
OUTPUT		
Voltage Range	V	±1 max
Steady State Current	mA	±5 max
Transient Current	mA	±50 max
Output Impedance	Ω	4 typ; 10 max
POWER SUPPLIES		
Supply Voltages	V	+15 -15 -5.2
Voltage Tolerance	%	±5 ±5 ±5
Absolute Max Voltage	V	+18 -18 -7
Current	mA	55typ 55typ 45typ 65max 65max 65max
Power Dissipation	W	1.9 average
TEMPERATURE RANGE [CASE]		
Operating		
—1 Option	°C	-55 to +125
—3 Option	°C	0 to +70
Storage	°C	-65 to +150
PHYSICAL		
Type		24 pin DDIP
Size	inch (mm)	1.4 x 0.8 x 0.2 (36 x 20.5 x 5)
Weight	oz (g)	.42 typ (11.9)

Notes:
(1) Measured during 50ns track time with input grounded.
(2) Sampling rate for 0.1% dynamic error.
(3) Settling time into Hold mode.

GENERAL

The TH-8530 track and hold amplifier (figure 1) includes a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltages are both buffered by amplifiers. The switch is controlled by an ECL logic gate signal which determines whether the holding capacitor voltage and output voltage will track the input signal (switch closed, logic 0) or will be held constant, retaining the value of the input at the moment the switch opens (switch open, logic 1).

The TH-8530 is available in several optional configurations. Provision for the use of an external holding capacitor has been made available on pin 10 (see Pin Connection Table). Because the external capacitor is connected in parallel with the internal capacitor, this option reduces the effects of droop and extends holding time. Acquisition time, however, is increased by the presence of additional capacitance created by this circuitry. This option is designated as "-10" when ordering the TH-8530 (see Ordering Information).

Unipolar voltage outputs may be ordered, which provide internal offsets of the specified ±1V input range. Option "P" produces 0 to +2V and option "N" produces 0 to -2V at the output (pin 15). A bipolar output range is available as option "B" (see Ordering Information).

TRIM ADJUSTMENTS

The offset and pedestal are trimmed at the factory to within the limits listed in the specifications table. Further adjustments may be made using the trim adjustments shown in figure 2. Connect the output (pin 15) to an oscilloscope and ground the analog input (pin 22). Apply a 50 nsec negative ECL pulse at a 1 MHz rate to the gate input. Vary the pedestal adjust potentiometer to minimize the pedestal and the offset potentiometer to trim the offset as shown in figure 3.

GROUNDING

To minimize coupling of a gate signal into an output signal, connect the gate signal ground to pin 4 only. Do not connect other grounds to pin 4. Analog input/output and supply voltage grounds can be connected to any of the analog

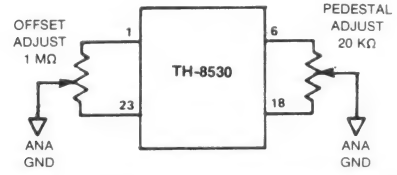


FIGURE 2. TRIM ADJUSTMENT CIRCUITS

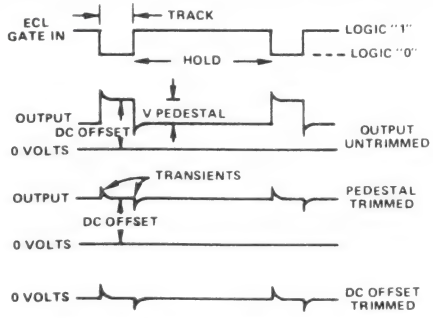


FIGURE 3. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

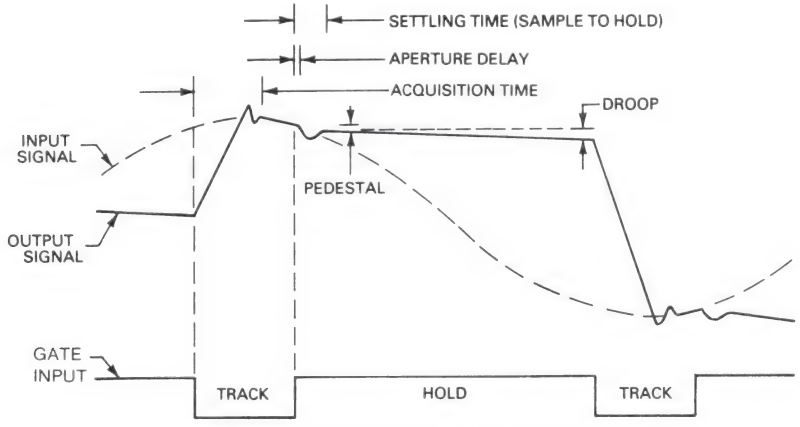


FIGURE 4. INPUT/OUTPUT CHARACTERISTICS

ground pins. The analog grounds are connected together internally and tied to the case. It is best to also connect these grounds together externally to minimize impedances. The analog and digital grounds are separated internally to avoid crosstalk between them and must be tied together externally.

Attention must be paid to proper high frequency grounding techniques in order to get the most performance from the TH-8530. It is highly desirable to use a large area ground plane under the track/hold. This will maintain a low impedance return path at all frequencies of interest. Each of the ground pins on the track/hold package must be connected to ground as close to the package as possible, in order to avoid voltage differences between the ground pins.

POWER SUPPLY DECOUPLING

The TH-8530 provides internal ceramic decoupling capacitors on the power supply lines. In most applications it is desirable to add external 1μf tantalum capacitors. These decoupling capacitors should be mounted as close as possible to the hybrid package to avoid high frequency power supply line drops.

INPUT/OUTPUT CHARACTERISTICS

As shown in the diagram of figure 4, the track interval is initiated when the Gate Input is brought LOW. The output slews as the hold capacitor is charged to a new value. Acquisition time is defined as the time required for the output to settle to within a given error band of its final value. Acquisition time for any interval depends on the magnitude of the voltage change since the last interval. The minimum track time must be at least as long as the acquisition time for the largest possible input change.

The hold interval is initiated when the Gate Input is brought HIGH. As shown in Figure 4, there is a short delay, the Aperture Delay, before the series switch opens to isolate the hold capacitor from the analog input. The uncertainty in this delay, called Aperture Jitter, causes an error in the output when the input slews fast.

After the Gate Input goes HIGH, a transient appears on the output due to charge transfer across the series switch. A Settling Time (Sample to Hold) interval elaspses before the output reaches a given error band of its final value. The track/hold output has not achieved rated performance until after this settling time interval has elapsed.

The charge transferred across the series switch onto the hold capacitor when the Gate Input goes HIGH causes a step error at the output. This Pedestal error is constant for every hold interval and does not vary with input voltage.

During the hold interval, the output voltage will increase or decrease linearly with time. This Droop error is caused by charging of the hold capacitor by bias current or series switch leakage current.

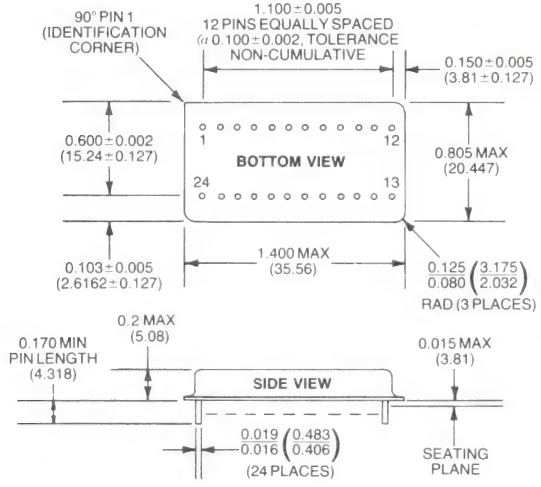
Another source of error, during the hold interval, is Feedthrough. Even though the series switch is open, fast slewing input signals can cause the output to change by voltage division across the open switch capacitance. The output error that results will be equal to the input voltage divided by the feedthrough attenuation.

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Offset Adjust	13	Analog Ground
2	—5.2 VDC	14	+15 VDC
3	Gate Input	15	Output
4	Digital Ground	16	Analog Ground
5	NC	17	NC
6	Pedestal Adjust	18	Pedestal Adjust
7	Analog Ground	19	NC
8	NC	20	NC
9	Analog Ground	21	Analog Ground
10	NC (See Note)	22	Analog Input
11	—15 VDC	23	Offset Adjust
12	Analog Ground	24	Analog Ground

Note: Pin 10 for external capacitor on special order only.

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



Notes:
(1.) Dimensions are shown in inches (millimeters).
(2.) Load identification numbers are for reference only.
(3.) Lead spacing dimensions apply only at seating plane.
(4.) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
(5.) Case tied to analog ground.

ORDERING INFORMATION

TH-8530 - 1 - B - 10 - 883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL- STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- 10 = Pin 10 connected to the holding capacitor.
  - Blank = No Connection.
- Output Voltage Range (all with ± 1V input):
  - B = -1V to +1V
  - N = 0 to -2V
  - P = 0 to +2V
- Temperature Range (Case):
  - -1 = -55°C to +125°C
  - -3 = 0°C to +70°C

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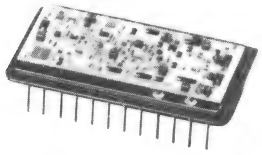
THA-05203

HIGH SPEED TRACK/HOLD HYBRID
150 nsec Acquisition Time
±0.005% Linearity Error



DESCRIPTION

The THA-05203 is a high speed, high accuracy track/hold amplifier packaged in a hermetic 24 pin DDIP. With its 150 nanosecond acquisition time to 0.01% for a 10 volt step, 0.005% linearity error, 60 picosecond aperture jitter and 74 dB feedthrough attenuation, the THA-05203 is ideal for use in digitizers with data throughput rates up to 5 MHz. Other performance features include −55°C to +125°C operating temperature range, ±10 volt input range, droop rate of 0.5 μV/μsec and small signal bandwidth of 16 MHz. The THA-05203 track/hold is pin for pin compatible with HTC-0300A and TP4860 type units, and offers comparable or superior performance for all parameters.

With its high performance, wide operating temperature range, and small hermetic package, the THA-05203 is ideal for the most demanding military and commercial data acquisition requirements. Typical applications include sonar and radar digitizing, medical and nuclear instrumentation and high speed waveform analyzers.

FEATURES

- *150 NSEC ACQUISITION TIME 10V STEP TO ±0.01% F.S.*
- *60 NSEC SAMPLE TO HOLD SETTLING TIME*
- *50 PSEC APERTURE JITTER*
- *74 dB FEEDTHROUGH ATTENUATION*
- *−55°C to +125°C OPERATING TEMPERATURE RANGE*
- *TTL COMPATIBLE*
- *HTC-0300A AND TP4860 PIN COMPATIBLE*

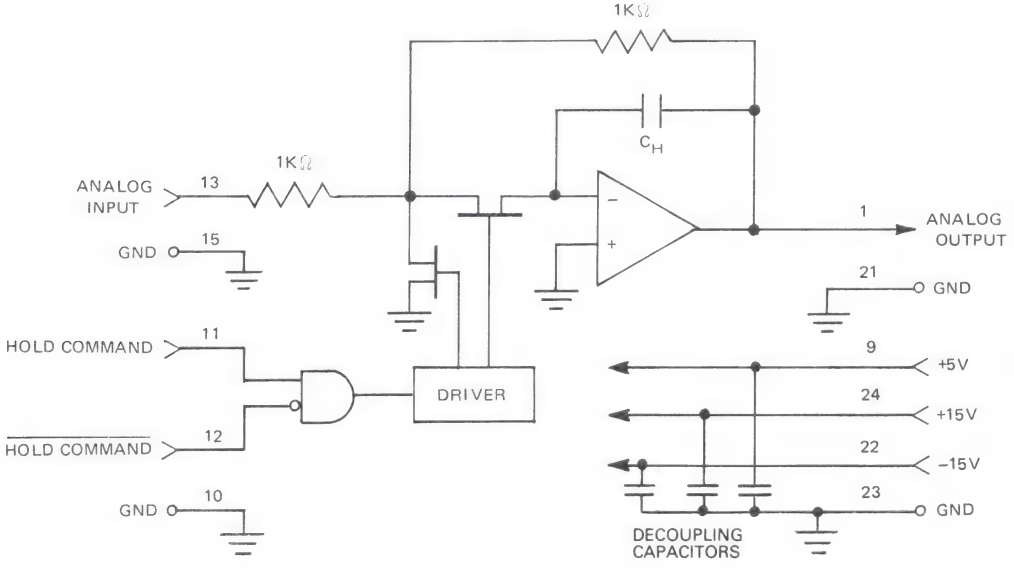


FIGURE 1. THA-05203 BLOCK DIAGRAM

SPECIFICATIONS

(At +25°C and nominal supply voltages unless otherwise noted)

PARAMETER	UNITS	VALUE	
ACCURACY			
Gain	V/V	−1.00 ±0.1% max	
Gain Tempco	ppm/°C	0.5 typ	5 max
Offset	mV	0.5 typ	5 max
Offset Tempco	ppm FSR/°C	3 typ	15 max
Linearity	% FS	0.005 typ	0.01 max
Pedestal (Hold Mode)	mV	2.5 typ	20 max
Pedestal Tempco	ppm FSR/°C	4 typ	
DYNAMIC CHARACTERISTICS			
Acquisition Time			
To 1% FS for 10V Step	nsec	90 typ	
To 0.1% FS for 10V Step	nsec	100 typ	170 max
To 0.01% FS for 10V Step	nsec	150 typ	200 max
Settling Time (Sample to Hold)			
To 0.1% FS	nsec	40 typ	
To 0.01% FS	nsec	60 typ	100 max
Aperture Jitter (RMS)	psec	50 typ	100 max
Aperture Delay	nsec	6 typ	
Feedthrough Attenuation			
DC to 2.5 MHz, 20V input	dB	74 typ	
Droop Rate			
+25°C	mV/usec	0.0005 typ	0.005 max
+70°C	mV/usec	0.015 typ	
+125°C	mV/usec	1 typ	
Bandwidth (3dB Small Signal)	MHz	16 typ	8 min
Slew Rate	V/usec	300 typ	150 min
Transient (Sample to Hold)	mV p-p	180 typ	
ANALOG INPUT			
Voltage Range	V	±11.5 typ	±10.25 min
Impedance	KΩ	1 typ	
DIGITAL INPUTS			
Logic Levels			
Logic "1"	V	+2.0 min	+5.0 max
Logic "0"	V	0 min	+0.8 max
Logic Loading	TTL	1 load typ	
ANALOG OUTPUT			
Voltage Range	V	±10.25 min	
Current[1]	mA	±50 max	
Impedance	Ω	0.1 typ	
Noise[2]	mV rms	0.1 typ	
Capacitive Load	pF	250 max	
POWER REQUIREMENTS			
Current Drain			
+15V Supply	mA	19 typ	25 max
−15V Supply	mA	21 typ	25 max
+5V Supply	mA	17 typ	25 max
Power Dissipation	mW	685 typ	875 max
Voltage Tolerance			
±15V	%	5 typ	
+5V	%	5 typ	
Power Supply Rejection Ratio	mV/V	±0.5 typ	
TEMPERATURE RANGE (Case)			
Operating			
−1 Option	°C	−55 to +125	
−3 Option	°C	0 to +70	
Storage	°C	−55 to +125	
PHYSICAL CHARACTERISTICS			
Package		24 pin DDIP	
Size	in (mm)	1.4x0.8x0.2 (36x20.3x5.1)	
Weight	oz (g)	0.4 (11.3)	

Notes:
(1) Output is short circuit protected to ground with a current limit of ±65 mA.
(2) Noise is specified in track mode with a 5 MHz bandwidth.

TECHNICAL DESCRIPTION

GENERAL

As shown in the block diagram of Figure 1, the THA-05203 consists of a unity gain inverting op amp with series and shunt switches at its summing point. Placing the track/hold in the track mode causes the series switch to close and the shunt switch to open. In the track mode, the analog output is an inverted version of the analog input. Placing the track/hold in the hold mode causes the series switch to open and the shunt switch to close. In the hold mode, the analog output is held constant by the hold capacitor at the value just prior to the series switch opening.

INPUT/OUTPUT CHARACTERISTICS

As shown in the diagram of Figure 2, the track interval is initiated when the HOLD COMMAND is brought LOW. The output slews as the hold capacitor is charged to a new value. Acquisition time is defined as the time required for the output to settle to within a given error band of its final value, after the HOLD COMMAND goes LOW. Acquisition time for any interval depends on the magnitude of the voltage change since the last interval. The minimum track time must be at least as long as the acquisition time for the largest possible input change. Figure 3 shows THA-05203 error versus acquisition time for a 10 volt input step.

The hold interval is initiated when the HOLD COMMAND is brought HIGH. As shown in Figure 2, there is a short delay, the Aperture Delay, before the series switch opens to isolate the hold capacitor from the analog input. The uncertainty in this delay, called Aperture Jitter, causes an error in the output when the input slews fast. Figure 4 shows aperture jitter error versus input slew rate, assuming 100 picosecond aperture jitter.

After the HOLD COMMAND goes HIGH, a transient appears on the output due to charge transfer across the series switch. A Settling Time (Sample to Hold) interval elapses before the output reaches a given error band of its final value. The track/hold output has not achieved rated performance until after this settling time interval has elapsed.

The charge transferred across the series switch onto the hold capacitor when the HOLD COMMAND goes HIGH causes a step error at the output. This Pedestal error is constant for every hold interval and does not vary with input voltage.

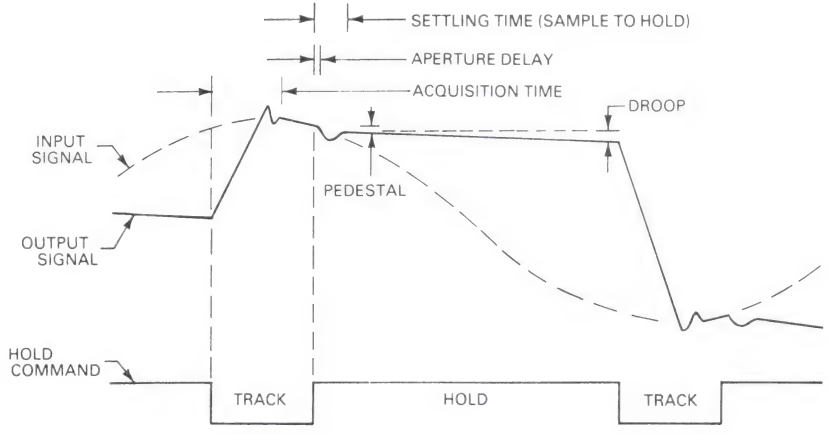


FIGURE 2. INPUT/OUTPUT CHARACTERISTICS

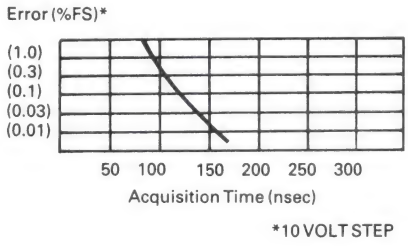


FIGURE 3. ERROR vs. ACQUISITION TIME

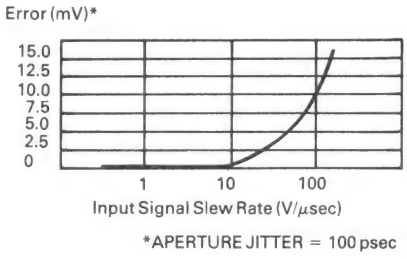


FIGURE 4. APERTURE ERROR vs. SLEW RATE

During the hold interval, the output voltage will increase or decrease linearly with time. This Droop error is caused by charging of the hold capacitor by op amp bias current or series switch leakage current.

Another source of error, during the hold interval, is Feedthrough. Even though the series switch is open, fast slewing input signals can cause the output to change by voltage division across the open switch capacitance. The output error that results will be equal to the input voltage divided by the feedthrough attenuation.

APERTURE ERROR

A track/hold is used with an A/D converter to keep the ADC input constant during the conversion interval. This is because converter input must vary no more than ½ LSB during the conversion time to maintain its accuracy.

The highest allowable frequency, while maintaining less than ½ LSB variation at the A/D converter input, can be calculated with and without the use of a track/hold. The dramatic increase in allowable input frequency when a track/hold is used illustrates why most applications use a track/hold and ADC combination.

The following example assumes a 10 volt sinusoidal input to a 12 bit 2μsec A/D converter, and calculates the frequency at which a ½ LSB change occurs during the aperture interval. With no track/hold, the aperture interval is equal to the ADC conversion time. With a track/hold, the aperture interval is equal to the aperture jitter time.

$$V_{in} = 10 \sin 2\pi ft$$

$$\frac{dV_{in}}{dt} = 20\pi f \cos 2\pi ft$$

$$\left.\frac{dV_{in}}{dt}\right|_{max} = 62.8\, f_{max}$$

$$f_{max} = \frac{2.5 \times 10^{-3}\ \text{volt}}{(62.8)\ (\text{Tap})}$$

For no track/hold: $\text{Tap} = 2 \times 10^{-6}$ sec

$f_{max} = 20\,\text{Hz}$

For track/hold: $\text{Tap} = 50 \times 10^{-12}$ sec

$f_{max} = 800\,\text{KHz}$

OUTPUT LOADING

Attention must be paid to the resistive and capacitive loading of the THA-05203 to maintain desired performance. Capacitive loads above 50pf will affect track/hold acquisition and settling time. Capacitive loads above 250pf are to be avoided, since the potential for oscillations will result. The recommended resistive load is 500 ohms or higher. Resistive loads as low as 250 ohms may be used, but at this load the potential exists for current limiting non-linearities.

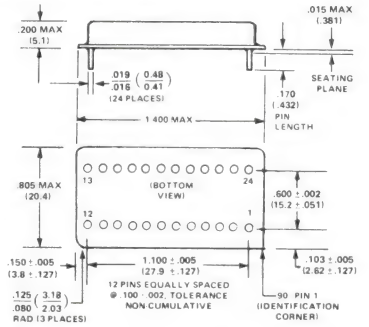
GROUNDING

Attention must be paid to proper high frequency grounding techniques in order to get the most performance from the THA-05203. It is highly desirable to use a large area ground plane under the track/hold. This will maintain a low impedance return path at all frequencies of interest. Each of the 4 ground pins on the track/hold package must be connected to ground as close to the package as possible, in order to avoid voltage differences between the ground pins.

POWER SUPPLY DECOUPLING

The THA-05203 provides internal ceramic decoupling capacitors on the +5 volt and ±15 volt power supply lines. In most applications it is desirable to add external 1μF tantalum capacitors. These decoupling capacitors should be mounted as close as possible to the hybrid package to avoid high frequency power supply line drops.

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches (millimeters)
2. Lead identificattion numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements MIL-STD-202E, Method 208C

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Analog Output	24	+15V Supply
2	N/C	23	Ground
3	N/C	22	−15V Supply
4	N/C	21	Ground
5	N/C	20	N/C
6	N/C	19	N/C
7	N/C	18	N/C
8	N/C	17	N/C
9	+5V Supply	16	N/C
10	Ground	15	Ground
11	$\overline{\text{Hold Command}}$	14	N/C
12	$\overline{\text{Hold Command}}$	13	Analog Input

ORDERING INFORMATION

THA-05203−100

Reliability Grade:
- 0 = Standard DDC procedures.
- 1 = Fully compliant with MIL-STD-883.
- 2 = Screened to MIL-STD-883 but without QCI testing.

Operating Temperature Range:
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

SECTION D
STANDARD MIL-DWGS and U.S. NAVY SEMs

PRODUCT SUMMARY TABLE

• *STANDARD MIL-DWGS* **			
MIL-DWG (DESC) #	**FEATURES**	**MODEL**	**PAGE**
5962-86049-02ZC	Monolitic Transceivers.	**BUS-63105 II**	D-2
5962-87535-01XC	MIL-STD-1553 dual redundant RT includes transceivers, encoder/decoder and protocol.	**BUS-65112**	
5962-87579-02XC	Dual reduntant monolithic transceivers in a single-hybrid.	**BUS-63125 II**	
5962-87632-01XC	Complete dual redundant RT and is a pin-for-pin and Functional BUS-65112 Replacement.	**BUS-65111**	
5962-87687-01XC	14 Bit Monolithic hybrid S/D and R/D tracking converter.	**HSDC-8920**	
5962-88517-01XC	14 bit deglitched D/A.	**DAC-02310**	
5962-88542-01XC	Track hold and A/D converter.	**ADC-00300**	
5962-88585-01XC	Dual reduntant MIL-STD-1553 BC, RT, and MT.	**BUS-65600**	
5962-88586-01XC	MIL-STD-1553 to microprcessor interface.	**BUS-66300 II**	
5962-88692-01XC	MIL-STD-1553 Dual Redundant RT/BC/MT Advanced Integrated MUX (AIM) Hybrid.	**BUS-61553**	
5962-89499-01XC	Military grade synchro or resolver input.	**SDC-14560**	

• *U.S. NAVY SEMs* **		
MODEL	**FEATURES**	**PAGE**
SEM PRODUCTS	Hybrid and discrete SEM products. Module qualification: JAN and special. Special (custom designs). Fuctions provided: Analog-to-Digital Converters. Synchro-to Digital Converters, tracking. Two-speed Synchro-to-Digital Converters. Synchro-to-Digital Converters, multiplexed. Digital-to-Resolver Converters. Scott-T Transformers. Solid-state Control Transformers (CT). Reference Isolation Transformers. MIL-STD-1553 Remote Terminal Unit. MIL-STD-1553 BUS Controller. MIL-STD-1553 RT Protocol. MIL-STD-1553 RT/BC/MT & 1750A CPU. Filters Geometric Analog-to-Digital Converters. Power Amplifiers.	D-3

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

**Variations and peculiarities exist — consult factory.

STANDARD MIL-DWGS

Using the **DESC** (Defense Electronics Supply Center) military drawing numbers listed below presents a considerable advantage to the designer in that the lengthy approval cycles for non-standard parts can be bypassed. For additional information about these products and a copy of DDC's newest MIL-STD-1553 Designer's Guide contact the DDC office nearest you.

MIL-DWG (DESC) #	Features	Model
5962-86049-02ZC	Monolitic Transceivers. Conforms to MIL-STD-1553A/B. High S/N ratio, internal filtering.Drives Harris 15530 directly. SEAFAC tested. +5V and -15Vdc operation.	**BUS-63105 II**
5962-87535-01XC	MIL-STD-1553 dual redundant RT includes transceivers, encoder/decoder and protocol. Supports 13 mode codes and has DMA type interface handshake. SEAFAC tested (15V operation).	**BUS-65112**
5962-87579-02XC	Dual reduntant monolithic transceivers in a single-hybrid. Conforms to MIL-STD-1553 A/B. High S/N ratio, internal filtering. Drives Harris 15530 directly. Complete isolation, including separate power and signal connections. SEAFAC tested.	**BUS-63125 II**
5962-87632-01XC	Complete dual redundant RT packages in either DDIP or Flatpack hybrid packages. Includes two low power transceivers, two bit processors. RT protocol, data buffers, timings control logic, supports 13 mode codes, and is a pin-for-pin and Functional BUS-65112 Replacement.(12V operation)	**BUS-65111**
5962-87687-01XC	14 Bit Monolithic hybrid S/D and R/D tracking converter. 10 RPS tracking, low power, 3-state latched outputs, accuracy of ± 0.9LSB standard, ± 2.6 min high-accuracy option, usable as control transformer, and inhibit does not interrupt tracking.	**HSDC-8920**
5962-88517-01XC	14 bit deglitched D/A with 10 MHz update rate, programmable output range, and 10 mVpp.	**DAC-02310**
5962-88542-01XC	Track hold and A/D converter. Very high speed. -55°C to + 125°C operation. Linearity Error (Max) of +0.0025% FSR, Conversion Time of 0.5µs.	**ADC-00300**
5962-88585-01XC	Dual reduntant MIL-STD-1553 BC, RT, and MT. Provides 16 bit tri-state parallel data bus and DMA handshaking for microprocessor compatibility. Supports all dual reduntant mode codes along with externally selectable illegal codes. DDIP & Flat Package.	**BUS-65600**
5962-88586-01XC	MIL-STD-1553 to microprcessor interface. Compatible with Motorola, Intel, and Zilog CPUs Off-loads 1553 I/O capability; compatible with DDC's BUS-65600 and 65112. Operates over full military temperature range. DDIP & Flat Package.	**BUS-66300 II**
5962-88692-01XC	MIL-STD-1553 Dual Redundant RT/BC/MT Advanced Integrated MUX (AIM) Hybrid including microprocessor interface and 8K × 16 RAM. DDIP & Flat Package.	**BUS-61553**
5962-89499-01XC	Military grade synchro or resolver input. Synthesized reference. Programmable resolution and track-like velocity input.	**SDC-14560**

HYBRID AND DISCRETE SEM PRODUCTS
JAN Qualified Modules for Navy SEM Program

DESCRIPTION

The product assurance program, facilities, and manufacturing procedures of ILC Data Device Corporation have been certified by the U.S. Navy for the production of JAN qualified modules for the Standard Electronic Module (SEM) program. Various standard DDC synchro and other data conversion products and a number of custom designed products have been adapted to SEM configuration with an assigned Key Code, as shown in the table. For these units to which an M28787 slash number has been assigned, DDC either has been JAN certified and is a QPL supplier, or is in the process of obtaining JAN certification. Consult the DDC factory for the most recent JAN certification status. Units listed in the table without M28787 numbers are some of the "special SEMs" which DDC has qualified.

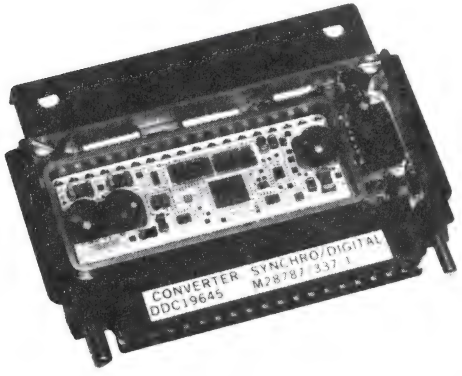
DDC's proven expertise in meeting SEM program requirements, its extensive experience in the design and manufacture of data conversion products, and its sophisticated hybrid capability are available for the creation of new SEM designs. The SEM modules shown in the table are able to implement complex functions such as single and dual speed synchro-to-digital tracking converters, multiplexed synchro-to-digital converters, and digital-to-synchro converters.

The Naval Avionics Center (NAC) in Indianapolis, Indiana has prepared applications data manuals for synchro SEM modules with assigned SEM part numbers. These manuals are available to SEM users call (317) 353-3808.

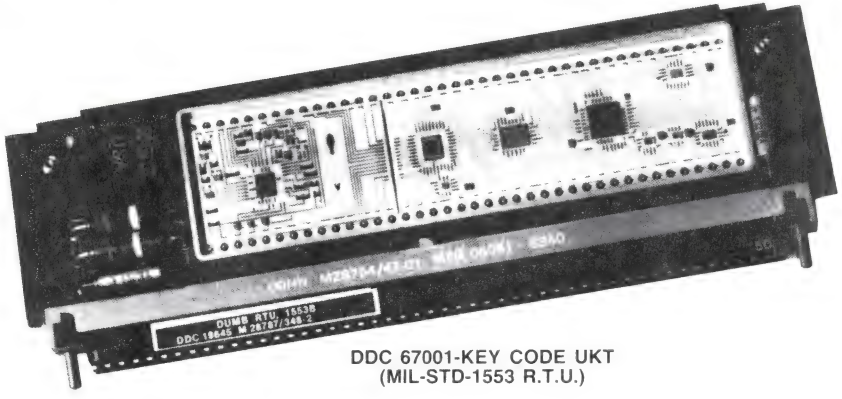
FEATURES

- *FACILITY CERTIFICATION BY N.W.S.C. CRANE, INDIANA*
- *MODULE QUALIFICATION – JAN AND QUALIFIED SPECIAL*
- *SPECIAL CUSTOM DESIGNS*
- *CAPABILITIES: S/D, D/S, A/D. D/A, DATA BUS, CUSTOM FILTERS, CUSTOM HYBRIDS*

D



DDC 9200-KEY CODE JWP
(14 BIT S/D CONVERTER)



DDC 67001-KEY CODE UKT
(MIL-STD-1553 R.T.U.)

DDC P/N	Closest DDC Standard Product	Function	SEM Part No. M2878/XXX †	Key Code	Module Size
BUS-67001	Custom Product	MIL-STD-1553B Interface Unit	/348	UKT	2A(1)
BUS-67002	Custom Product	MIL-STD-1553B Protocal and Subsystem	/349	UKU	2A(1)
BUS-67003	Custom Product	MIL-STD-1553B Bus Controller	/367	UKS	2A(1)
BUS-67005-600	Custom Product	MIL-STD-1553 Dual Redundant Interface	Special	AAJH	2A(2)
SEM09000-600	ADH-8516-1	12 bit, 3usec A/D Converter with Buffer (+/-10V Input)	Special	DRG	1A
SEM09001-601	Custom Product	Sonar Filter	Special	DE5	1A
SEM18004-301	Custom Product	60-400Hz 14 bit R/D Converter with Tri-state Data	Special	NKP	1A
SEM18005-600	Custom Product	400Hz 14 bit R/D Converter with Tri-state Data	Special	EER	1A
SEM18005-601	Custom Product	400Hz 14 bit S/D Converter with Tri-state Data	/345	JAP	1A(1)
SEM18007-600	Custom Product	5VA 4 Channel D/S Converter	Special	ADSA	2A(3)
SEM88000-600	Custom Product	Selectable Bandpass Filter	Special	BYQ	2A
SEM88000-601	Custom Product	Selectable Bandpass Filter	Special	BYK	2A
SEM88000-602	Custom Product	Selectable Bandpass Filter	Special	BYP	2A
9200	Monobrid S/D	60-400Hz 14 bit S/D Converter with Tri-state Data	/337	JWP	1A
9201	H & HMSDC-Series	Dual Power Amplifier	/184	SES	1C
9202	H & HMSDC-Series	Scott-T and Reference Transformer-Input/Output	/185	STT	1C
9203	HXDC-10-6H-1	60Hz 10 bit S/D Converter	Special	KMJ	1A(4)
9204	HRCT-14-L-1-A/+HDP-6-1	400Hz 14 bit R/D Converter	Special	KMR	IB
9205	H & HMSDC-Series	Two-Speed Error Crossover Switch/Detector	/225	HUH	1A
9207	HXDC-10-6-1	10 bit S/D Converter	Special	HLD	1A
9208	HXDC-10-4-1	10 bit S/D Converter	Special	KMK	1A
9210	H & HMSDC-Series	MSB Function Generator	/186	SHY	1A
9220	H & HMSDC-Series	LSB Function Generator	/187	SHU	1A
9225	SC8711-1	4 Channel MUX Synchro/Sine-Cos	Special	PMK	1A(4)
9241	H & HMSDC-Series	Octant/Quadrant Detector	/188	SHV	1A
9250	H & HMSDC-Series	Error Detector	/189	SHX	1A
9251	H & HMSDC-Series	60 Hz Reference Input Processor-Transformer	Special	JMC	1B
9253	BUS-8553-1 & BUS-8937-1	MIL-STD-1553 BUS Adaptor (R.T.U.)	Special	MAN	2A(1)
9271	H & HMSDC-Series	60 HZ Input Processor-Transformer	Special	JMB	1C
9280	HSCT-14-L-1	Solid State Control Transformer	Special	KMP	1A(4)
9281	HSCT-14-H-1	Solid State Control Transformer	Special	KME	1A(4)
9286	HXCT-14-1	Solid State Control Transformer	Special	KMD	1A
9288	HDP-4-1	400Hz Error Processor	Special	KMF	1A
9289	HDP-6-1	60Hz Error Processor	Special	KMG	1A
9290	Custom Product	60-400Hz Scott-T and Reference Transformer	Special	HLC	1B
9291	HCCT-14-1	400Hz 14 bit Solis State Cosine Control Transformer	Special	KMQ	1A
9293	HRDC-14-1	14 bit D/R Converter	Special	KMM	1A
9297	Custom Product	Geometric A/D Converter	Special	CA4	2A
9299	HSDC-10-4H-1	400Hz 10 bit S/D Converter	Special	KMH	1A(4)
9300	Custom Product	12 bit A/D Converter	/232	QQQ	1B
9401	H & HMSDC-Series	Quadrant Selector and Successive Appoximation Logic	NAVALEX0104-925	KMA	1C
9450	H & HMSDC-Series	Reference Input Processor-Transformer	NAVALEX0104-925	KMB	IB
9470	H & HMSDC-Series	Synchro Input Processor-Transformer	NAVALEX0104-925	KMC	IB
9900	ADH-8516-1	12 bit, 3usec A/D Converter with Buffer (+/-5V Input)	Special	UFU	1A

NOTES: (1) Configuration is Format B (ISEM)
(2) Configuration is Format C
(3) Configuration is Format D
(4) Includes Solid State Scott-T
(5) All units with MIL-M-28787 part number are presently JAN or in process of being qualified
† For modules other than "Special" refer to MIL-STD-1634 and M28787 for detailed information.

ORDERING INFORMATION

9205-HUH-M28787/225

- MIL part no. (where applicable)
- Key Code
- DDC part number

D

SECTION E
SYNCHRO AND RESOLVER TO DIGITAL (S/D, R/D) CONVERTERS

PRODUCT SUMMARY TABLE

• *SINGLE-SPEED TRACKING*

	MODEL	RESOLUTION	ACCURACY	TRACKING RATE	PACKAGE	DESCRIPTION/FEATURES	PAGE
	HSDC-8915 Monobrid Series	14 Bit	to ± 2.6'	10 rps	36 Pin DDIP 0.79 x 1.9 x 0.2"	Low power S/D. 3-state output, tracks during output inhibit. LSI based hi-rel. All common inputs. Can operate as CT.	E-6
	RDC-19200 Monobrid Series	10, 12, 14, or 16 Bit	± 10' to ± 2' + 1 LSB	3.2 to 800 rps	40 Pin TDIP 1.14 x 2.02 x 0.23"	R/D(sine and cosine) conversion. Pin programmable for 10, 12, 14, or 16 bit resolution. Bandwidth and scalable Velocity Output voltage. Features BIT and LOS outputs. 2 and 11.8 Vrms inputs. Inductrosyn compatible.	E-16
*	**RDC-19220 Series**	10, 12, 14, or 16 Bit	to ±2.3'	to 2300 rps	28 Pin DDIP 1.4 x 0.6 x 0.2" 40 Pin DDIP 2.0 x 0.6 x 0.2"	Low cost, monolithic programmable Resolver and LDVT to Digital converter with tach grade velocity output. Available in military and industrial models.	E-36
	SDC-630	10 Bit	± 21'	50 rps	2.6 x 3.1 x 2.6" Module	Low profile, transformer isolated, industry standard pin out. 47 Hz to 1000 Hz.	E-57
	SDC-632	12 Bit	± 8.5'	40 rps	2.6 x 3.1 x 0.4" Module	Low profile (0.4) industry standard. All common inputs. Transformer isolation.	
	SDC-634	14 Bit	to ± 2.6'	10 rps	2.6 x 3.1 x 0.4" Module	Low profile (0.4) industry standard. All common inputs. Transfomer isolated.	
	SDC-14531II Series	14 or 16 Bit	to ± 1.3'	0.61 to 10 rps	36 Pin DDIP 1.9 x 0.78 x 0.21" Hybrid	Low cost, high reliability synchro or resolver to digital converter. Built-in-test (BIT). Internal Synthesized Reference, and single 5V power supply.	E-61
	SDC-14532 Series	12 or 14 Bit	± 8.5' or ± 5.3'	12 to 48 rps	32 Pin TDIP 1.74 x 1.14 x 0.28"	Low cost programmable R/D converter. It has CT Mode capability, three-state latched outputs, and the inhibit does not interrupt tracking.	E-72
*	**SDC-14545 Series**	13 Bit	± 8'	5 rps	24 Pin DDIP 1.3 x 0.77 x 0.21"	Small, S/D only converter with unique open line detector. Available in military and commercial grades.	E-77
*	**SDC-14550 Series**	10,12,14, or 16 Bit	to ± 2.3'	0.5 to 160 rps	34 Pin 1.0 x 0.78 x 0.21"	Small, +5V only S/D or R/D. 16 Bit parallel data, BIT, and velocity. Available in military and commercial grades.	E-79
	SDC-14560 Series	10,12,14, or 16 Bit	± 6' to ± 1' + 1 LSB	0.61 to 160 rps	36 Pin DDIP 1.9 x 0.78 x 0.21"	Military grade synchro or resolver input. Synthesized reference. Programmable resolution and tack-like velocity output. Packaged in a hermetic case. Can operate as CT.	E-85
*	**SDC-14570/75 Series**	14/16 Bit	to ± 2.3'	to 10 rps	1.0 x 0.8 x 0.2"	Small, low cost converters with tachometer quality velocity output.	E-93
*	**SDC-14580 Series**	10, 12, 14, or 16 Bit	to ± 1.3'	0.61 to 10 rps	36 Pin DDIP 1.9 x 0.78 x 0.21" Hybrid	Low cost, high reliability synchro or resolver to digital converter. Built-In-Test (BIT), Wide Bandwidth, High Carrier Freq (1-3kHz), and Internal Synthesized Reference.	E-97
*	**SDC-14600/05 Series**	14/16 Bit	to ± 2.3'	to 10 rps	28 Pin DDIP 1.5 x 0.8 x 0.2"	Low cost dual channel S/D converters with tachometer quality velocity output.	E-112
*	**SDC-14610/15 Series**	14/16 Bit	to ± 2.3'	to 10 rps	36 Pin DDIP 1.9 x 0.8 x 0.2"	Low cost triple channel S/D converters with tachometer quality velocity output.	E-116
*	**SDC-14620**	10,12,14, or 16 Bit	to ± 2.3'	0.5 to 160 rps	54 Pin 1.5 x 0.78 x 0.21"	Small, dual channel +5V only S/D or R/D. 16 Bit parallel data, BIT, and velocity. Available in military and commercial grades.	E-120
	SDC-14700	5 decades	± 0.03°	180°/sec	3.1 x 2.6 x 0.4"	0.01° synchro or resolver to BCD converter.	E-126
	SDC-19204 Monobrid Series	10,12,14, or 16 Bit	± 8' to ± 2' + 1 LSB	2.5 to 160 rps	40 Pin TDIP 2.0 x 1.1 x 0.23"	Low cost. Programmable resolution and BW. Velocity output eliminates tach.	E-128

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

Synchro Products continued.

* New Product

PRODUCT SUMMARY TABLE (continued)

	MODEL	RESOLUTION	ACCURACY	TRACKING RATE	PACKAGE	DESCRIPTION/FEATURES	PAGE
	• *MULTI-SPEED TRACKING*						
	SDC-361	16 Bit	± 1 LSB	1000°/sec	2.6 x 3.1 x 0.8" Module	1x, 36x 2 speed S/D. Transformer isolated, broadband 47 Hz to 3000 Hz. All common inputs.	E-53
	SDC-362	16 Bit	± 1 LSB	1000°/sec	2.6 x 3.1 x 0.8" Module	1x, 18x 2 speed S/D. Transformer isolated, broadband 47 Hz to 3000 Hz. All common inputs.	
	• *MULTIPLEXED INPUT*						
	MODEL	**RESOLUTION**	**ACCURACY**	**FREQ.**	**PACKAGE**	**DESCRIPTION/FEATURES**	
	HMSDC-8700	14 Bit	±4.6' ±1/2 LSB	—	36 Pin DDIP 1.9 x 0.79 x 0.21" (x2)	Two hybrids or encapsulated modules are used for a 4-channel, multiplexed system. The two packages consist of a central converter and an input processor which accepts four signal channels and one reference channel. Multiple input processors can be accommodated with one central converter. 150 µsec conversion time per channel. Simultaneous sampling and random accessing. All common L-L voltages and frequencies.	E-8
	MSDC-700	14 Bit	±4.6' ±1/2 LSB	—	2.6 x 3.1 x 0.4" (x2 Module)		
	• *REFERENCE OSCILLATORS*						
	OSC-15801	—	—	400Hz - 20kHz	1.0 x 0.8 x 0.2"	Synchro/Resolver/Inductosyn reference oscillator and has quadrature ref. output voltages (two outputs 90° out of phase) with programmable output freq. (400Hz - 20kHz).	E-10
*	OSC-15802	—	—	400Hz - 10kHz	1.0 x 0.8 x 0.2"	ADI alternate source, similar to OSC-15801.	E-13
	REF-15001 Series	—	—	2.5kHz or 10kHz	1.52 x 1.78 x 0.35"	Synchro/Resolver/Inductosyn reference oscillator. 2.5 kHz or 10 kHz for high-speed applications. Provides pin programmable AC reference for 11.8V, 4.4V,or 2.0V.	E-48
*	REF-15003/4	—	—	to 10kHz	6.0 x 3.0 x 1.4"	15VA programmable power oscillator.	E-51

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

* New Product

BACKGROUND INFORMATION

INTRODUCTION

DDC's synchro-to-digital and resolver-to-digital converters employ the latest in component and circuit technology and represent a significant improvement in performance and reliability over former units.

From a systems engineer's standpoint, outstanding performance features have been incorporated into these units. They are designed for printed circuit board mounting by hand soldering or flow soldering techniques. Each unit is fully trimmed and tested before leaving the factory. DDC builds hundreds of synchro converters each month, making shipments from stock a common occurrence.

THEORY OF OPERATION

Theory of operation is explained for DDC's discrete and hybrid tracking synchro-to-digital converters. The same principles apply to the resolver-to-digital converters except that the angular analog data input is in 4-wire resolver form rather than 3-wire synchro. Synchro or resolver angle data is proportional to the ratio of line-to-line amplitudes across the terminals. These line-to-line amplitudes vary as the shaft angle is changed. The angle information is converted from synchro format, (see Figure 1A), i.e., Sin θ cos ωt, sin $(\theta + 120^\circ)$ cos ωt, sin $(\theta + 240^\circ)$ cos ωt, to resolver format, (see Figure 1B), i.e., sin θ cos ωt and cos θ cos ωt, by the Scott "T" Transformer,

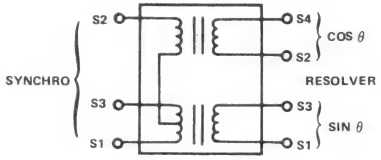
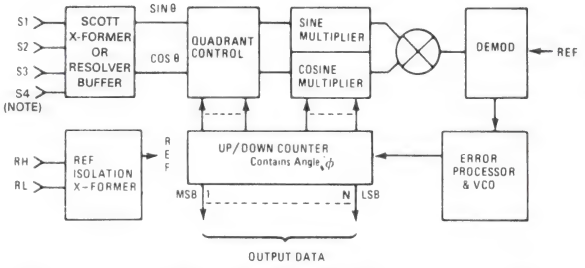


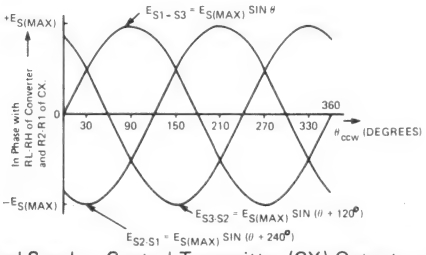
FIGURE 2. SCOTT "T" TRANSFORMER



Note: Use S1, S2, S3 and S4 for resolver inputs, or S1, S2 and S3 only for synchro inputs.

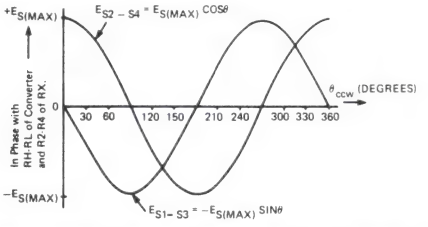
FIGURE 3. BLOCK DIAGRAM SYNCHRO-DIGITAL CONVERTER

(A)



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ)

(B)



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 1. SYNCHRO AND RESOLVER SIGNALS

shown in Figure 2. In a synchro transmitter, RH-RL corresponds to R1-R2, and in a resolver RH-RL corresponds to R2-R4. Note that all converters use resolver format internally. The carrier, cos ωt, is of minor importance to this discussion and will be dropped from the notations hereafter. As shown in the block diagram of Figure 3, the converter performs the following trigonometric computation:

$$\text{Sin}\,(\theta - \phi) = (\text{Sin}\,\theta \cos\phi - \cos\theta \sin\phi).$$

In this expression, θ represents the input data angle and ϕ represents the angle contained in the up-down binary counter. The error function, sin $(\theta - \phi)$, is processed and controls the up-down counter in such a manner that at null, $\theta = \phi$. The converter includes a dual integration, making it a Type II servo loop and hysteresis function to eliminate the one or two bits of "hunting" otherwise present in a Type II servo loop. Prior to the counter being updated due to an input data change, a "converter busy" signal is generated. When it returns to normal, the data may be frozen by activating the "inhibit" control line and transferring the data simultaneously. It is important to realize that one advantage of a tracking converter is that the output data is always fresh and always available. There are no errors due to velocity lags or minor varitions in synchro carrier amplitudes or power supply voltage.

SYNCHRO AND RESOLVER TO DIGITAL CONVERTERS

The loop dynamics of DDC's tracking S/D converters are described by the unity feedback configuration shown in Figure 4. The closed-loop transient response is nominally critically damped, and the parameters A and B for each S/D converter can be requested from the applications engineering group at DDC if they are not listed in the product section of this catalog.

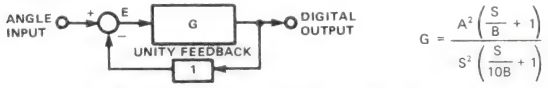


FIGURE 4. S/D CONVERTER LOOP DYNAMICS

APPLICATIONS

For all of DDC's synchro converters, the input synchro signals are connected to S1, S2 and S3. Input resolver signals are connected to S1, S2, S3, and S4. The conventions are shown in Figure 5. These signals are applied to an input Scott "T" transformer or a resolver isolation transformer. Application of DC voltages, or AC voltages other than those intended, may damage this transformer. The same is true with regard to the reference signal applied to RH and RL. Also, careful attention must be given to making the proper electrical connections. Reversal or misapplication of power supplies can result in damage to the converter.

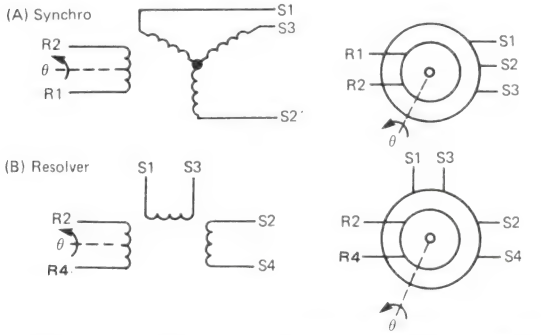


FIGURE 5. SYNCHRO AND RESOLVER CONVENTIONS

MULTIPLEXED S/D CONVERTER SYSTEMS

Multiplexed S/D converter systems differ from tracking type converters for two reasons: they have multiple inputs rather than one, and they use a successive approximation conversion technique rather than a Type II tracking loop. The heart of the system is the central converter, which consists of one or more modules. Added to this are input circuits for each channel which transform the synchro information to resolver format. The reference carrier is monitored and when a peak is detected, the sin and cos (resolver) levels of all channels are sampled and held as DC information. One channel is now selected and the central converter is started. A successive approximation technique is used by the central converter to determine the status of each digital bit, one at a time, starting with the most significant bit (MSB) and ending with the least significant bit (LSB).

The central converter uses a solid state control transformer whose inputs are θ (the analog input angle) and ϕ (the digital angle in the output register). The output from the solid state CT is sin $(\theta - \phi)$, the same form as an electromechanical CT. The converter operates on this signal to reduce it to a minimum, thus making θ equal to ϕ. Since only n trials are needed to resolve 2^n different levels, relatively fast S/D conversions can be made in this fashion.

MULTISPEED S/D CONVERSION

The operation of a two speed S/D is essentially the same as a single speed tracking S/D, except there are two solid state CTs generating two error voltages. These two CTs are driven from a single up/down counter. One CT is referred to as the coarse CT and the other is called the fine CT. Digital information from the counter to the fine CT is multiplied by the speed ratio between the two (for example, 36X). A cross-over switch selects which CT error signal is fed to the error processor. Assuming an off-null condition, the cross-over switch feeds the coarse CT error to the error processor. The converter seeks a null in the same manner described for a single speed S/D. As a null is approached, the coarse CT error voltage drops below a preset limit and the cross-over switch automatically switches over to the fine CT error voltage to feed into the error processor. Since the counter angle θ is multiplied by the speed ratio, the gradient of the fine CT error voltage is multiplied by the same amount. The tracking loop is now able to seek an even finer null, using the fine error voltage, and will switch back to the coarse error voltage only if the preset theshold is exceeded. In order to eliminate false nulls 180 degrees away from the true null, a digital offset and a "stickoff" voltage are introduced in the coarse channel.

ACCURACY TESTS

Because of the high accuracy of DDC's S/D converters, only laboratory-grade synchro or resolver substitution boxes or standards should be used. If synchro standards are not available, arrangements may be made to witness the final source inspection at the DDC factory.

Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14 LSB	0.0220	1.32

FIGURE 6. BIT WEIGHT TABLE

Figure 7 shows how to arrange test equipment for measuring the accuracy of S/D converters. A separate lamp driver or suitable readout is required for each of the output data lines. The synchro standard is set to any desired test angle, and the lamps which are on are added according to their bit weights (see Figure 6) and compared with the test angle.

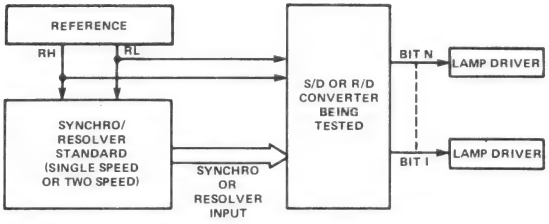


FIGURE 7. ACCURACY TEST CIRCUIT

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc. Appropriate handling procedures should be used in order to prevent damage to CMOS circuits.

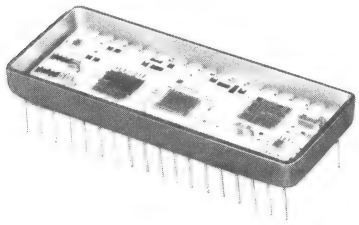
It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

See page N-19 for a list of Application Notes available from DDC.

DDC
ILC DATA DEVICE CORPORATION

HSDC-8915 MONOBRID® SERIES*

14 BIT MONOLITHIC HYBRID S/D AND R/D TRACKING CONVERTERS



FULL DATA SHEET AVAILABLE

DESCRIPTION

The HSDC-8915 Monobrid® Series is the first complete 14-bit synchro-to-digital or resolver-to-digital converter contained in a single hybrid module. Most of its circuitry has been incorporated into a custom designed monolithic chip, thereby greatly reducing parts count inside the hybrid. The Monobrid combination of monolithic and hybrid technologies allows a more sophisticated design with better performance and additional features to fit inside a standard 36 pin DDIP hybrid package. Power consumption is reduced, reliability is increased, and costs are lower.

New features found in the HSDC-8915 Series are 3-state output in two bytes, and a transparent latch which allows the converter to keep tracking even while an Inhibit is being applied. Innovative features found in other recent DDC hybrid converters are also included, such as a ±2.6 minute high accuracy option, analog velocity signal, error voltage outputs, solid state signal and reference isolation, broadband input, and accommodation to non-standard line-to-line voltage levels.

The HSDC-8915 Series is available in two accuracy grades: ±4 minutes ±0,9 LSB and ±2,6 minutes. The accuracy is not affected by carrier amplitude variation because the conversion is ratiometric. Phase sensitive detection in the error loop rejects quadrature and noise. Adjustments and calibration are never required.

The HSDC-8915 Series accepts broadband inputs: 360 to 1000 Hz or 47 to 1000 Hz. Two kinds of input signal isolation are available: internal differential solid state input with high common mode rejection, and transformer isolation with external transformers. Output angle is natural binary code, parallel positive logic, and TTL/CMOS compatible. Synchronization to a computer is complete via a Converter Busy output and an Inhibit input.

Only one main power supply is required. Its +15V DC nominal level can range from +11 to +16.5 volts with no degradation in performance. The HSDC-8915 is also connected to the external logic power supply. Internal logic is CMOS, and all logic inputs and outputs are buffered to the external logic level. TTL or any external CMOS logic level between +4.5V and the +15V supply level can be accommodated.

APPLICATIONS

With three-state output and an Inhibit that does not stop the tracking process, HSDC-8915 Series converters are especially suited for bus multiplexing and interfacing with microprocessors. These converters are ideal for remotely located and hard to access equipment where low power requirements, small size, and high MTBF are critical. All units are processed to MIL-STD-883. They are well suited to the most stringent and severe industrial or military and avionics applications. In conjunction with other devices, they are easily adapted for closed loop control.

Designed for printed circuit board mounting by standard techniques, the HSDC-8915 Series can be readily incorporated into other equipment by the OEM user. Because of their low cost, they are competitive with discrete S/D converters in many applications.

FEATURES

- *10 RPS TRACKING*
- *LOW POWER:*
  150 mW, Typical
- *ACCURACY:*
  ±4 minutes ±0.9 LSB standard
  ±2.6 minutes high accuracy option
- *3-STATE LATCHED OUTPUTS FOR MICROPROCESSOR DATA BUS*
- *USABLE AS CONTROL TRANSFORMER (CT)*
- *INHIBIT DOES NOT INTERRUPT TRACKING*
- *LOGIC:*
  TTL and CMOS compatible 14 bit parallel binary angle
  Converter Busy and Inhibit
  Enable lines for 3-state output

*Patented

Note: Monobrid® is a registered trademark of ILC Data Device Corporation.

RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations and susceptibility information are available on request.

ORDERING INFORMATION

1. Converters may be ordered as follows.

HSDC - 8915 –1 –a –883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883
  - B = Screened to MIL-STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- Accuracy:
  - Blank = ±4 minutes ±0.9 LSB (Standard)
  - a = ±2.6 minutes max. (High Accuracy)
- Operating Temperature Range:
  - 1 = –55°C to +125°C
  - 3 = 0°C to +70°C
- Input Type:
  - Voltage Follower Buffer (requires external signal conditioner such as an isolation transformer):
    - 8915 = 400 Hz
    - 8916 = 60 Hz
  - Solid State Synchro (direct input):
    - 8917 = 400 Hz, 11.8V L-L
    - 8918 = 400 Hz, 90V L-L
    - 8919 = 60 Hz, 90V L-L
  - Solid State Resolver (direct input):
    - 8920 = 400 Hz, 11.8V L-L
    - 8921 = 400 Hz, 26V L-L
    - 8922 = 400 Hz, 90V L-L

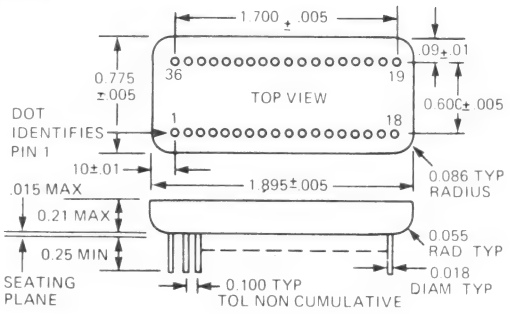
2. Reference and signal transformers for the voltage follower buffer input converters must be ordered separately as follows:

Type	Frequency	Ref. Voltage	L-L Voltage	Part Numbers: Ref. Xfmr.	Part Numbers: Signal Xfmr.
Synchro	400 Hz	115V	90V	21049	21045*
Synchro	400 Hz	26V	11.8V	21049	21044*
Resolver	400 Hz	115V	90V	21049	21048*
Resolver	400 Hz	26V	26V	21049	21047*
Resolver	400 Hz	26V	11.8V	21049	21046*
Synchro†	60 Hz	115V	90V	24133-1	24126-1
				24133-3	24126-3

*The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

†60 Hz synchro transformers are available in two temperature ranges:
1 = –55°C to +105°C
3 = 0°C to +70°C

MECHANICAL OUTLINE
36 PIN DOUBLE DIP *



NOTES

1. Dimensions shown are in inches.
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

*Flatpack available, consult factory.

PIN CONNECTION TABLE

PIN	FUNCTION: Solid St. Resolver	FUNCTION: Solid St. Synchro	FUNCTION: Volt. Fol. Buffer	PIN	FUNCTION
1	S1	S1	N.C.	19	RH (Ref. High)
2	S2	S2	COS	20	RL (Ref. Low)
3	S3	S3	SIN	21	N.C.
4	S4	N.C.	N.C.	22	ξ (Filtered DC Error Out)
5	Bit 1 MSB			23	θ (Analog Velocity Out)
6	Bit 2			24	CB (Converter Busy)
7	Bit 3			25	$\overline{EN\ 7\text{-}14}$ (Enable, Bits 7 to 14)
8	Bit 4			26	$\overline{EN\ 1\text{-}6}$ (Enable, Bits 1 to 6)
9	Bit 5			27	e (AC Error Out)
10	Bit 6			28	V_L (Logic Voltage Input)
11	Bit 7			29	GND
12	Bit 8			30	$\overline{S}$
13	Bit 9			31	Ge (Gain Control)
14	Bit 10			32	+15V (Power Supply In)
15	Bit 11			33	INH (Inhibit)
16	Bit 12			34	V (Internal DC Ref.)
17	Bit 13			35	BC (Buffered Cos)
18	Bit 14 LSB			36	BS (Buffered Sin)

NOTES

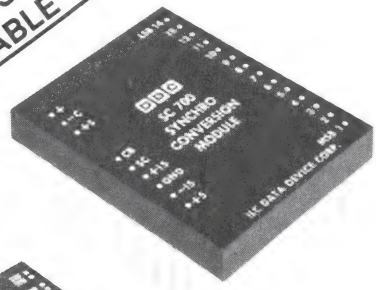
BS and BC pins are used in other applications.

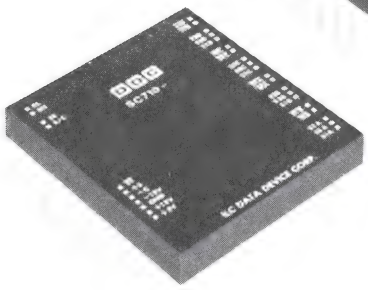
DDC
ILC DATA DEVICE CORPORATION

MSDC-700/HMSDC-8700

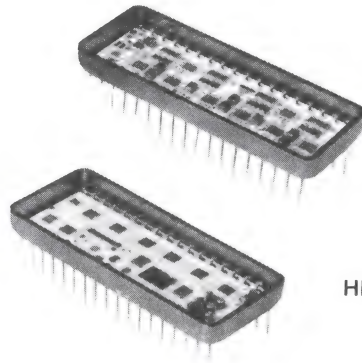
MULTIPLEXED 14 BIT S/D AND R/D CONVERTERS
New Design Requires Fewer Modules

FULL DATA SHEET AVAILABLE





MSDC-700



HMSDC-8700

FEATURES

- *SIMULTANEOUS SAMPLING AND RANDOM ACCESS*
- *SUPERIOR ALGORITHM GIVES INHERENTLY HIGH ACCURACY*
- *ONLY TWO TYPES OF MODULES 4 channel input module and central converter*
- *MODULES AVAILABLE IN DISCRETE OR HYBRID FORM*

DESCRIPTION

These two new series of multiplexed S/D and R/D converters are cost effective because they require fewer components and interconnections. Since each input module contains four signal channels, and the central converter is complete in one module, a 4 channel system can be made with only two modules. All common synchro and resolver line-to-line voltages and frequencies are available, and signal and reference input channels can be interconnected in any combination.

Discrete and hybrid modules can be used together because they are electrically interchangeable. Modules in the discrete MSDC-700 series are low profile (0.43 inch high) and low cost. They feature internal isolation transformers at both 60 Hz and 400 Hz. Modules in the hybrid HMSDC-8700 series have the small size, low weight, and high reliability of thick-film hybrids. They feature differential solid-state signal and reference inputs with substantial common mode rejection so that transformer isolation is not usually required.

APPLICATIONS

Multiplexed S/D and R/D converters can be used when multiple synchro or resolver inputs are sampled for digital computation or display, and real time tracking is not required. Multiplexing is found in data logging systems, process monitors, ordnance aiming controls, navigation systems, numerical control, and range instrumentation. The synchro and resolver inputs often represent variables which are analyzed by a computer for monitoring or control.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

PIN CONNECTION TABLES FOR HYBRID MODULES

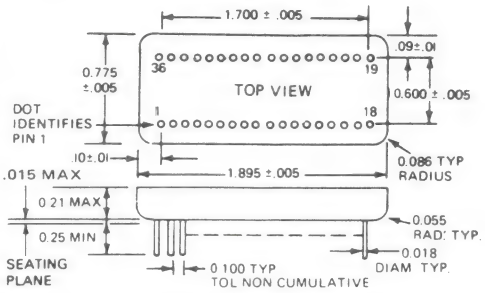
1. PIN CONNECTION TABLE FOR CENTRAL CONVERTER: SC-8700

Pin	Name	Description	Pin	Name	Description
1	B1	14 Bit Outputs	20	-C	-COS input. Connect to -C outputs on all input modules.
2	B2				
3	B3				
4	B4		21	+S	+SIN input. Connect to +S outputs on all input modules.
5	B5				
6	B6				
7	B7		22	CB	Converter busy output
8	B8		23	SC	Start conversion input
9	B9		24	TP4	(+5.6) Factory test point
10	B10		25	TP6	(e) Factory test point
11	B11		26	NC	No connection
12	B12		27	+	No connection if unused
13	B13		28	NC	No connection
14	B14		29	TP8	Factory test point
15	NC	No connection	30	TP9	(T) Factory test point
16	TP1	(+BC) Factory test points	31	+5V	Power supply connections
17	TP3	(-BS) Factory test points	32	-15V	Power supply connections
18	TP2	(-BC) Factory test points	33	TP7	(E) Factory test point
19	AG	Analog GND (Must be connected to pin 34)	34	GND	Power supply and logic GND
			35	TP5	Factory test point
			36	+15V	Power supply connection

2. PIN CONNECTION TABLE FOR INPUT MODULES: SC-8710 TO SC-8714

Pin	Name	Description	Pin	Name	Description
1	S1A	Synchro or resolver input A. S4 for Resolver only.	21	NC	No connection
2	S3A		22	+5V	Power supply connections
3	S4A		23	-15V	
4	S2A		24	GND	
5	S1B	Synchro or resolver input B. S4 for resolver only.	25	+15V	
6	S3B		26	$\overline{STD}$	Sample time inputs and MUX select lines for inputs A, B, C, and D. Connect sample time inputs to any appropriate ST output.
7	S4B		27	$\overline{MD}$	
8	S2B		28	$\overline{STC}$	
9	S1C	Synchro or resolver input C. S4 for resolver only.	29	$\overline{MC}$	
10	S3C		30	$\overline{MB}$	
11	S4C		31	$\overline{STB}$	
12	S2C		32	$\overline{STA}$	
13	S1D	Synchro or resolver input D. S4 for resolver only.	33	$\overline{MA}$	
14	S3D		34	+S	+SIN output. Connect to +S input on central converter module.
15	S4D				
16	S2D				
17	RH	Ref input high	35	-C	-COS output. Connect to -C input on central converter module.
18	RL	Ref input low			
19	SE	Sample enable input. No connection if unused.	36	S/C	SIN/COS select input. No connection if unused.
20	$\overline{ST}$	Sample time output. Connect to sample time inputs on any module.			

MECHANICAL DIAGRAM FOR ALL HYBRID MODULES (SC 8700, SC 8710 – SC 8714)



PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING
PINS ARE KOVAR WITH GOLD PLATING (50 μINCH MIN)
CASE IS ELECTRICALLY FLOATING

ORDERING INFORMATION

Each module required is specified separately. Modules are called out with temperature range as follows:

SC 8710 – 1 – 883B

- Reliability Grade: (Applies to hybrid modules only.)
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL- STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- Temperature Range (Operating):
  - 1 = −55°C to +105°C
  - 3 = 0°C to +70°C
- Module Number:
  - 700 Series = Discrete encapsulated modules
  - 8700 Series = Hybrid modules

Each system requires the following:

1. Central Converter. Order one of the following:
   Discrete: SC 700.

   Hybrid: SC-8700

2. Signal Input Module. Order one or more of the following:

Input Type	L-L Voltage	Discrete Module No.	Discrete Frequency	Hybrid Module No.	Hybrid Frequency
Synchro	11.8V	SC 710	360-440 Hz	SC 8710	47-440 Hz
Synchro	90V	SC 711	360-440 Hz	SC 8711	47-440 Hz
Synchro	90V	SC-715*	47-440 Hz	–	–
Resolver	11.8V	SC 712	360-440 Hz	SC 8712	47-440 Hz
Resolver	26V	SC 713	360-440 Hz	SC 8713	47-440 Hz
Resolver	90V	SC 714	360-440 Hz	SC 8714	47-440 Hz

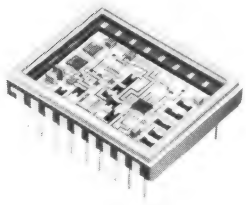
*The SC-715 module may be used at 400 Hz by interconnecting the SC-711 sample time outputs ($\overline{ST}$) to the desired SC-715 sample time inputs ($\overline{STA}$, $\overline{STB}$, $\overline{STC}$ and $\overline{STD}$).

D-ABR

DDC
ILC DATA DEVICE CORPORATION

OSC-15801

SYNCHRO/RESOLVER/INDUCTOSYN® REFERENCE OSCILLATOR



FEATURES

- *QUADRATURE REFERENCE OUTPUT VOLTAGES FOR INDUCTOSYN APPLICATIONS*
- *PROGRAMMABLE OUTPUT FREQUENCY FROM 400 Hz TO 20 KHz*
- *SMALL 18 PIN DDIP*
- *SCALEABLE REFERENCE OUTPUT*
- *-55°C TO +125°C OPERATING TEMPERATURE RANGE*

DESCRIPTION

The OSC-15801 is a quadrature power oscillator with two outputs 90° out of phase. These outputs provide both the reference and quadrature signals simultaneously, making the OSC-15801 ideally suited for Inductosyn applications.

With the use of two capacitors, the oscillator's outputs are pin programmable in frequency down from 20 KHz to 400 Hz. The Reference output voltage is 8.8Vrms at 20 KHz and can be scaled down with a single resistor.

Packaged in an 18 pin hermetic DDIP, the OSC-15801 operates over a temperature range of -55°C to +125°C making it an excellent choice for Inductosyn applications.

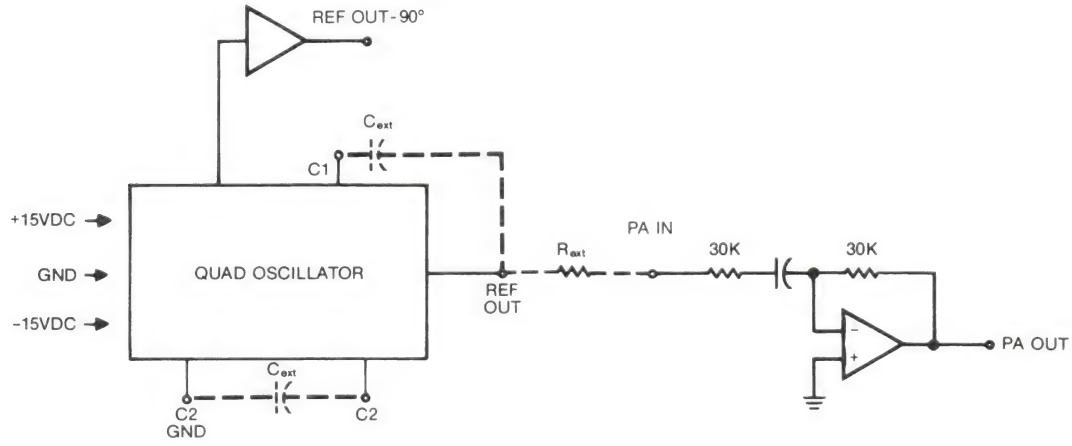


FIGURE 1. OSC-15801 BLOCK DIAGRAM

®Inductosyn is a registered trademark of Farrand Controls Corporation.

TABLE 1. OSC-15801 SPECIFICATIONS		
Specifications apply over temperature range and power supply range.		
PARAMETER	**UNITS**	**VALUE**
FREQUENCY	Hz	Programmable from 400 to 20K
OUTPUTS (Note 1)		
PA OUT		
Voltage	Vrms	7.1 to 8.8
Current	mA rms	215 min
REF		
Voltage	Vrms	7.1 to 8.8
Current	mA rms	3 min
REF -90°		
Voltage	Vrms	(Note 2)
Current	mA rms	3 min
Protection		short circuit and transient proof
POWER SUPPLIES		
Voltage	VDC	±15 ±5%
Current	mA	10 max plus load current
Maximum Voltage without damage	VDC	±18
TEMPERATURE RANGE		
Operating		
-10X	°C	-55 to +125
-30X	°C	0 to +70
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in (mm)	1.0 x 0.8 x 0.2 (25.45 x 20.32 x 4.83) 18 pin DDIP
Weight	oz (gm)	0.4 (1)

Notes:
1. Output voltage tracks ±15V supply levels.
2. Clipped sine wave for demodulator drive only, 10Vrms typ.

OSC-15801 OPERATION

PROGRAMMABLE FREQUENCY OUTPUT

The output frequency of the OSC-15801 is programmable from 20 KHz down to 400 Hz. The frequency is programmed using two external equal value capacitors (see figure 2). The value of the capacitors (Cext) is calculated as follows:

$$Cext = (2{,}400{,}000/f) - 100$$

Where: C is capacitance in picofarads
f is frequency in Hertz

PROGRAMMABLE REFERENCE VOLTAGE OUTPUT

The PA OUT (REF), pin 13, provides from 7.1V to 8.8V rms, depending on the operating frequency. Table 2 lists the PA OUT voltages at the (programmed) operating frequency. These voltages are the maximum voltages obtained at these frequencies, with Rext = 0 Ohms (pin 7 jumped to pin 3).

TABLE 2. PA OUT/FREQUENCY	
PA OUT	**FREQUENCY**
8.8 Vrms	20KHz
7.5 Vrms	10KHz
7.1 Vrms	.4KHz

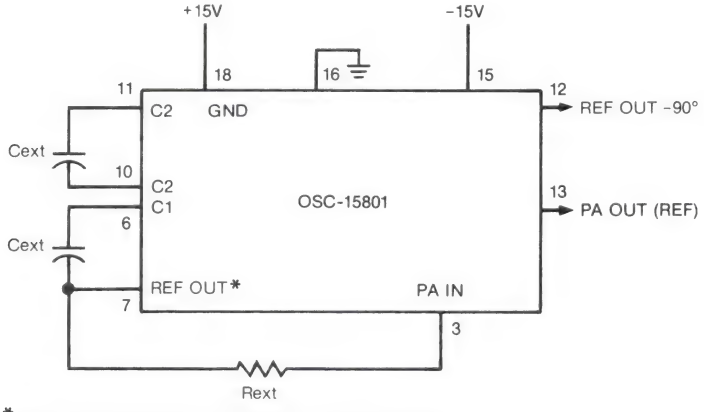
To scale down the PA OUT voltage, an external resistor (Rext) is connected between pins 3 and 7. The value of Rext is calculated as follows:

$$Rext = 30\ [(PA\ OUT/desired\ voltage) - 1]$$

Where: Rext is in K Ohms.
desired voltage is in Vrms.
PA OUT is dependent on frequency used.

FOR EXAMPLE, to scale down PA OUT to 5Vrms at 10KHz the value of Rext would be calculated as follows:

$$Rext = 30\ [(PA\ OUT/desired\ voltage) - 1]$$
$$Rext = 30\ [(7.5/5) - 1]$$
$$Rext = 15K$$



* Pin 7. REF OUT is the unbuffered output of oscillator.

FIGURE 2. PROGRAMMING RESISTOR AND CAPACITOR CONNECTIONS

TABLE 2. OSC-15801 PIN FUNCTIONS

PIN	NAME	FUNCTION
1	NC	No connection.
2	NC	No connection.
3	PA IN	Power Amplifier inverting input.
4	NC	No connection.
5	NC	No connection.
6	C1	Capacitor connection for pin programmable frequency.
7	REF OUT	Reference output.
8	NC	No connection.
9	NC	No connection.
10	C2	Capacitor connection for pin programmable frequency.
11	C2 GND	Capacitor connection for pin programmable frequency.
12	REF OUT -90°	-90° reference output signal.
13	PA OUT	Power Amplifier output.
14	NC	No connection.
15	-15V	-15VDC power supply voltage.
16	GND	Ground
17	NC	No connection.
18	+15V	+15VDC power supply voltage.

ORDERING INFORMATION

OSC-15801-300

Reliability Grade:

0 = Standard DDC processing

1 = Fully compliant with MIL-STD-883C, including full QCI testing.

2 = Screened to MIL-STD-883 but without QCI Testing.

Temperature:

1 = -55°C to +125°C

3 = 0°C to +70°C

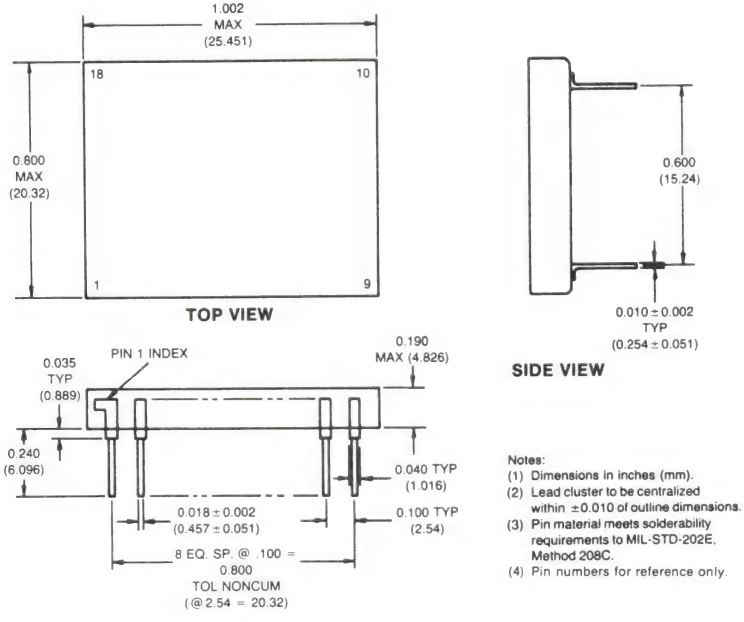
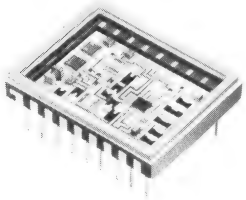


FIGURE 3. OSC-15801 MECHANICAL OUTLINE

OSC-15802

SYNCHRO/RESOLVER/INDUCTOSYN® REFERENCE OSCILLATOR



NEW

DESCRIPTION

The OSC-15802 is a quadrature power oscillator with two outputs 90° out of phase. These outputs provide both the reference and quadrature signals simultaneously, making the OSC-15802 ideally suited for synchro, resolver, LVDT (RVDT), and Inductosyn applications.

With the use of two capacitors, the oscillator's outputs are pin programmable in frequency to 10 kHz. The Reference output voltage is 7V rms and can be scaled down with a single resistor.

APPLICATIONS

Packaged in an 18 pin hermetic DDIP, the OSC-15802 operates over a temperature range of -55°C to +125°C making is an excellent choice for synchro, resolver, LVDT (RVDT), and Inductosyn applications.

FEATURES

- ***ADI Alternate Source***
- ***Quadrature Reference Output Voltages for Inductosyn Applications***
- ***Programmable Output Frequency to 10 kHz***
- ***Small 18 Pin DDIP***
- ***Scaleable Reference Output***
- ***-55°C to +125°C Operating Temperature Range***

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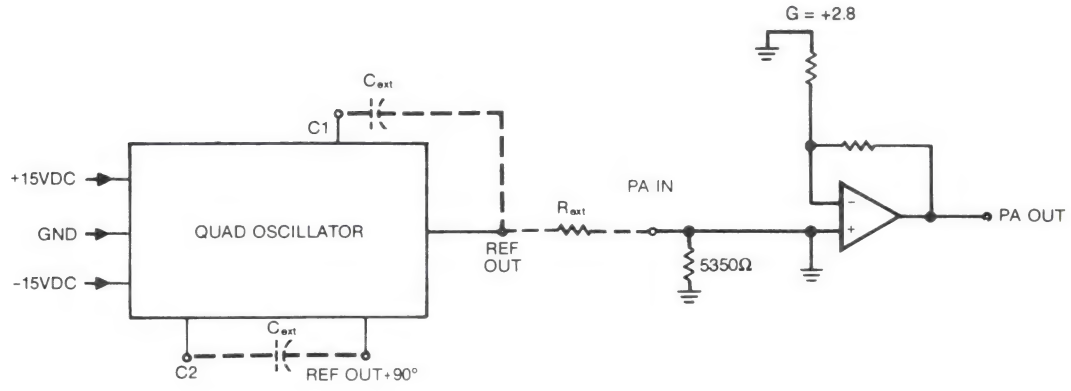

FIGURE 1. OSC-15802 BLOCK DIAGRAM

TABLE 1. OSC-15802 SPECIFICATIONS		
Specifications apply over temperature range and power supply range.		
PARAMETER	**UNITS**	**VALUE**
FREQUENCY	Hz	Programmable from 400 to 10k
OUTPUTS		
PA OUT		
■ Voltage	V rms	7±1% for 2.5V input
■ Current	mA rms	215 min
REF		
■ Voltage	V rms	2.5 ±10%
■ Current	mA rms	3 min
REF +90°		
■ Voltage	V rms	2.5 ±10%
■ Current	mA rms	3 min
■ Protection		short circuit and transient proof
POWER SUPPLIES		
Voltage	Vdc	±15 ±5%
Current	mA	20 max plus current load
Max Voltage without damage	Vdc	±18
TEMPERATURE RANGE		
Operating		
■ -10X	°C	-55 to +125
■ -30X	°C	0 to +70
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in (mm)	1.0 x 0.8 x 0.2 (25.45 x 20.32 x 4.83) 18 pin DDIP
Weight	oz (gm)	0.4 (1)

OSC-15802 OPERATION

PROGRAMMABLE FREQUENCY OUTPUT

The output frequency of the OSC-15802 is programmable to 10 kHz. The frequency is programmed using two external equal value capacitors (see Figure 2). The value of the capacitors (C_{ext}) is calculated as follows:

$$C_{ext} = \frac{10^7}{f}$$

Where: C is capacitance in picofarads (use NPO ceramic).

f is frequency in Hertz.

To scale down the PA OUT voltage, an external resistor (R_{ext}) is connected between pins 3 and 7. The value of R_{ext} is calculated as follows:

$$R_{ext} = \frac{37.5}{V_{out}} - 5.35$$

Where: R_{ext} is in k Ohms.

V_{out} is the desired voltage in Vrms.

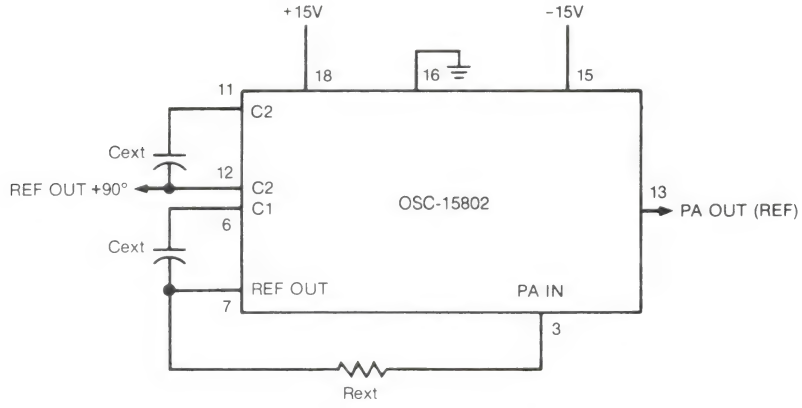

FIGURE 2. PROGRAMMING RESISTOR AND CAPACITOR CONNECTIONS

TABLE 2. OSC-15802 PIN FUNCTIONS		
PIN	NAME	FUNCTION
1	NC	No connection
2	NC	No connection
3	PA IN	Power amplifier input
4	NC	No connection
5	NC	No connection
6	C1	Capaictor connection (pin programmable freq)
7	REF OUT	Reference Output
8	NC	No connection
9	NC	No connection
10	NC	No connection
11	C2	Capaictor connection (pin programmable freq)
12	REF OUT +90°	+90° reference output signal
13	PA OUT	Power amplifier output
14	NC	No connection
15	-15V	-15Vdc power supply voltage
16	GND	Ground
17	NC	No connection
18	+15V	+15Vdc power supply voltage

ORDERING INFORMATION

OSC-15802-3 0 0

Reliability Grade:

0 = Standard DDC processing

1 = Fully compliant with MIL-STD-883B, including full QCI testing.

2 = Screened to MIL-STD-883B, but without QCI Testing.

Temperature:

1 = -55°C to +125°C

3 = 0°C to +70°C

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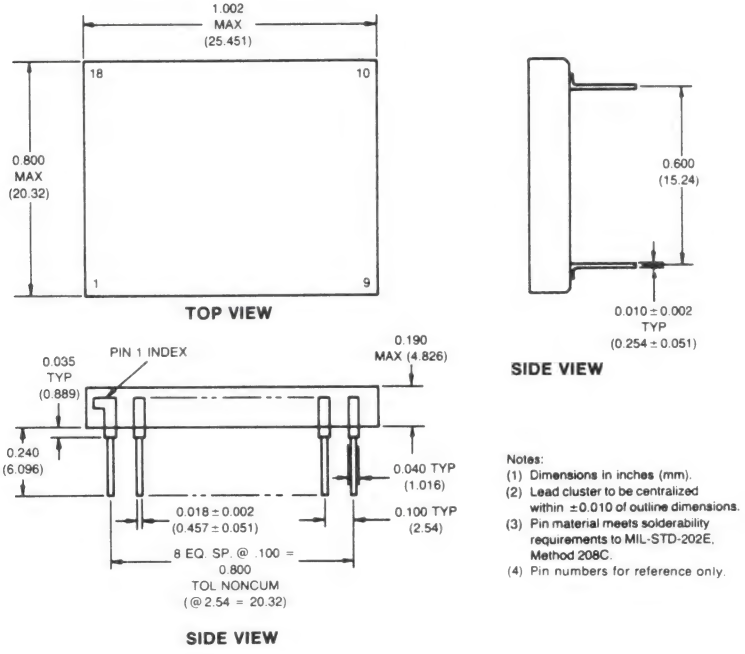

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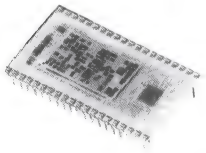
FIGURE 3. OSC-15802 MECHANICAL OUTLINE

DDC
ILC DATA DEVICE CORPORATION

RDC-19200 MONOBRID® SERIES



10, 12, 14, OR 16 BIT INDUSTRIAL RESOLVER TO DIGITAL CONVERTERS

DESCRIPTION

The RDC-19200 Monobrid Series are versatile state-of-the-art resolver to digital converters featuring programmable resolution and bandwidth and a velocity output voltage.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with commensurate accuracies up to 2 minutes +1 LSB. Resolution programming combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in one package.

The velocity output (VEL) from the RDC-19200 is a ground based voltage of 0 to ±10VDC with a linearity of 2.0% or 0.7%. VEL may be scaled up by a single external resistor to provide up to ±10VDC for the required maximum tracking rate.

APPLICATIONS

The RDC-19200 Series converters are designed for use in modern high performance commercial and industrial control systems. Applications include motor control, theodolite, radar antenna position information, CNC machine tooling, robot axis control, and process control. With their low cost and superior performance, the RDC-19200 Series converters are ideal for motion control and position monitoring applications.

FEATURES

- *LOW COST*
- *IDEAL FOR MOTOR CONTROL*
- *BUILT-IN-TEST (BIT) AND LOSS-OF-SIGNAL (LOS) OUTPUTS*
- *VELOCITY OUTPUT ELIMINATES TACHOMETER*
- *PROGRAMMABLE RESOLUTION*
- *PROGRAMMABLE BANDWIDTH*
- *ACCURACY TO ±2.3 ARC MIN.*

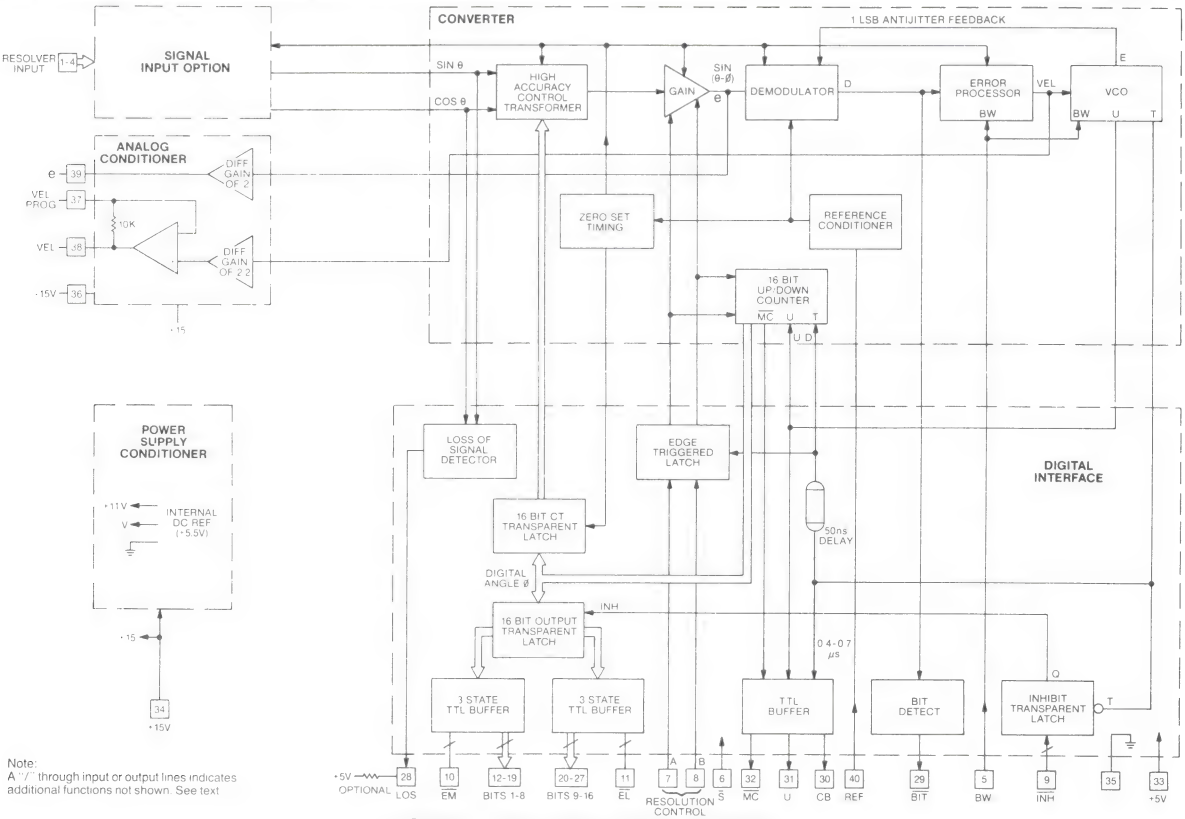


FIGURE 1. RDC-19200 BLOCK DIAGRAM

® Monobrid is a registered trademark of ILC Data Device Corporation.

TABLE 1. RDC-19200 SPECIFICATIONS

These specifications apply over temperature range, power supply range, reference frequency and amplitude range; ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	DESCRIPTION
RESOLUTION	10, 12, 14, or 16 bits	Programmable
ACCURACY GRADES	10, 8, 4, 3, 2 minutes	Max +1 LSB of selected resolution, see Ordering Information
DIFFERENTIAL LINEARITY	16, 12, 8, or 4	LSBs in the 16th bit, see Ordering Information
REPEATABILITY	1 LSB max	
REF INPUT CHARACTERISTICS		
Voltage Range	4-50Vrms	
Single Ended Input Impedance	100K Ohm min, 110K Ohm nom	
Frequency Range	360Hz to 6KHz	See Table 4, Dynamic Characteristics
SIGNAL INPUT CHARACTERISTICS		Voltage options and minimum input impedance, balanced.
Resolver	11.8V L-L	
Z_{in} Single Ended	70K Ohm	
Z_{in} Differential	140K Ohm	
Z_{in} Each line-ground	80K Ohm	
Common Mode Range	26V peak	
Max Voltage w/o damage	100V transient	
Direct	2.0V L-L	
Input Signal Type		Sin and Cos resolver signal referenced to converter's internal DC ref voltage of +5.5V.
Sin/Cos Voltage Range	2V nom, 2.3V max	
Max Voltage w/o Damage	15V continuous, 110V peak transient	
Z_{in}	>20M ohm//10pf voltage follower	
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Max Voltage w/o Damage	−0.3 to 11V	
Loading	−10 μA max	Pull-up current source to +5V//5pf max CMOS transient protected.
$\overline{INH}$ (Inhibit)		Logic 0 inhibits, Logic 1 enables, Data stable within 0.3μs
$\overline{EM}$ (Enable bits 1-8) $\overline{EL}$ (Enable bits 9-16)		Logic 0 enables, data valid within 150 ns. Logic 1 high Z within 100 ns.
$\overline{S}$ (Control Transformer)		Logic 0 for Control Transformer, Logic 1 for normal tracking.
BW (Bandwidth)		Logic 1 = High BW (530 Hz); Logic 0 = Low BW (130 Hz)
Resolution Control 10 Bit 12 Bit 14 Bit 16 Bit		B (pin8) / A (pin 7) 0 / 0 0 / 1 1 / 0 1 / 1 Unused output bits are at logic 0
OUTPUTS		
Parallel Data	10, 12, 14, or 16 bits	Natural binary angle, positive logic
CB (Converter Busy)		0.4 μs to 0.7 μs positive pulse; leading edge initiates counter update.
U (Direction)		Logic 1 counts up, Logic 0 counts down
$\overline{MC}$ (Major Carry)		Logic 0 at $\overline{MC}$
$\overline{BIT}$ (Built in Test)		Logic 0 for $\overline{BIT}$ condition.
LOS (Loss of Signal)		Logic 1 for LOS (1-3μA pull-up to +5V).
Drive Capability	Logic 0: 1 TTL Load Logic 1: 10 TTL Loads High Z: 10μA/5pf max	−1.6mA at 0.4V max 0.4mA at 2.8V min
ANALOG OUTPUTS		
V (Internal DC ref)	+5.5V nom	
VEL (Velocity)		See Table 6, Velocity Characteristics
e (AC error)	50mVrms per LSB of error 25mVrms per LSB of error 12.5mVrms per LSB of error 6.3mVrms per LSB of error	10 bit mode 12 bit mode 14 bit mode 16 bit mode
Dynamic Characteristics		See Table 4, Dynamic Characteristics

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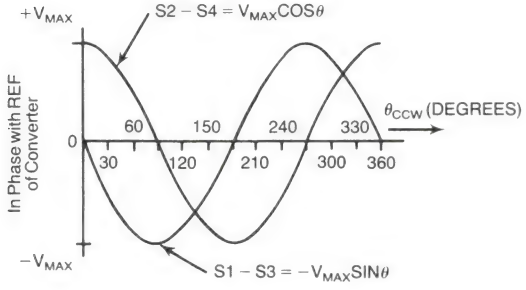
TABLE 1. RDC-19200 SPECIFICATIONS (Continued)

PARAMETER	VALUE			DESCRIPTION
POWER SUPPLY CHARACTERISTICS				
Nominal Voltage and Range	+15VDC ±5%	+5VDC ±10%	−15VDC ±5%	Note: When analog outputs are not required, ground −15V (pin 36).
Max Voltage w/o Damage	+18V	+8V	−18V	
Max Current	25mA	10mA	15mA	
TEMPERATURE RANGES				
Operating	0°C to +70°C			
Storage	−40°C to +120°C			
PHYSICAL CHARACTERISTICS				
Size	1.14 x 2.02 x 0.23 inches (28.96 x 51.3 x 5.84 mm)			40 pin TDIP
Weight	0.46 oz (13 gm)			

TECHNICAL INFORMATION

INTRODUCTION

The RDC-19200 Series are small, 40 pin TDIP resolver to digital hybrid converters. As shown in the block diagram (figure 1), the RDC-19200 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. RESOLVER SIGNALS

SIGNAL INPUT OPTIONS

In a resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The converter internal to the RDC-19200 operates with signals in resolver format, $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Figure 2 shows the resolver signals as a function of the angle θ. The RDC-19200 accepts solid state resolver (11.8Vrms) and direct (2Vrms) inputs. The reference is a single ended input with 100K ohm impedance.

2V DIRECT INPUT OPTION. The direct inputs are transient protected voltage followers which accept 2Vrms resolver inputs, as shown in figure 3. A 2V input from a resolver allows use of a lower reference voltage. This lowers oscillator cost and allows a lower power reference oscillator.

INTERNAL DC REFERENCE VOLTAGE (V). This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference common with the direct input option. It is nominally +5.5V and is proportional to the +15VDC supply.

11.8V RESOLVER INPUT OPTION. The 11.8V resolver inputs are true differential inputs with high AC and DC common mode rejection (see figure 4). Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed 26V peak; maximum transient peak voltage should not exceed 100V.

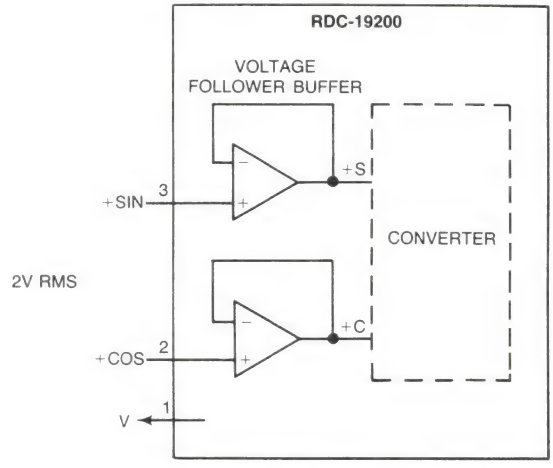


FIGURE 3. DIRECT INPUT OPTION – 2V

RESISTOR PROGRAMMING FOR NON-STANDARD INPUT VOLTAGES. When applying voltages greater than 2Vrms, a simple voltage divider can be used to attenuate both the sin and cos inputs. Since the converter inputs are voltage followers, there will be no loading on the resistor dividers (see figure 5).

The 11.8V resolver input conditioner consists of two differential amplifiers. The 11.8V input is scaled down to 2V. When applying resolver inputs greater than 11.8V, four resistors, one in series with each input line, can be used to scale down the voltage (see figure 6).

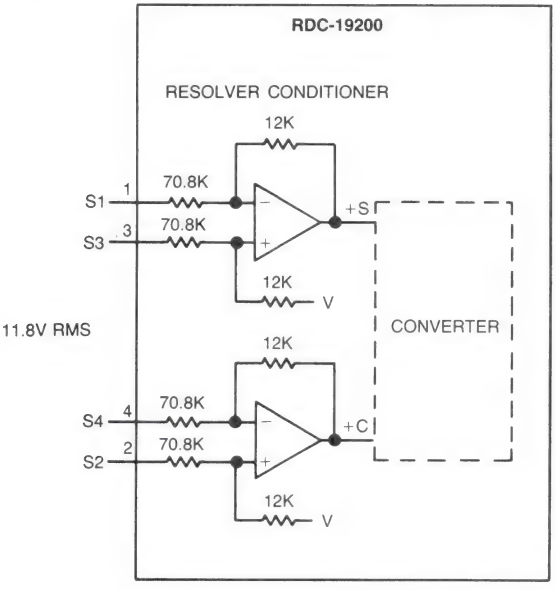
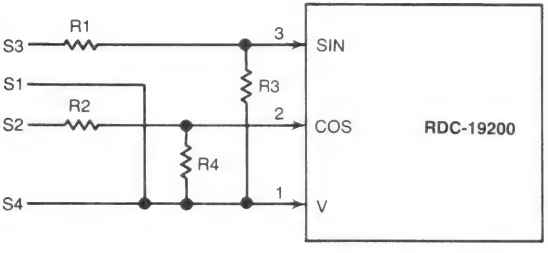


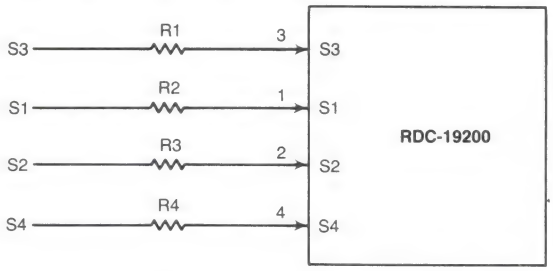
FIGURE 4. RESOLVER INPUT OPTION – 11.8V



$$\frac{\text{Input Voltage L-L}}{2V} = \frac{R1 + R3}{R3}$$

Notes:
(1) R1 = R2; R3 = R4 to 0.1% match.
(2) R1 + R3 and R2 + R4 should be as high as possible to minimize resolver loading.

FIGURE 5. INPUT RESISTOR SCALING – 2V



$$\frac{R + 70.8K}{70.8K} = \frac{\text{Input Voltage L-L}}{11.8V}$$

Notes:
(1) Input Voltage L-L is greater than 11.8V.
(2) R = R1 = R2 = R3 = R4 to 0.1% match.

FIGURE 6. INPUT RESISTOR SCALING – 11.8V

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CONVERTER OPERATION

As shown in figure 1, the converter section of the RDC-19200 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, zero-set timing, and reference conditioner. The converter produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter.

The **control transformer** performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta, representing the resolver shaft position.
ϕ is digital angle phi, contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \blacktriangleright 0$, so that ϕ will repeat the shaft position θ.

The output of the **demodulator** is an analog DC level proportional to $\sin(\theta - \phi)$. The **error processor** receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the **up/down counter**. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

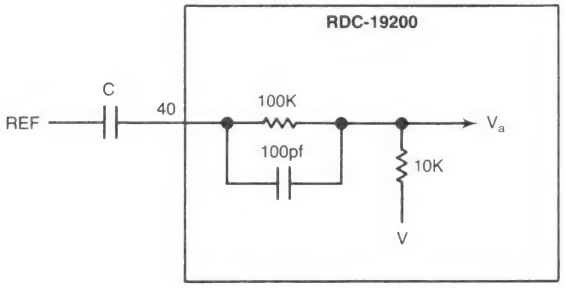
The RDC-19200 has unique **zero-set timing** circuits that cancel out all internal op-amp DC offsets. This zero-setting is done twice a reference input carrier cycle centered around the zero crossings. Each zero-setting cycle lasts for 18μs. During this time, the resolver input is disconnected and a zero input is switched in. The digital input to the control transformer is latched. The resultant DC error at the output of the demodulator is sampled and injected back in during the normal mode of operation.

The result is an effective way of simulating DC offset-free op-amps which ensure a converter whose actual dynamic and large signal performance is the same as its mathematical theoretical

performance. In a somewhat similar manner, the velocity op-amp integrator's DC offset voltage is also cancelled out with this zero-setting scheme.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It is single ended ground based with an input Z of 100K ohms min, 110K ohms nom, resistive.

MINIMIZING ERRORS DUE TO QUADRATURE. In those applications where highest accuracy is needed, the REF input can be phase shifted by adding a capacitor in series with the REF input (pin 40) to add a phase lead equal to the nominal phase lead of the resolver input. To determine the capacitor's value, see figure 7.



Note:
Choose C such that the V_a to REF phase lead is equal to the resolver to REF phase lead plus 9μs.

FIGURE 7. PHASE SHIFTING THE REF INPUT

QUADRATURE VOLTAGES. In a resolver, quadrature voltages are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error = (Quadrature Voltage/F.S. signal) • tan(α)

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift.

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: α = 6°
Then: Magnitude of Error = 0.35 min ≃ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier freq) • F.S. signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the resolver.
Carrier frequency is the REF in Hz.

ANALOG CONDITIONER

The Analog Conditioner section performs three functions. It converts analog ground from 5.5V to 0V, provides a gain of 2 for AC Error (e) and a gain of 2.2 for Velocity (VEL). The velocity scaling sensitivity can be increased with an external resistor. Refer to VEL PROGRAMMING section for more information.

POWER SUPPLY CONDITIONER

The power supply conditioner lowers the internal power supply voltage to the custom CMOS chip to +11V from the +15V supply. The +11V will track the +15V. Internal analog ground is one half of 11V or +5.5V, nom.

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the RDC-19200.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the RDC-19200, applying an Inhibit ($\overline{INH}$) command will lock the data in the **output transparent latch** without interfering with the continuous tracking of the converter's feedback loop. Therefore, the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 9) paragraph.

The **BIT detect** circuitry monitors the error level (D) from the demodulator and the **LOS (loss of signal) detector** detects disconnected resolver inputs.

LOGIC INPUT/OUTPUT

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 10) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 11) to a logic 0. The second byte will contain either bits 9-10 (10 bit resolution), bits 9-12 (12 bit resolution), bits 9-14 (14 bit resolution) or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 2 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EL}$ and $\overline{EM}$ are set to logic 1. Both enables are internally pulled up to +5V by −10μA max current sources.

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1 (MSB ALL MODES)	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.5
8	1.405	84.38
9	0.7031	42.19
10 (LSB 10 BIT MODE)	0.3516	21.09
11	0.1758	10.55
12 (LSB 12 BIT MODE)	0.879	5.27
13	0.439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE)	0.0055	0.33

Note: $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs.

DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 10, 12, 14, or 16 parallel data bits. All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive, 0.4 to 0.7 μs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay (shown in figure 1). Data is valid 0.2 μs after the leading edge of CB (see figure 8). The angle is determined by the sum of the bits at logic 1.

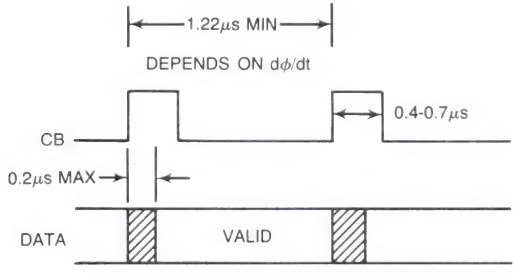


FIGURE 8. CB TIMING

INHIBIT ($\overline{INH}$, PIN 9)

When an Inhibit ($\overline{INH}$) input is applied to the RDC-19200, the Output Transparent Latch is locked, causing the output data bits to remain stable while data is being transferred (see figure 9). The output data bits are stable 0.3 μs after INH is driven to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and INH. While the counter is not being updated, CB is at logic 0 and the INH latch is transparent; when CB goes to logic 1, the INH latch is locked. If CB occurs after INH has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if INH is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and INH where the up-down counter begins to change as an INH is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{INH}$.
(2) Wait 0.3 μs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 10 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

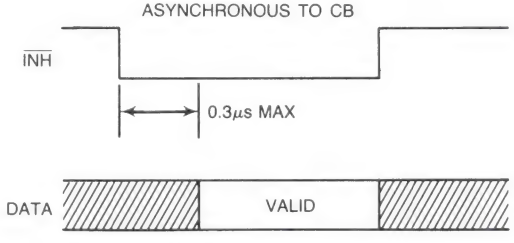


FIGURE 9. INHIBIT TIMING

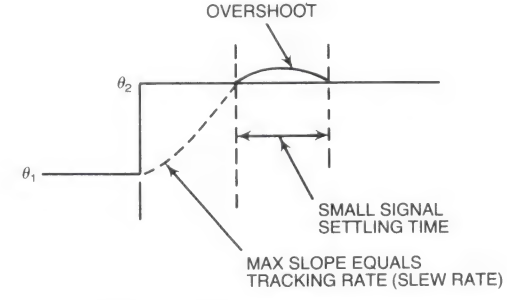


FIGURE 10. RESPONSE TO A STEP INPUT

DATA TRANSFERS

Digital output data from the RDC-19200 can be transferred to 8 bit and 16 bit bus systems. For 8 bit systems, the MSB and LSB bytes are transferred sequentially (see figures 11 and 12). For 16 bit systems, all bits are transferred at the same time (see figures 13 and 14).

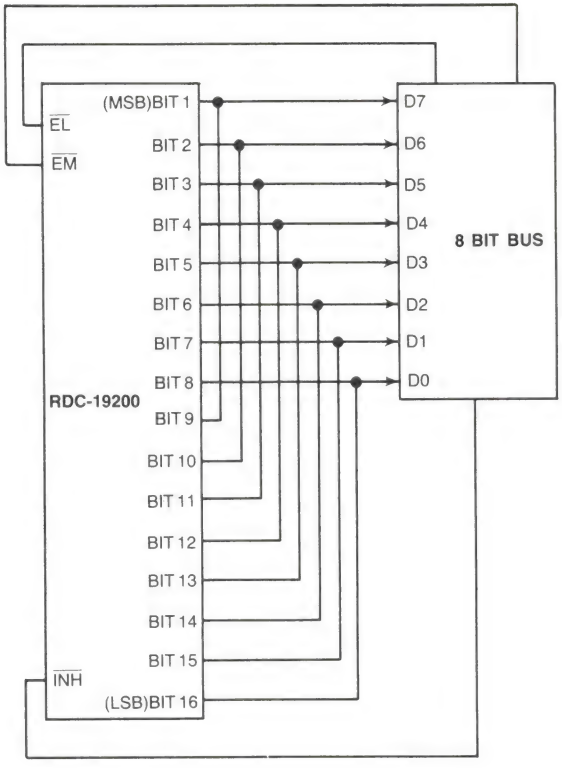


FIGURE 11. DATA TRANSFER TO 8 BIT BUS

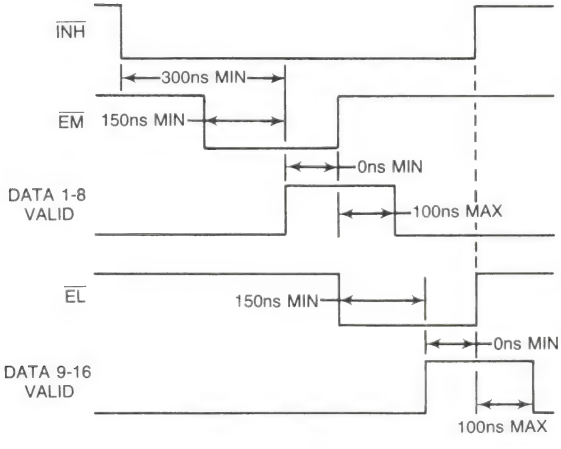


FIGURE 12. DATA TRANSFER TO 8 BIT BUS TIMING

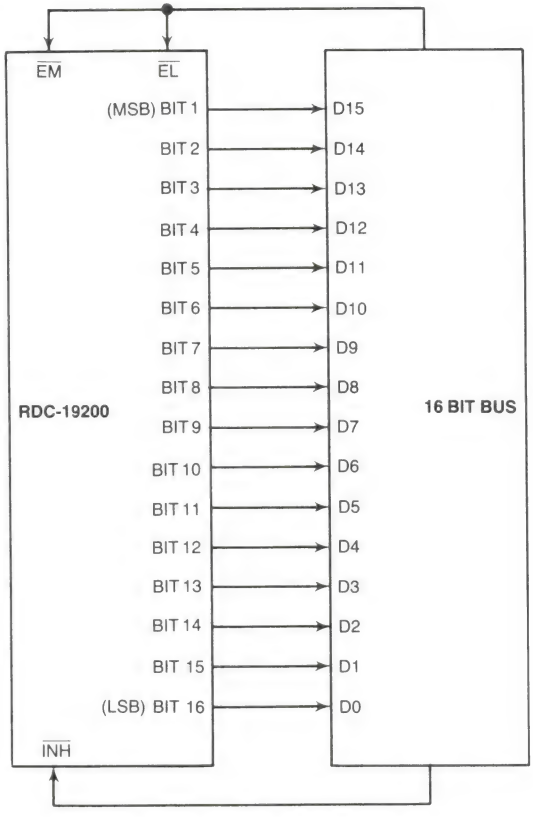


FIGURE 13. 16 BIT DATA TRANSFER

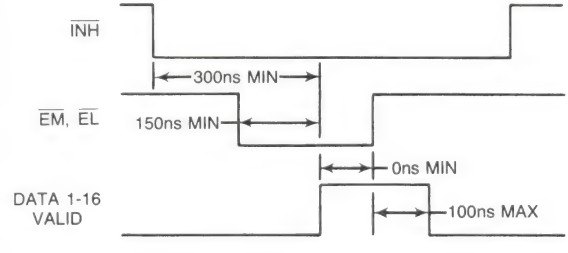


FIGURE 14. 16 BIT DATA TRANSFER TIMING

PROGRAMMABLE RESOLUTION

Resolution is controlled by two logic inputs, A and B (see table 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are transferred through the latch internally on the trailing edge of CB (see figure 15).

TABLE 3. RESOLUTION CONTROL

B (pin 8)	A (pin 7)	RESOLUTION
0	0	10 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Note: All unused digital output data bits are at logic 0.

FASTER SETTLING TIME USING BIT TO REDUCE RESOLUTION

Since the RDC-19200 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the RDC-19200 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth (see figure 22).

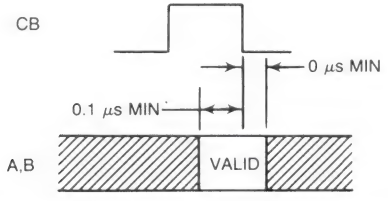


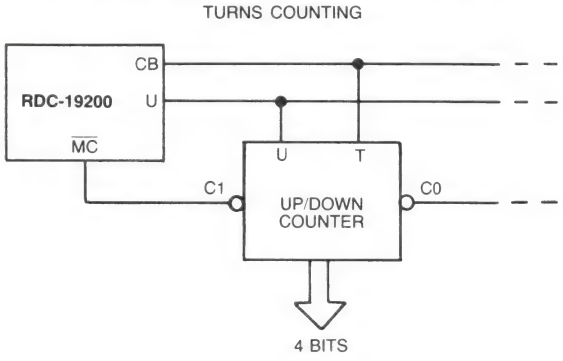
FIGURE 15. RESOLUTION CONTROL TIMING

MAJOR CARRY ($\overline{MC}$, PIN 32)

Major Carry is used with Direction Output (U) for multi-turn applications. This signal is similar to the popular MSI four bit up-down counter CO (Carry Out), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. See figure 16 for a typical interconnection.

DIRECTION OUTPUT (U, PIN 31)

Direction Output (U) is shown in figure 17. It is at logic 1 to count up and logic 0 for down. The logic level at (U) is valid at least 0.5μs before and at least 20ns after the leading edge of CB.



Notes:
(1) For the 4 bit up/down counter, use 74LS169B(TTL) or 4516 (CMOS).
(2) U = up/down line, logic 1 counts up.
(3) T = toggle line, counts on positive edge.

FIGURE 16. TURNS COUNTING CONNECTION DIAGRAM

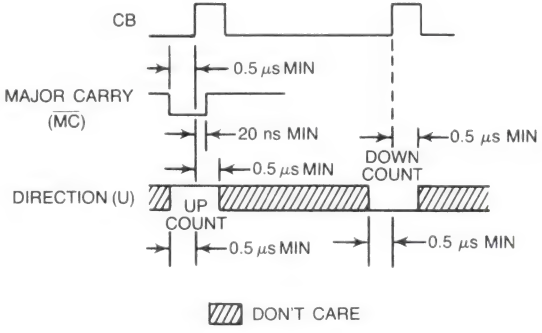


FIGURE 17. DIRECTION OUTPUT (U) TIMING

SYSTEM SELF-TEST

The RDC-19200 provides two useful logic outputs for systems self test, $\overline{BIT}$ and LOS.

BUILT-IN-TEST ($\overline{BIT}$, PIN 29)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition because the converter loop cannot maintain input-output sync or if the converter malfunctions where it cannot maintain the loop at a null. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

LOSS OF SIGNAL (LOS, PIN 28)

The Loss of Signal (LOS) output is used for system safety. The LOS output changes from logic 0 to 1 if both resolver inputs are disconnected. With disconnected resolver inputs, unpredictable converter performance occurs.

If the LOS signal is used with the 2V Direct Input option, connect a 10M ohm resistor from +S to V and from +C to V. This will insure that if the input resolver signal opens, the input pin will go to V volts.

PROGRAMMABLE BANDWIDTH (BW, PIN 5)

Either low or high bandwidth can be selected by using the BW logic input. A logic 0 applied to BW selects low bandwidth (130 Hz nom), while a logic 1 selects high bandwidth (530 Hz nom). Bandwidth can be changed during converter operation.

Bandwidth and the acceleration constant (K_a) can be determined from the following formulas:

$$\text{Closed Loop Bandwidth (Hz)} = \sqrt{2}\, A/\pi$$

$$K_a = A^2$$

See Dynamic Characteristics Table 4 and figures 25 to 27 for values.

TABLE 4. DYNAMIC CHARACTERISTICS

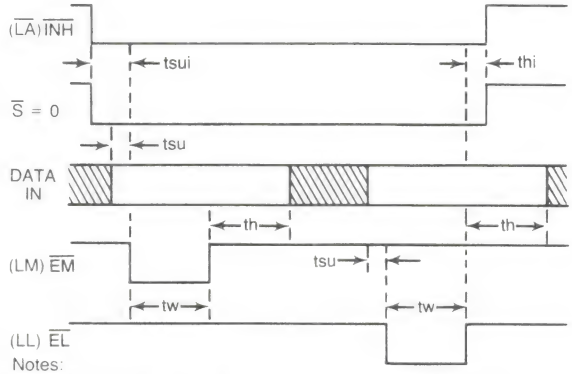
PARAMETER	UNITS	BANDWIDTH							
		HIGH				LOW			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	KHz	1-6	*	2-6	NR	.36-6	*	*	2-6
Tracking Rate	RPS†	800	200	50	12.5	200	50	12.5	3.2
Bandwidth, CL	Hz	530	*	*	*	130	*	*	*
K_a	1/sec^2	1.4M	*	*	*	90K	*	*	*
A_1**	1/sec	8	*	*	*	2	*	*	*
A_2**	1/sec	178	*	*	*	45K	*	*	*
A**	1/sec	1200	*	*	*	300	*	*	*
B**	1/sec	600	*	*	*	150	*	*	*
acc-1 LSB lag	°/sec^2	512K	128K	32K	8K	32K	8K	2K	500
Settling time	msec	10	15	30	75	40	60	120	300

†RPS minimum
*Same as value to left
**See figure 25 for definition of A_1, A_2, A, and B.

CONTROL TRANSFORMER MODE ($\overline{S}$, PIN 6)

The converter will function as a Control Transformer (CT) by placing $\overline{S}$ (pin 6) to logic 0. In the CT mode, the digital inputs are double buffered, $\overline{EM}$ is redefined as LM, $\overline{EL}$ is redefined as LL and $\overline{INH}$ becomes LA (see figures 19 and **28**). Figure 18 shows CT mode timing for a two byte transfer.

The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the resolver input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.



Notes:
(1) tw = 100 ns min (pulse width)
th = 50 ns min (hold time)
thui = 0 ns min (hold time inhibit)
tsu = 0 ns min (setup time)
tsui = 300 ns min (setup inhibit)
(2) When $\overline{S}$ is low:
(LM) $\overline{EM}$ is latch control for MSB byte.
(LL) $\overline{EL}$ is latch control for LSB byte.
1 – data held in latch.
0 – latch is transparent.
(3) (LA) $\overline{INH}$ is latch control for CT latch.
1 – latch is transparent.
0 – data held in latch.

FIGURE 18. CT MODE TIMING – TWO BYTE TRANSFER, DOUBLE BUFFERED

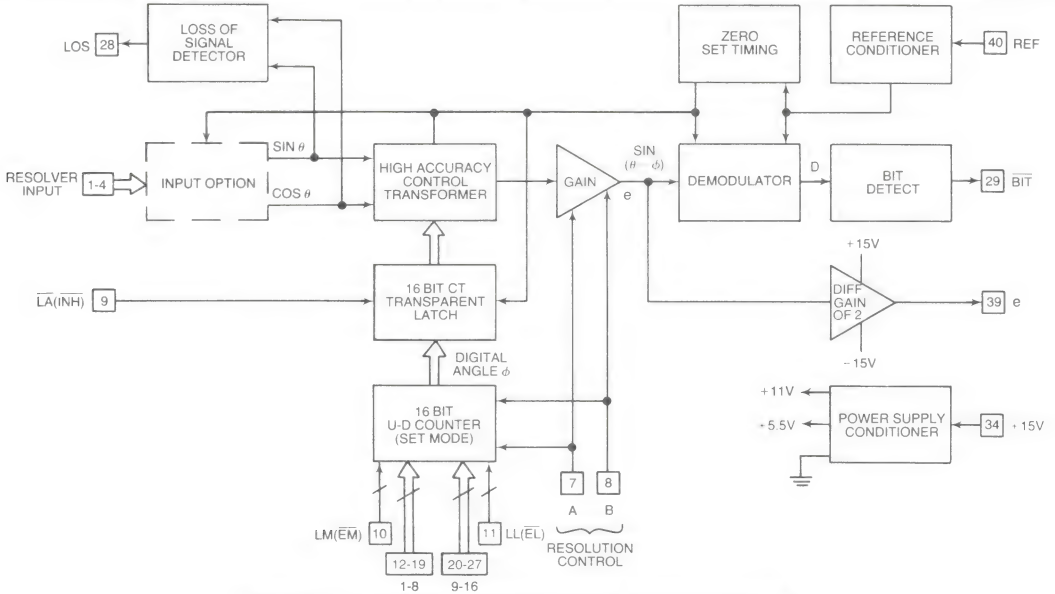


FIGURE 19. CONTROL TRANSFORMER BLOCK DIAGRAM

ANALOG OUTPUTS

The analog outputs are AC error (e) and velocity (VEL). If the analog outputs are not required, ground −15V (pin 36).

AC ERROR (e, PIN 39)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the resolver input angle θ and the digital input angle ϕ, $(\theta - \phi)$, with a scaling of:

50mVrms/LSB (10 bit mode)
25mVrms/LSB (12 bit mode)
12.5mVrms/LSB (14 bit mode)
6.3mVrms/LSB (16 bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10V peak min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level.

VELOCITY (VEL, PIN 38)

The velocity output (VEL, pin 38) is a DC voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The maximum VEL output can swing ±10V min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in table 5.

The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

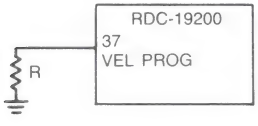
VELOCITY PROGRAMMING (VEL PROG, PIN 37)

The velocity output scale factor can be increased by connecting an external resistor (R) from VEL PROG, pin 37 to ground. By scaling up the output, the noise and offset will increase proportionally. The value of R can be determined by the following formula:

$$R = \frac{10 \times B/A}{1 - B/A}$$

Where:

R = external resistor in K Ohms
A = specified voltage scaling (RPS/VOLT)
B = desired voltage scaling (RPS/VOLT)



To determine A, refer to Table 6, Voltage Scaling.

TABLE 5. VELOCITY OUTPUT CHARACTERISTICS

PARAMETER	UNIT	RDC-19200/19202		RDC-19201/19203	
		TYP	MAX	TYP	MAX
Polarity		(positive for increasing angle)			
Voltage scaling	RPS/V	See Voltage Scaling Table 6			
Scale Factor	%	5	10	5	10
Scale Factor TC	PPM/°C	100	200	100	200
Reversal Error	%	1	2	0.5	0.7 overtemp
Linearity	% output	1	2	0.5	0.7 overtemp
Zero Offset	mV	15	40	15	40
Zero Offset TC	µV/°C	25	50	25	50
Load	KOhms	–	3	–	3
Output Voltage	V	±13	±10 min	±13	±10 min

TABLE 6. VELOCITY OUTPUT VOLTAGE SCALING (RPS/VOLT)

BW	10 BIT	12 BIT	14 BIT	16 BIT
HIGH	80	20	5	1.25
LOW	20	5	1.25	0.32

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the RDC-19200 superior dynamic performance as listed in table 1.

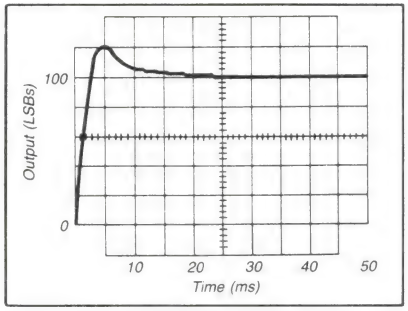
SMALL SIGNAL STEP RESPONSE. Figure 20 illustrates the Small Signal Step Response (100 LSB step) for low and high bandwidth for the four resolutions.

LARGE SIGNAL STEP RESPONSE. Figure 21 illustrates the Large Signal Step Response (179° step) for low and high bandwidth for the four resolutions.

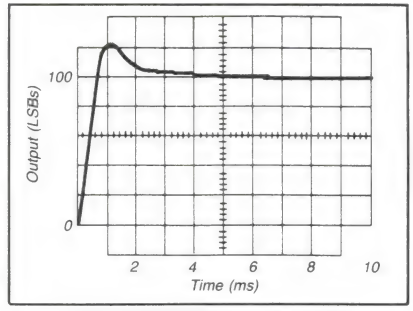
BIT OUTPUT REDUCES SETTLING TIME. By using the $\overline{BIT}$ output together with the A and B inputs, the Large Signal Settling Time may be significantly reduced. Figure 22 shows the connections required for $\overline{BIT}$, A, and B and the resultant settling for the different resolution modes.

VELOCITY RESPONSE

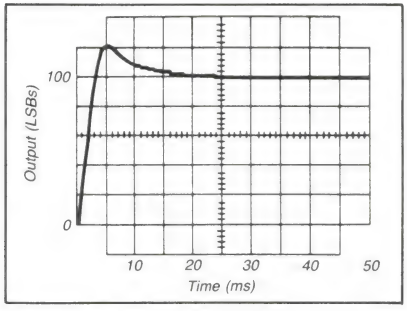
A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. Figure 23 shows the VEL output with and without a filter for low and high bandwidths. The VEL filter is shown in figure 24.



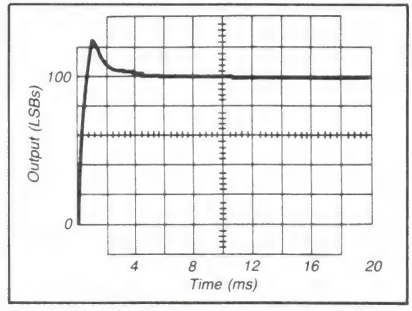
LOW BANDWIDTH – 10 BIT MODE



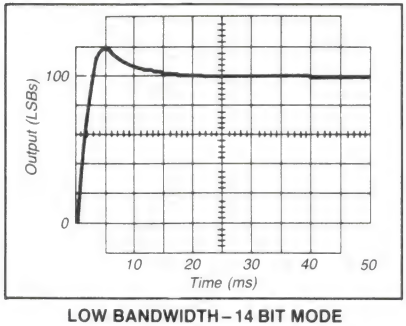
HIGH BANDWIDTH – 10 BIT MODE



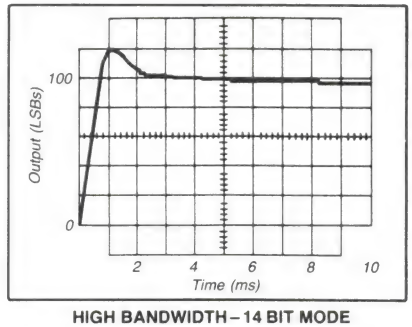
LOW BANDWIDTH – 12 BIT MODE



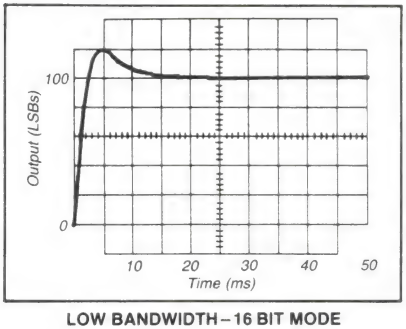
HIGH BANDWIDTH – 12 BIT MODE



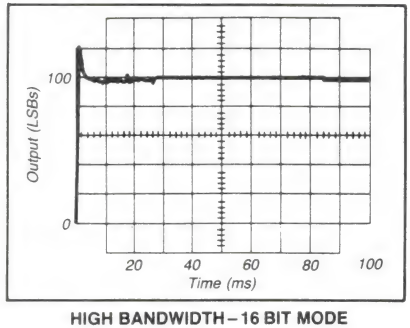
LOW BANDWIDTH – 14 BIT MODE



HIGH BANDWIDTH – 14 BIT MODE

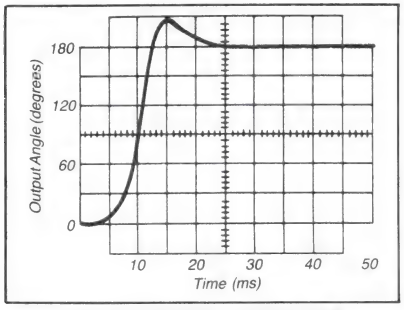


LOW BANDWIDTH – 16 BIT MODE

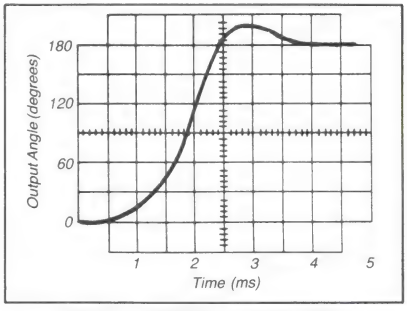


HIGH BANDWIDTH – 16 BIT MODE

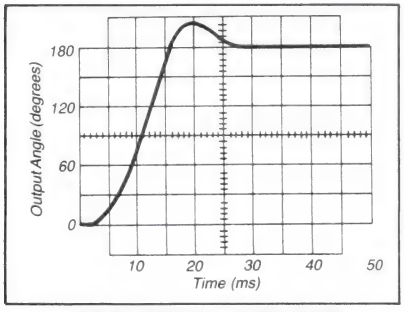
FIGURE 20. SMALL SIGNAL STEP RESPONSE (100 LSB STEP)



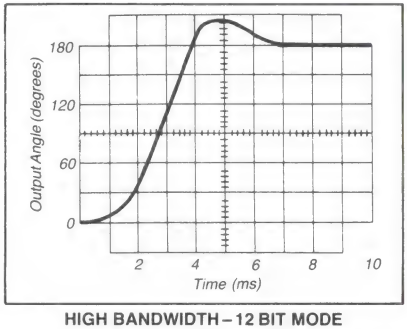
LOW BANDWIDTH – 10 BIT MODE



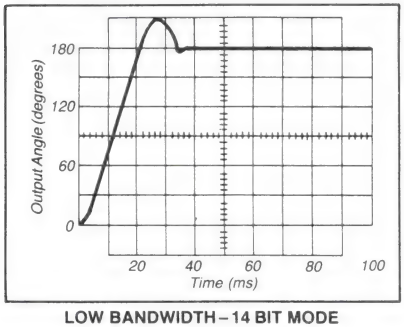
HIGH BANDWIDTH – 10 BIT MODE



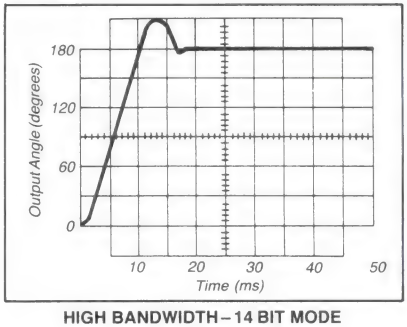
LOW BANDWIDTH – 12 BIT MODE



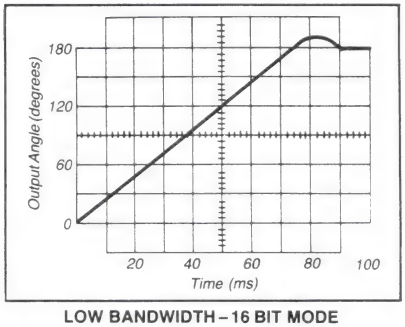
HIGH BANDWIDTH – 12 BIT MODE



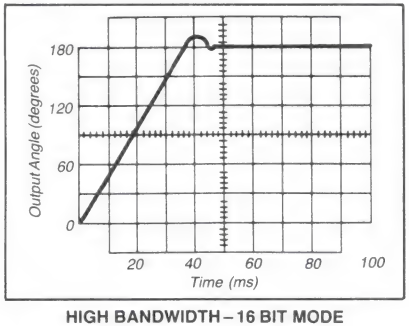
LOW BANDWIDTH – 14 BIT MODE



HIGH BANDWIDTH – 14 BIT MODE

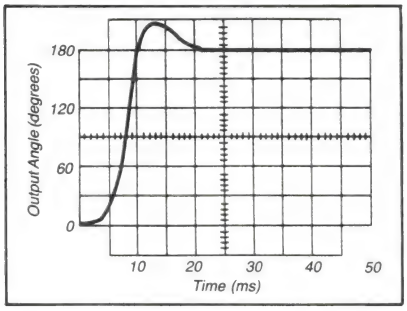


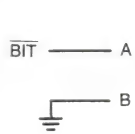
LOW BANDWIDTH – 16 BIT MODE



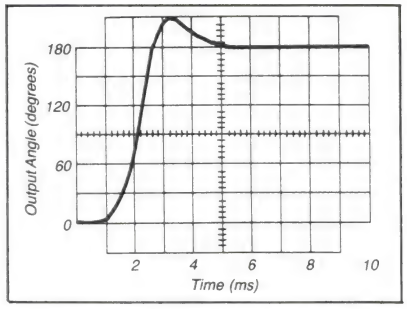
HIGH BANDWIDTH – 16 BIT MODE

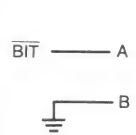
FIGURE 21. LARGE SIGNAL STEP RESPONSE (179° STEP)



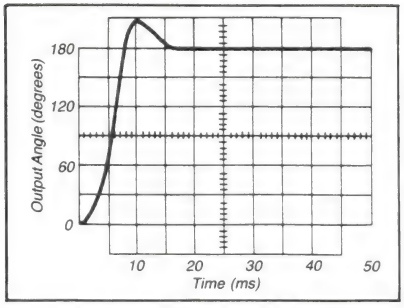


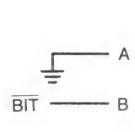
LOW BANDWIDTH 12-10 BIT MODE



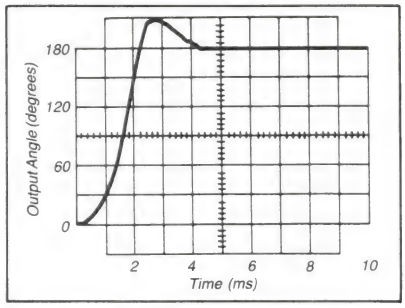


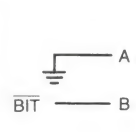
HIGH BANDWIDTH 12-10 BIT MODE



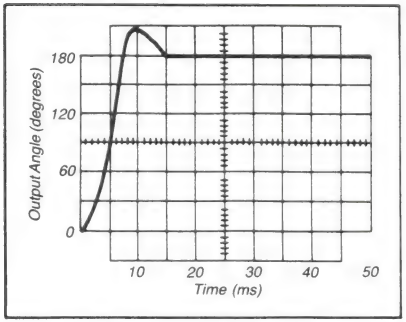


LOW BANDWIDTH 14-10 BIT MODE

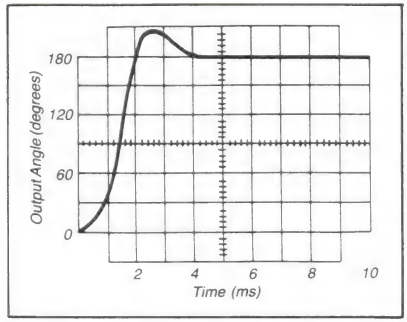




HIGH BANDWIDTH 14-10 BIT MODE

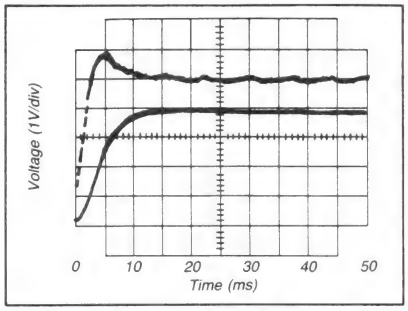


LOW BANDWIDTH 16-10 BIT MODE



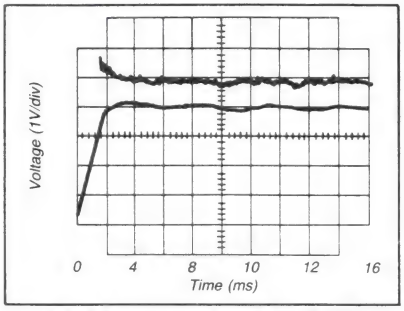
HIGH BANDWIDTH 16-10 BIT MODE

FIGURE 22. USING BIT TO REDUCE SETTLING TIME (179° STEP)



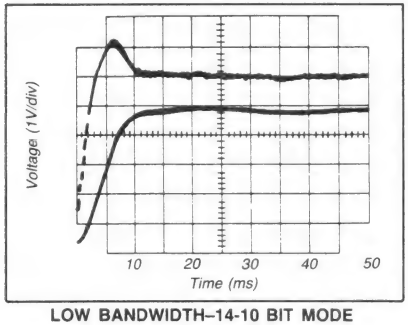
BEFORE FILTER
AFTER FILTER

LOW BANDWIDTH–12-10 BIT MODE



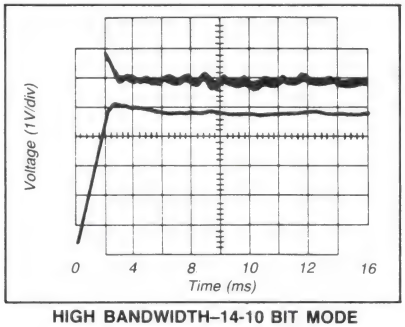
BEFORE FILTER
AFTER FILTER

HIGH BANDWIDTH–12-10 BIT MODE



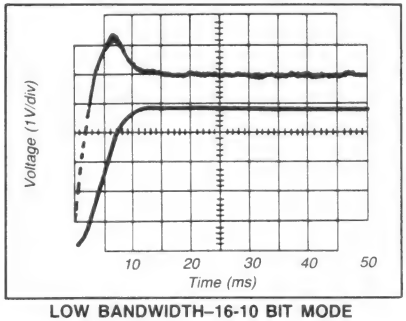
BEFORE FILTER
AFTER FILTER

LOW BANDWIDTH–14-10 BIT MODE



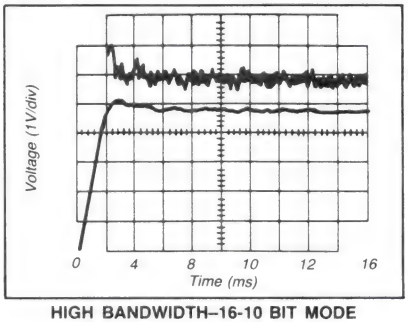
BEFORE FILTER
AFTER FILTER

HIGH BANDWIDTH–14-10 BIT MODE



BEFORE FILTER
AFTER FILTER

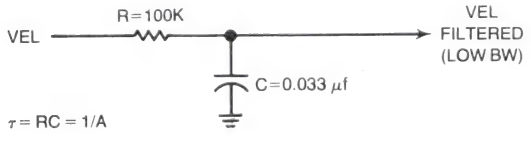
LOW BANDWIDTH–16-10 BIT MODE



BEFORE FILTER
AFTER FILTER

HIGH BANDWIDTH–16-10 BIT MODE

FIGURE 23. VEL OUTPUT WITH AND WITHOUT FILTER



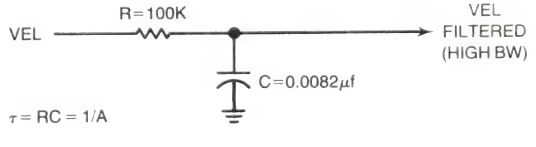
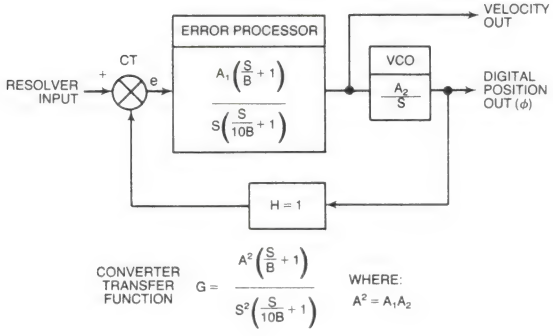


FIGURE 24. VEL OUTPUT FILTERS

TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 25) and open and closed loop Bode plots (figures 26 and 27). Table 4 lists the parameters relating to the RDC-19200's dynamic characteristics for different resolution and bandwidth modes.



Note: See table 4 for values of A1, A2, and B.

FIGURE 25. TRANSFER FUNCTION BLOCK DIAGRAM

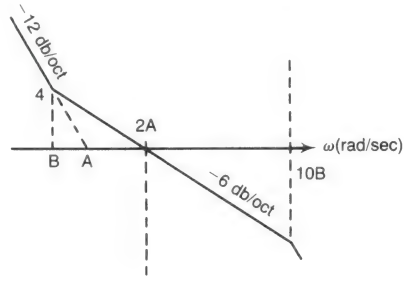


FIGURE 26. OPEN LOOP BODE PLOT

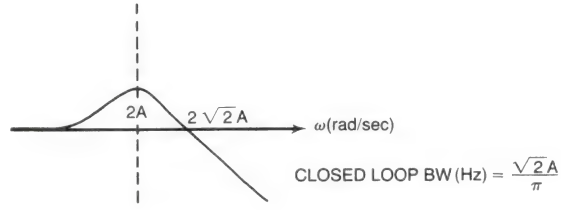


FIGURE 27. CLOSED LOOP BODE PLOT

ACCURACY AND RESOLUTION

Table 7 lists the total accuracy including quantization for the various resolution and accuracy grades.

TABLE 7. ACCURACY/RESOLUTION

RDC-19200 SERIES MODEL NO.	ACCURACY	10 BIT	12 BIT	14 BIT	16 BIT
RDC-1920X-304	2′ + 1 LSB	23.1	7.3	3.3	2.3
RDC-1920X-303	3′ + 1 LSB	24.1	8.3	4.3	3.3
RDC-1920X-302	4′ + 1 LSB	25.1	9.3	5.3	4.3
RDC-1920X-301	8′ + 1 LSB	29.1	13.3	9.3	8.3

RDC-19200 APPLICATIONS

USING THE RDC-19200 IN THE CT MODE

The CT mode can be applied in servo systems, as shown in figure 28. In this application, changes in position are commanded by the computer through signals fed to the CT. The CT then drives the motors through DC power amplifiers.

MULTI-TURN APPLICATIONS – USE OF MAJOR CARRY (MC, PIN 32)

Refer to Major Carry paragraph on page 8 for details.

USING THE RDC-19200 AS AN R/D WITH VEL TO STABILIZE POSITION LOOP

Figure 29 illustrates a typical use of a RDC-19200 connected as an R/D using the VEL output to stabilize the position loop.

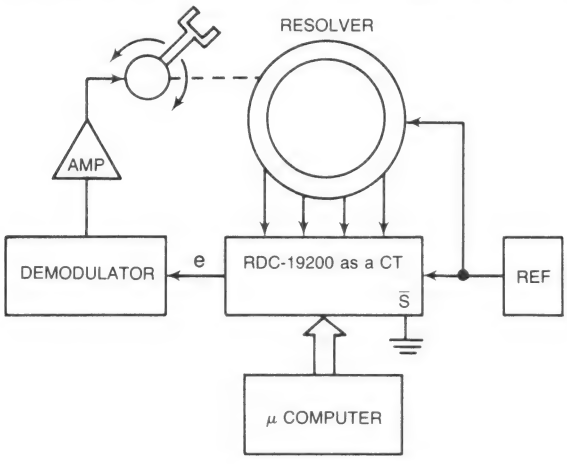


FIGURE 28. CT MODE APPLICATION

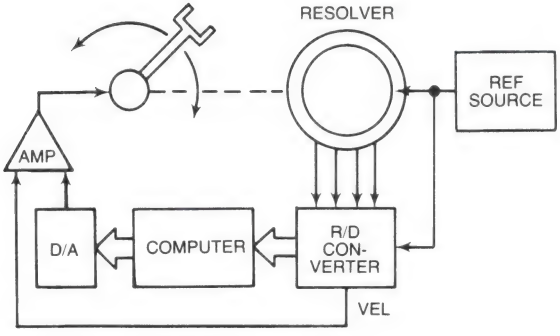


FIGURE 29. R/D WITH VEL TO STABILIZE POSITION

INTERFACING THE RDC-19200 WITH AN IBM PC/XT/AT®

The RDC-19200 can be connected to an IBM PC/XT/AT through the IBM PC Bus located at address HEX 300 through 303. This location is reserved by the PC for prototype cards. Figure 31 illustrates the connection to the IBM PC Bus; figure 30 illustrates the timing considerations for the interface.

RDC-19200 TO IBM PC/XT/AT THEORY OF OPERATION

1. The port address where the RDC-19200 is located is hard wired with jumpers into the 74LS688 address decoder. This address is HEX 300 through 303 and is reserved for prototype cards.

2. Address line A1 selects the upper or lower 8 bits of the RDC-19200 to be placed on the Bus. When A1 is high, bits 1-8 are selected.

3. Address line A0 sets and resets the RDC-19200 INHIBIT line. When A0 is low, the INHIBIT command ($\overline{INH}$) is invoked.

4. To read the output of the RDC-19200, perform the following:

   a. Send address HEX 302 to INHIBIT the RDC-19200 (hold data stable) and place bits 1-8 on the Bus. Read and store data on D0 to D7.

   b. Send address 300 HEX to keep the RDC-19200 in the INHIBIT mode and place bits 9-14 on the Bus. Read and store data on D0 to D7.

   c. Read address 301 HEX or 303 HEX to release the RDC-19200 from the INHIBIT mode and prepare for the next measurement. No valid data will be on the bus during this command.

5. Since the output data is not valid until 0.5μs after the INHIBIT command is invoked, the I/O READY line is held low for this period of time. When I/O READY returns to the high level, the data on the bus reads on the next negative clock edge.

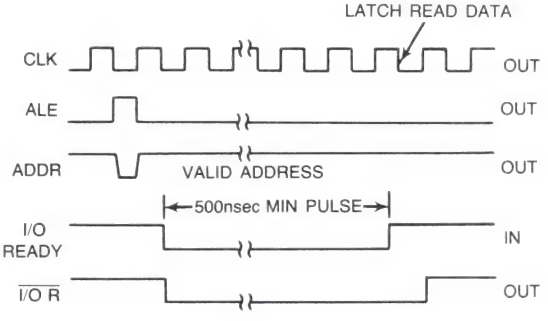


FIGURE 30. PC APPLICATION – I/O READ CYCLE TIMING

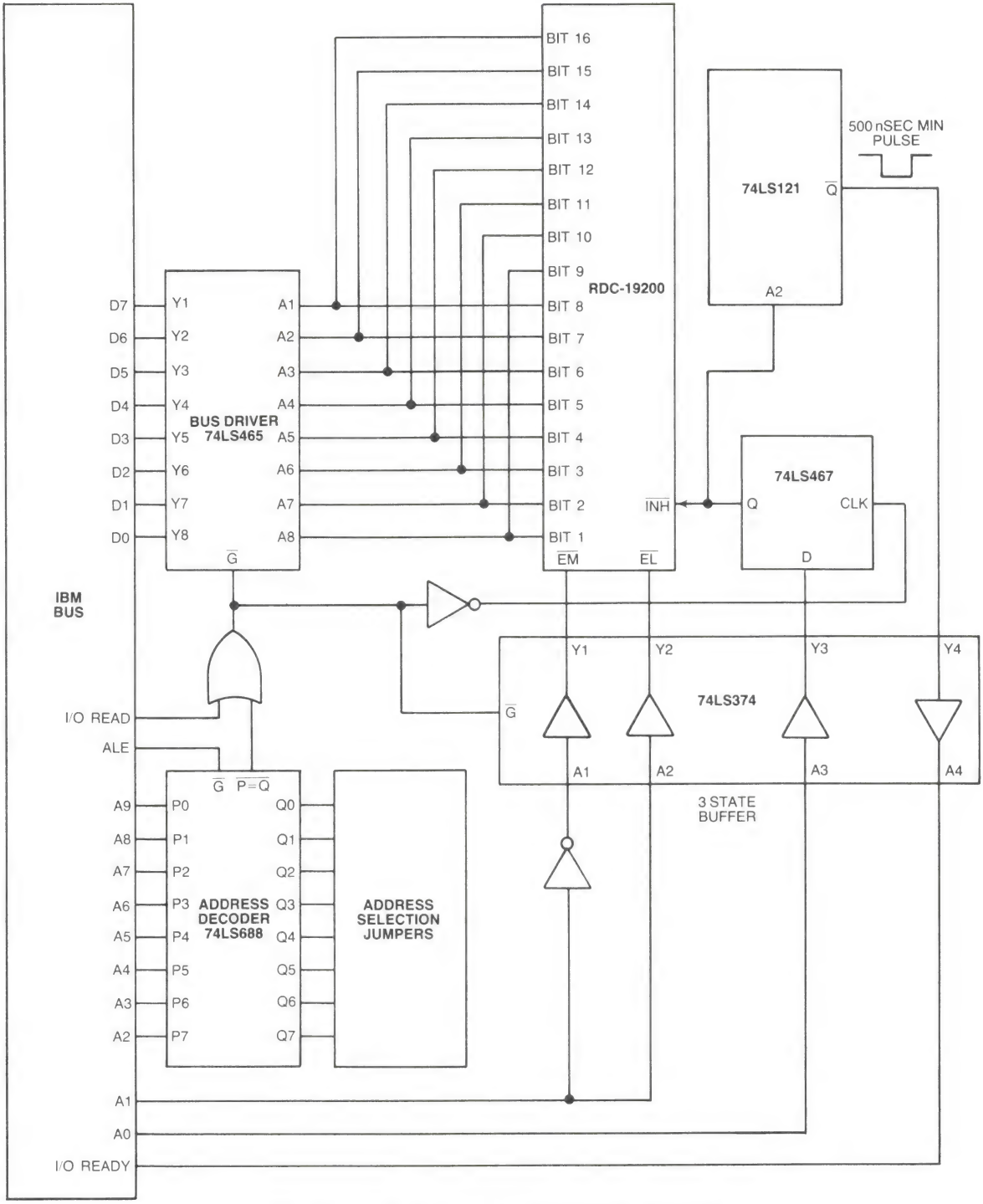


FIGURE 31. RDC-19200 TO PC CONNECTION DIAGRAM

TABLE 8. RDC-19200 PIN FUNCTIONS

PIN NO.	TITLE	I/O	FUNCTION
1	S1(R)V(X)	I	(R) = 11.8V Resolver input; (X) = 2V Direct input.
2	S2(R)+C(X)	I	(R) = 11.8V Resolver input; (X) = 2V Direct input.
3	S3(R)+S(X)	I	(R) = 11.8V Resolver input; (X) = 2V Direct input.
4	S4(R)−	I	(R) = 11.8V Resolver input.
5	BW	I	Bandwidth. Logic 1 for high BW (530 Hz); logic 0 for low BW (130 Hz).
6	$\overline{S}$	I	Control Transformer Set. Logic 1 for normal tracking; logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input, and for presetting the converter to a specific angle to reduce the step response time.
7 8	A B	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bit, depending on logic level. B A Resolution 0 0 10 BIT 0 1 12 BIT 1 0 14 BIT 1 1 16 BIT
9	$\overline{INH}$	I	Inhibit. Logic 0 prevents digital output bits from changing.
10	$\overline{EM}$	I	Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits.
11	$\overline{EL}$	I	Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits.
12	1	O	Digital Output Bit 1 (MSB all modes)
13	2	O	Digital Output Bit 2
14	3	O	Digital Output Bit 3
15	4	O	Digital Output Bit 4
16	5	O	Digital Output Bit 5
17	6	O	Digital Output Bit 6
18	7	O	Digital Output Bit 7
19	8	O	Digital Output Bit 8
20	9	O	Digital Output Bit 9
21	10	O	Digital Output Bit 10 (LSB-10 BIT MODE)
22	11	O	Digital Output Bit 11
23	12	O	Digital Output Bit 12 (LSB-12 BIT MODE)
24	13	O	Digital Output Bit 13
25	14	O	Digital Output Bit 14 (LSB-14 BIT MODE)
26	15	O	Digital Output Bit 15
27	16	O	Digital Output Bit 16 (LSB-16 BIT MODE)
28	LOS	O	Loss of signal. Used for system safety, the LOS output changes from logic 0 to 1 if both resolver inputs are disconnected.
29	$\overline{BIT}$	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65 bits, approx. Also logic 0 for an over-velocity condition.
30	CB	O	Converter Busy. Indicates digital output update.
31	U	O	Direction. Logic 1 to count up; logic 0 to count down.
32	$\overline{MC}$	O	Major Carry. Used for turns counting applications; normally high, goes low for all 1's when counting up or all 0's when counting down.
33	+5V	I	Supply Voltage
34	+15V	I	Supply Voltage
35	GND	−	Ground
36	−15V	I	Supply Voltage.
37	VEL PROG	I	Velocity Programming. Increases output scale factor with external resistor (R) from VEL PROG, pin 37 to ground.
38	VEL	O	Velocity. DC voltage proportional to angular velocity
39	e	O	AC Error. Used in CT mode; e is proportional to the difference between the resolver input angle θ and the digital output angle ϕ ($\theta - \phi$).
40	REF	I	AC Reference Input. Used to drive internal demodulator.

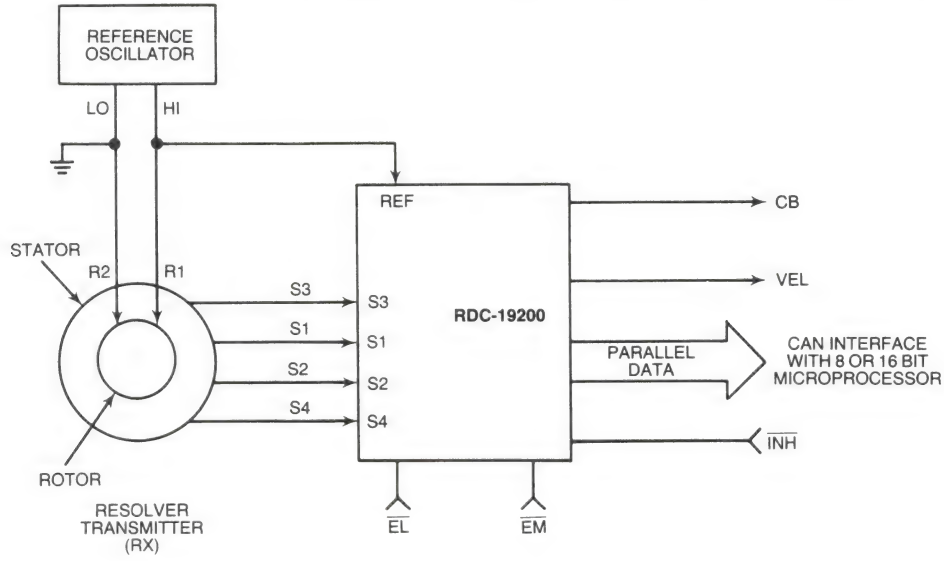


FIGURE 32. RESOLVER CONNECTION – 11.8V

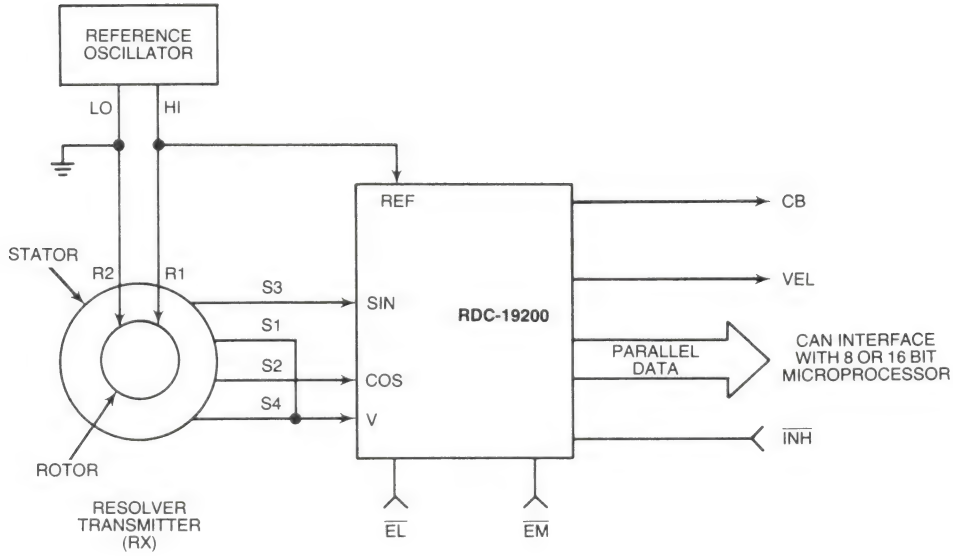


FIGURE 33. RESOLVER CONNECTION – 2V

SOURCES OF SOCKETS FOR THE RDC-19200

The following companies are sources of sockets for use with the RDC-19200 Series. Consult them for more information.

Aries Electronics, Inc.
P.O. Box 130
Frenchtown, NJ 08825
Tel: 1-908-996-6841

Single In-Line Socket
Strip-Line Socket
Part No. 20-05511-11

Circuit Assembly Corp.
18 Thomas Street
Irvine, CA 92718
Tel: 714-855-7887

Part No. CA-20-STL-XX XX-X

ORDERING INFORMATION

RDC-1920X-3 0 X

Accuracy

0 = 10 min +1 LSB (1)
(16 LSBs Differential Linearity, RDC-19200 and RDC-19202 only)

1 = 8 min +1 LSB
(12 LSBs Differential Linearity)

2 = 4 min +1 LSB
(8 LSBs Differential Linearity)

3 = 3 min +1 LSB
(4 LSBs Differential Linearity)

4 = 2 min +1 LSB
(4 LSBs Differential Linearity)

Configuration:

0 = 11.8V, 2% Linearity

1 = 11.8V, 0.7% Linearity

2 = 2V, 2% Linearity

3 = 2V, 0.7% Linearity

Dimensions are inches (mm).

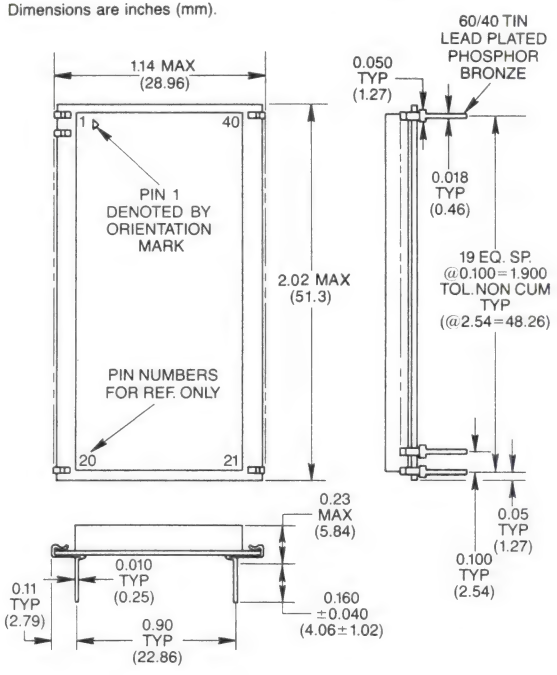


FIGURE 34. RDC-19200 MECHANICAL OUTLINE

CONNECTING THE RDC-19200

The RDC-19200 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

Do not use vapor phase soldering as this product contains SN60 or SN62 solder which melts at 180°C (356°F).

Since the RDC-19200 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

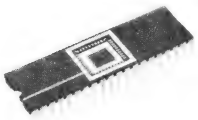
Notes:
(1) Vel and e not characterized on models RDC-19200-300 and RDC-19202-300.
(2) Differential Linearity is x LSB in the 16th bit.

H

DDC
ILC DATA DEVICE CORPORATION

RDC-19220 SERIES

16 BIT MONOLITHIC TRACKING RESOLVER (and LVDT) TO DIGITAL CONVERTERS



DESCRIPTION

The RDC-19220 Series are low cost versatile 16 bit monolithic state-of-the-art Resolver (and LVDT) to Digital Converters. These single chip converters are available in small 40 pin DDIP, 28 pin DDIP, or 44 pin PLCC packages and offer programmable features such as resolution, bandwidth, and velocity output scaling.

Resolution programming allows selection of 10, 12, 14, or 16 bits, with accuracies to 2.3 min. This feature combines the high tracking rate of a 10 bit converter with the precision and low speed velocity resolution of a 16 bit converter in one package.

The velocity output (VEL) from the RDC-19220 Series, which can be used to replace a tachometer, is a 4V signal referenced to ground with a linearity of 0.75% of output voltage. The full scale value of VEL is set by the user with a single resistor.

RDC-19220 Series converters are available with operating temperature ranges of 0° to +70°C, -40° to +85°C, and -55° to +125°C , and military processing is available (consult factory).

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the RDC-19220 Series converters are ideal for use in modern high performance industrial and military control systems. Typical applications include motor control, radar antenna positioning, machine tool control, robotics, and process control.

FEATURES

- *+5V ONLY*
- *ONLY 5 EXTERNAL PASSIVE COMPONENTS*
- *PROGRAMMABLE:*
  - *Resolution 10, 12, 14 , or 16 bits*
  - *Bandwidth to 1060 Hz*
  - *Tracking to 2300 RPS*
- *DIFFERENTIAL RESOLVER AND LVDT INPUT MODES*
- *VELOCITY OUTPUT ELIMINATES TACHOMETER*
- *BUILT-IN-TEST (BIT) OUTPUT*
- *SMALL SIZE: 28 OR 40 PIN DDIP OR 44 PIN PLCC*
- *-55° TO +125°C OPERATING TEMPERATURE*

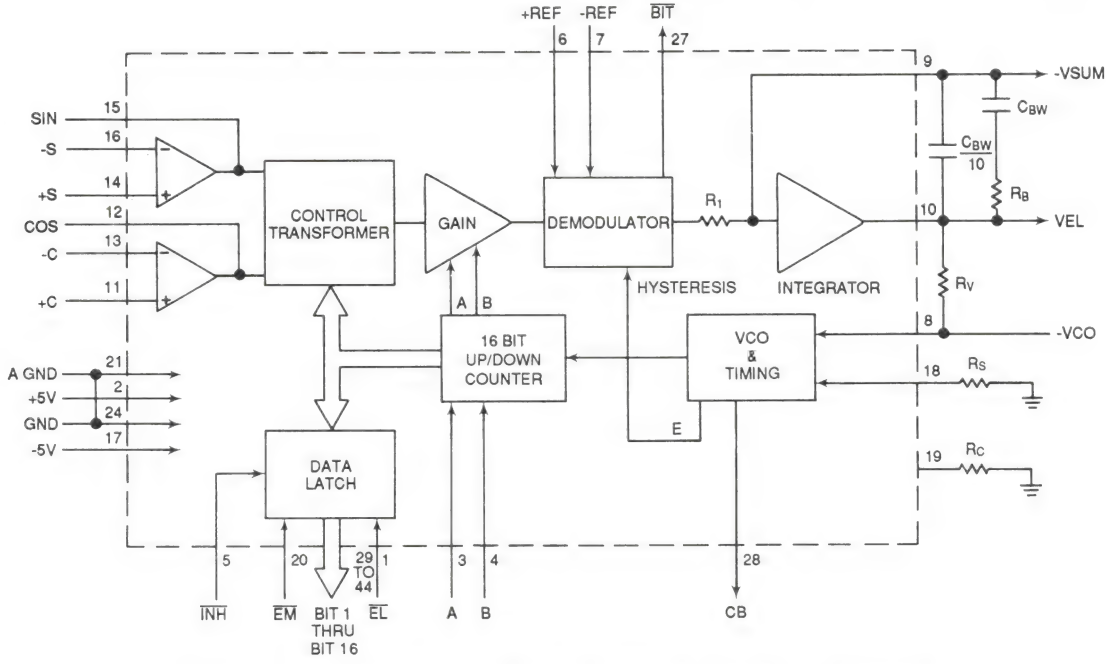


FIGURE 1. RDC-19220 SERIES BLOCK DIAGRAM (44 pin PLCC package)

TABLE 1. RDC-19220 SPECIFICATIONS
These specs apply over the rated power supply, temperature, and reference frequency ranges; and 10% signal amplitude variation & 10% harmonic distortion.

PARAMETER	UNIT	VALUE
RESOLUTION	Bits	10, 12 , 14, or 16
ACCURACY	Min	8, 4, or 2 + 1 LSB (note 3)
REPEATABILITY	LSB	1 max
DIFFERENTIAL LINEARITY	LSB	1 max in the 16th bit
REFERENCE		(+REF, -REF)
Type		Differential
Voltage: differential	V	±10 max
single ended	V	±5 max
overload	V	±25 continuous, 100 transient
Frequency	Hz	DC to 40,000 (note 4)
Input Impedance	Ohm	10M min //20 pf
SIGNAL INPUT		(+S, -S, SIN, +C, -C, COS)
Type		Resolver, differential, groundbased
Voltage: operating	Vrms	2 ±15%
overload	V	±25 continuous
Input impedance	Ohm	10M min //10 pf.
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pf max. CMOS transient protected
Inhibit ($\overline{INH}$)		Logic 0 inhibits; Data stable within 0.3µS
Enable Bits 1 to 8 ($\overline{EM}$) Enable Bits 9 to 16 ($\overline{EL}$)		Logic 0 enables; Data stable within 150 nS Logic 1 = High Impedance Data High Z within 100 nS
Resolution and Mode Control(A & B) (see notes 1 and 2.)		Mode B A Resolution resolver 0 0 10 bits " 0 1 12 bits " 1 0 14 bits " 1 1 16 bits LVDT -5V 0 8 bits " 0 -5V 10 bits " 1 -5V 12 bits " -5V -5V 14 bits
Outputs		
Parallel Data (1-16)		10, 12, 14, or 16 parallel lines; natural binary angle, positive logic (see note 2)
Converter Busy (CB)		0.25 to 0.75 µsec positive pulse leading edge initiates counter update.
Zero Index	(ZI)	Logic 1 at all 0s [$\overline{ENL}$ to -5V]; LSBs are enabled

NOTES: 1. Unused data bits are set to logic "0".
2. In LVDT mode, Bit 16 is LSB for 14 Bit resolution or Bit 12 is LSB for 10 Bit resolution.
3. Accuracy in LVDT mode is 0.15% + 1LSB.
4. See text for higher tracking rates and carrier frequencies, which depend on R_S and R_C selection.

TABLE 1. RDC-19220 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT (continued)		
Outputs (continued)		
Built-in-Test ($\overline{BIT}$)		Logic 0 for BIT condition. ±100 LSBs of error with a filter of 500 µS, Loss-of-Signal (LOS), or Loss-of-Reference (LOR).
Drive Capability		50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, -0.4 mA at 2.8V min Logic 0; 100mV max driving CMOS Logic 1; +5V supply minus 100mV min driving CMOS High Z; 10 uA //5 pF max
DYNAMIC CHARACTERISTICS		(at maximum bandwidth)
Resolution	bits	10 / 12 / 14 / 16
Tracking Rate (min)(note 4)	RPS	1152 / 288 / 72 / 18
Bandwidth(Closed Loop)	Hz	1080 / * / 540 / 270
Ka	$1/sec^2$	5.7M / * / 1.4M / 360k
A_1	1/sec	19.5 / * / 4.9 / 1.2
A_2	1/sec	295k / * / * / *
A	1/sec	2400 / * / 1200 / 600
B	1/sec	1200 / * / 600 / 300
Acceleration (1LSB lag)	deg/s^2	2M / 500k / 30k / 2k
Settling Time(179^o step)	msec	2 / 8 / 20 / 50
VELOCITY CHARACTERISTICS		
Polarity		Positive for increasing angle
Voltage Range(Full Scale)	V	±4
Voltage Scaling (note 4)	RPS/FS	Tracking Rate (min)
Scale Factor	%	10 typ 20max
Scale Factor TC	PPM/C	100 typ 200 max
Reversal Error	%	0.75 typ 1.3 max
Linearity	%	0.25 typ 0.50 max
Zero Offset	mv	5 typ 10max
Zero Offset TC	µV/C	15 typ 30max
Load	kohm	8 max
POWER SUPPLIES		
Nominal Voltage	V	+5 -5
Voltage Range	%	± 5 +5, -20
Max Volt. w/o Damage	V	+7 -7
Current	mA	14 typ,22 max
TEMPERATURE RANGE		
Operating		
-30X	°C	0 to +70
-20X	°C	-40 to +85
-10X	°C	-55 to +125
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size: 40 pin DDIP	in	2.0 x 0.6 x 0.2 (50.8 x 15.24 x 5.08)
28 pin DDIP	(mm)	1.4 x 0.6 x 0.2 (35.56 x 15.24 x 5.08)
44 pin PLCC		0.690 square (17.526)
Weight: 40 pin DDIP	oz	0.94 (26.65)
28 pin DDIP	(g)	0.66 (18.71)
44 pin PLCC		0.5 (14.18)

E

THEORY OF OPERATION

The RDC-19220 series of converters are single CMOS custom monolithic chips. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

Figure 1 is the Functional Block Diagram of RDC-19220 Series. The converter operates with ±5Vdc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of two main sections; a converter and a digital Interface. The converter front-end consists of sine and cosine differential input amplifiers. These inputs are protected to ±25V with 2kohm resistors and diode clamps to the ±5Vdc supplies. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic, and capacitors in precision ratios. **Note:** The transfer function of the CT is normally trigonometric, but in LDVT-mode the transfer function is triangular (linear) and could thereby convert any linear transducer output.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate (67kHz) to eliminate this drifting and at the same time to cancel out the op-amp offsets.
The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and its Bode Plots (open and closed loop). These are shown in figures 2, 3, and 4. The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient and $A^2 = A_1A_2$
and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod with 2Vrms input)

- Integrator gain = $\frac{C_SF_S}{1.1C_{BW}}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25R_VC_{VCO}}$ LSBs per second per volt

where: C_S = 10 pf
F_S = 67 kHz when R_S = 30 kΩ
F_S = 100 kHz when R_S = 20 kΩ
F_S = 134 kHz when R_S = 15 kΩ
C_{VCO} = 50 pf

R_V, R_B, and C_{BW} are selected by the user to set velocity scaling and bandwidth.

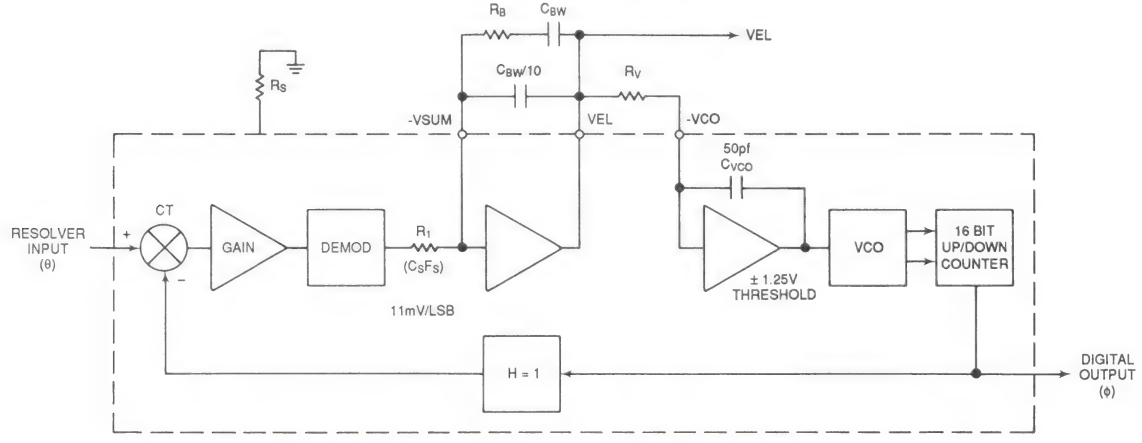


FIGURE 2. TRANSFER FUNCTION BLOCK DIAGRAM #1

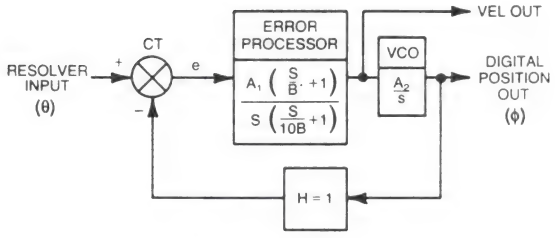


FIGURE 3. TRANSFER FUNCTION BLOCK DIAGRAM #2

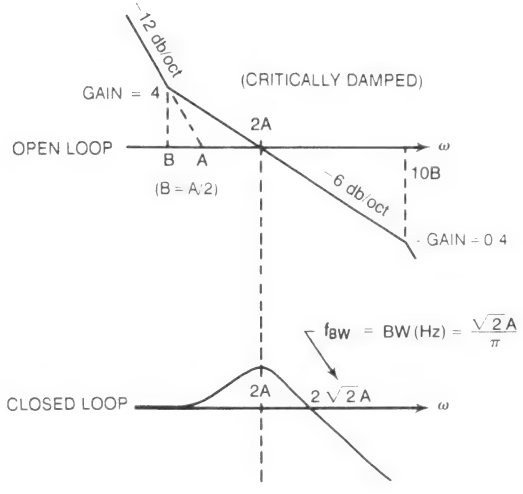


FIGURE 4. BODE PLOTS

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the RDC-19220 Series R/D converters:

1) Power supplies are ±5Vdc. For lowest noise performance it is recommended that a 10 µfd or larger cap be connected from each supply to ground near the converter package.

2) Resolver inputs and velocity output are referenced to A GND. This pin should be connected to GND near the converter package. Digital currents flowing through ground will not disturb the analog signals.

3) The $\overline{BIT}$ output which is active low is activated by an error of about 100 LSBs. During normal operation for step inputs or on power up a large error can exist. Connecting the $\overline{BIT}$ output back to the resolution control lines, A and B which would change the resolution of the converter down would make the converter settle out faster. The converter bandwidth is independent of the resolution.

4) Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

- Select the desired f_{BW}(closed loop)

- Select $f_{carrier} \geq 4\ f_{BW}$

- Compute $R_V = 55k\Omega \times \frac{\{\text{For the converter max tracking rate value, see the row indicated in Table 2.}\}}{\text{Application max rate}}$

- Compute $C_{BW}(pf) = \frac{3.2 \times F_S\,(Hz) \times 10^8}{R_V \times (f_{BW})^2}$

- Compute $R_B = \frac{0.9}{C_{BW} \times f_{BW}}$

- Compute $\frac{C_{BW}}{10}$

5a) **For RDC-19222:**
When using the built-in -5V inverter: connect pin 2 to 26, pin 17 to 22, a 10 µF/10Vdc capacitor from pin 23 (negative terminal) to pin 25 (positive terminal), and a 47µF/10Vdc capacitor from -5V to GND. The current drain from the +5V supply doubles. No external -5V supply is needed.

5b) **For RDC-19223:**
When using the built-in -5V inverter: connect pin 2 to 22, pin 10 to 18, a 10 µF/10Vdc capacitor from pin 19 (negative terminal) to pin 21 (positive terminal), and a 47µF/10Vdc capacitor from -5V to GND. The current drain from the +5V supply doubles. No external -5V supply is needed.

Note: The RDC-19220 Series is completely supply/signal sequence insensitive.

HIGHER TRACKING RATES AND CARRIER FREQUENCIES.

Tracking rate (nominally 4V) is limited by two factors: Velocity voltage saturation and maximum internal clock rate (nominally 1,333,333 Hz). An understanding of their interaction is essential to extending performance.

The General Setup Considerations section makes note of the selection of R_V for the desired velocity scaling. R_V is the input resistor to an inverting integrator with a 50 pF nominal feedback capacitor. When it integrates to -1.25V, the converter counts up 1 LSB and when it integrates to +1.25V, the converter counts down 1 LSB. When a count is taken, a charge is dumped on the capacitor; such that, the voltage on it changes 1.25V in a direction to bring it to 0V. The output counts per second per volt input is therefore:

$$\frac{1}{(R_V \times 50pF \times 1.25)}$$

As an example:

Calculate R_V for the maximum counting rate, at a VEL voltage of 4V.

For a 12 bit converter there are 2^{12} or 4096 counts per rotation. 1,333,333/4096 = 325 rotations per second or 333,333 counts per second per volt.

$$R_V = \frac{1}{(333{,}333 \times 50pF \times 1.25)} = 48k \text{ ohms}$$

The maximum rate capability of the RDC-19220 is set by R_S. When R_S = 30kΩ (or is an open circuit) it is nominally 1,333,333 counts/sec, which equates to 325 RPS (rotations per second). The converter maximum tracking rate can be increased 50% in the 16 and 14 bit modes and 100% in the 12 and 10 bit modes by increasing the supply current from 12 to 15mA (by using an R_C = 23kΩ); and by increasing the sampling rate by changing R_S to 20kΩ for 16 and 14 bit resolution or to 15kΩ for 12 and 10 bit resolution. (See Table 2.)

The maximum carrier frquency can, in the same way, increase from: 5 to 10 kHz in the 16 bit mode, 7 to 14kHz in the 14 bit mode, 11 to 32kHz in the 12 bit mode, and 20 to 40kHz in the 10 bit mode. (See Table 3.)

The maximum tracking rate and carrier frequency for full performance are set by the power supply current control resistor (R_C) per the following tables:

Table 2. Max Tracking Rate (min) in rps

R_C	R_S	resolution			
		10	12	14	16
30k or open	27k	1152	288	72	18
23k	20k	1728	432	108	27
23k	15k	2304	576	*	*

Depending on the resolution, select one of the values from this row, for use in converter max tracking rate formula. (See previous page for formula.)

*Not recommended

Table 3. Carrier Frequency (max) in kHz

R_C	R_S	resolution			
		10	12	14	16
30k or open	27k	20	11	7	5
23k	27k	24	12	11	7
23k	20k	34	30	14	10
23k	15k	40	32	*	*

*Not recommended

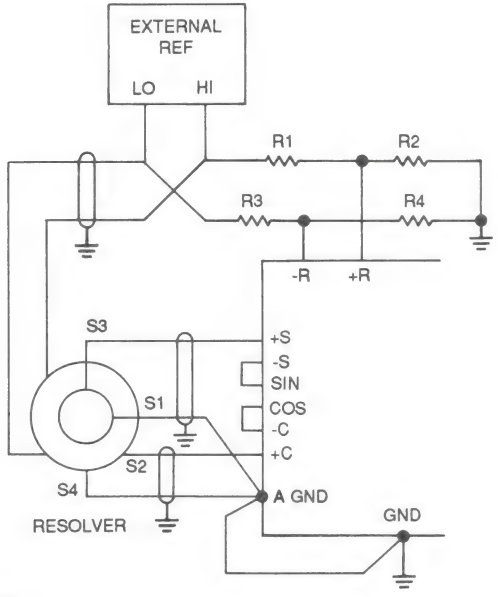
Carrier frequency should be 1/10, or less, of the sampling frquency in order to have many samples per carrier cycle. The converter will work with reduced quadrature rejection at a carrier frequency up to 1/4 the sampling frequency. Carrier frequency should be at least 4 times the BW in order to eliminate the chance of jitter.

REDUCED POWER SUPPLY CURRENTS

When R_S = 30kΩ , and the tracking is not being pushed, power supply current can be cut from 14 to 9mA by setting R_C = 53kΩ.

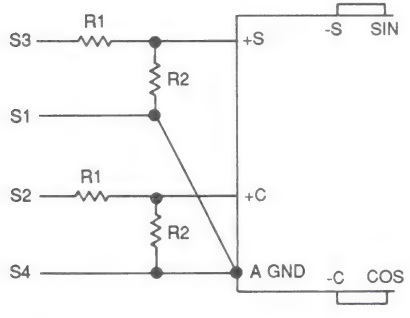
TYPICAL INPUTS

Figures 5 through 8 illustrate typical input configurations.



Notes:
1. Resistors selected to limit V_{ref} peak to between 1V and 4V.
2. If External Reference LO is grounded, then R3 and R4 are not needed, and -R is connected to GND.

FIGURE 5. TYPICAL HOOK-UP, 2V RESOLVER, DIRECT INPUT.



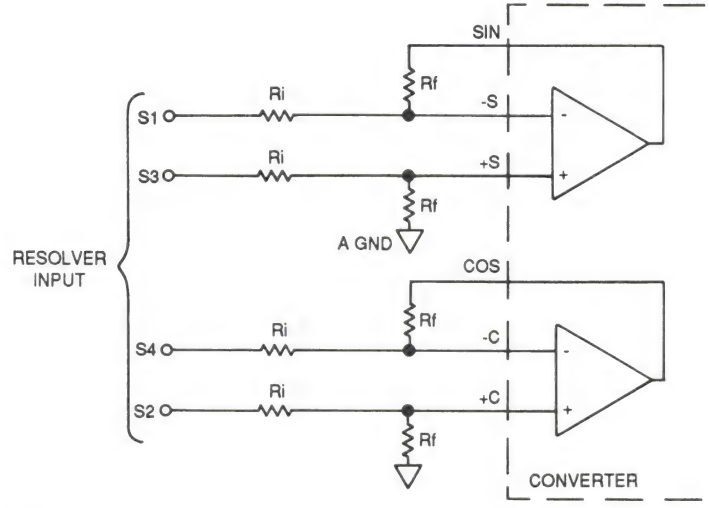
$$\frac{R2}{R1+R2} = \frac{2}{X\ Volt}$$

R1 + R2 should not load the Resolver too much; it is recommended to use a R2 =10k.

R1 + R2 Ratio Errors will result in Angular Errors, 2 cycle, 0.1% Ratio Error = 0.029° Peak Error.

FIGURE 6. TYPICAL HOOK-UP, X- VOLT RESOLVER, DIRECT INPUT.

Consult factory for input thin-film resistor networks.

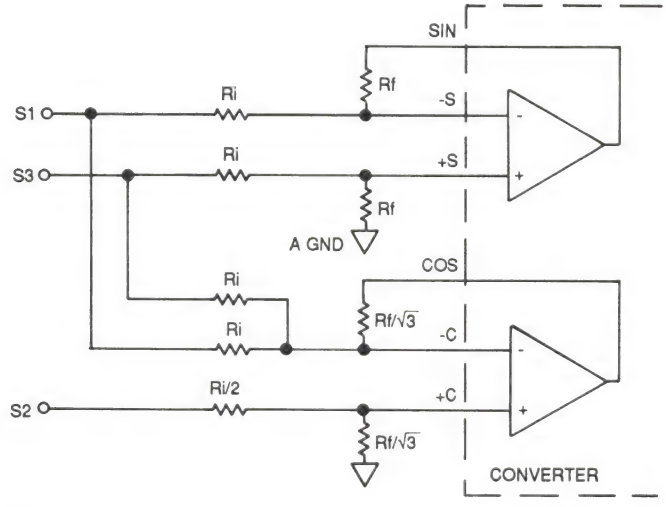


$\frac{Ri}{Rf}$ X 2Vrms = Resolver L-L rms voltage

Rf ≥ 10k ohms.

S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.

FIGURE 7. DIFFERENTIAL RESOLVER INPUT.



Use precision resistors.

$\frac{Ri}{Rf}$ X 2Vrms = Synchro L-L rms voltage

Rf ≥ 10k ohms.

S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded; In both cases the shield should be tied to GND at the converter.

FIGURE 8. SYNCHRO INPUT.

DC INPUTS

As noted in Table 1 the RDC-19220 will accept dc inputs. It is necessary to set the REF input to dc by tying +REF to +5V and -REF to GND or -5V.

VELOCITY TRIMMING

RDC-19220 Series specifications for velocity scaling, reversal error, and offset are contained in Table 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. Figure 9 shows the setup for trimming these parameters with external pots.

It should also be noted that when the resolution is changed, VEL Scaling is also changed. Since the VEL output is from an integrator with capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth. This transient **does not** effect postion data.

LVDT MODE

As shown in Table 1 the RDC-19220 Series units can be made to operate as LVDT-to-digital converters by connecting Resolution Control inputs A and B to "0", "1", or the -5 volt supply. In this mode the RDC-19220 Series functions as a ratiometric tracking linear converter. When linear ac inputs are applied from a LVDT the converter operates over one quadrant of its range. This results in two less bits of resolution for LVDT mode than are provided in resolver mode.

Figure 10a shows a direct LVDT 1Vrms full scale input. Some LDVT output signals will need to be scaled to be compatible with the converter input. Figure 10b is a schematic of an input scaling circuit applicable to 3-wire LVDTs. The value of the scaling constant "a" is selected to provide an input of 2Vrms at full stroke of the LVDT. The value of scaling constant "b" is selected to provide an input of 1Vrms at null of the LVDT. Suggested components for implementing the input scaling circuit are a quad op amp, such as a 4741 type, and precision film resistors of 0.1% tolerance.

Data output of the RDC-19220 Series is Binary Coded in LVDT mode. The most negative stroke of the LVDT is represented by ALL ZEROS and the most positive stroke of the LVDT is represented by ALL ONES. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code "01" and negative overrange is indicated by code "11" (see Table 4).

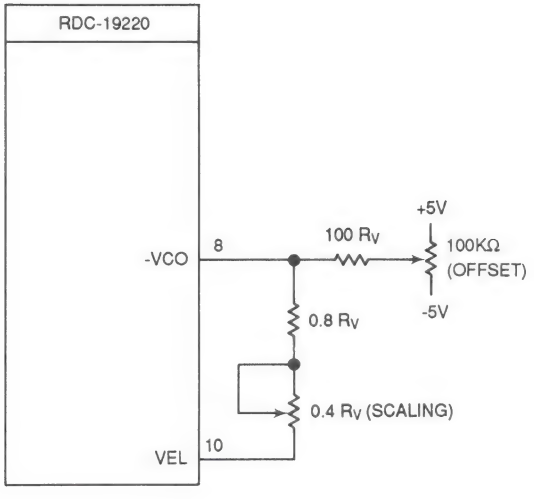


FIGURE 9. VELOCITY TRIMMING

TABLE 4.

LVDT OUTPUT	MSB			LSB
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1LSB	00	1111	1111	1111
+ 0.5 travel	00	1100	0000	0000
+ 1LSB	00	1000	0000	0001
null	00	1000	0000	0000
- 1LSB	00	0111	1111	1111
- 0.5 travel	00	0100	0000	0000
- full travel +1LSB	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx

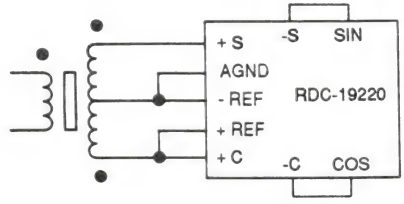
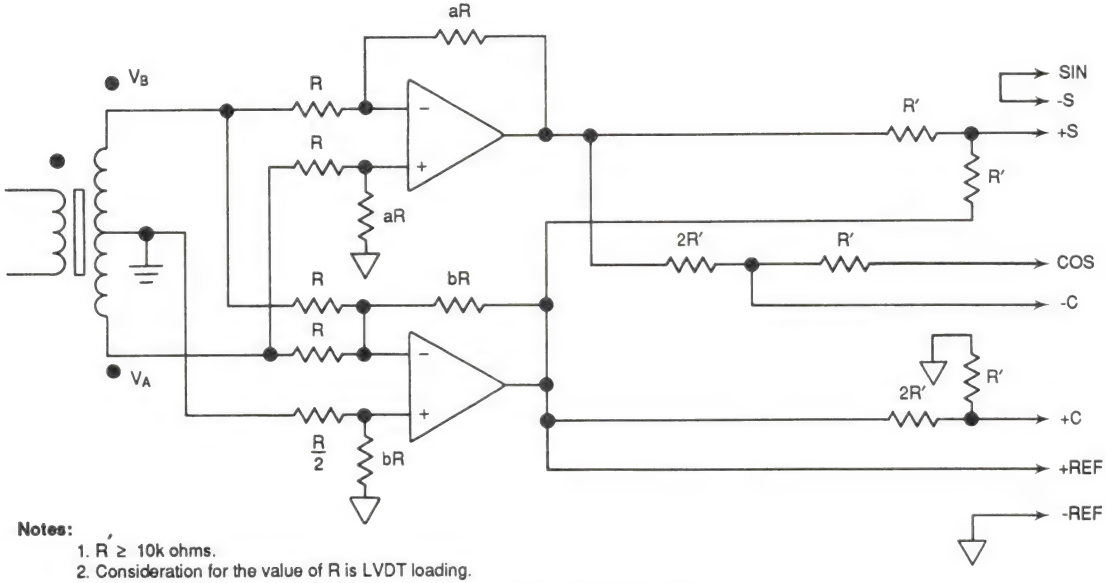
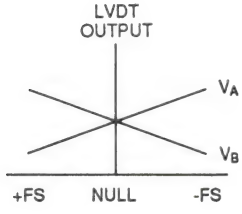


FIGURE 10a. 3-WIRE LVDT DIRECT INPUT



Notes:
1. R′ ≥ 10k ohms.
2. Consideration for the value of R is LVDT loading.



$$b = \frac{1}{V_{A_{null}}} = \frac{1}{V_{B_{null}}}$$

$$a = \frac{2}{(V_A - V_B)_{max}}$$

$$SIN = 1 + \frac{a}{2}(V_A - V_B)$$

$$COS = 1 - \frac{a}{2}(V_A - V_B)$$

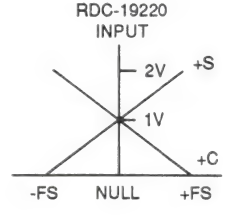


FIGURE 10b. 3-WIRE LVDT SCALING CIRCUIT

INHIBIT, ENABLE, and CB TIMING

The Inhibit (INH) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 11, angular output data is valid 300 nanoseconds maximum after the application of the negative inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{EM}$) is used for the most significant 8 bits and Enable LSBs ($\overline{EL}$) is used for the least significant 8 bits. As shown in figure 12, output data is valid 150 nanoseconds maximum after the application of a negative enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB. As shown in figure 13, output data is valid 150 nanoseconds maximum after the middle of the CB pulse. CB pulse width is 1/40 Fs, which is nominally 375nsec.

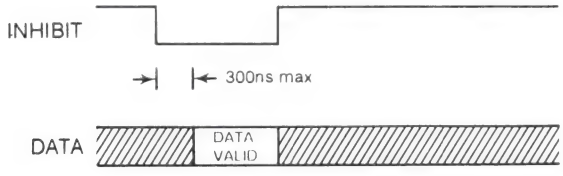


FIGURE 11. INHIBIT TIMING

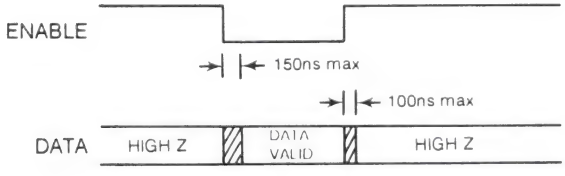


FIGURE 12. ENABLE TIMING

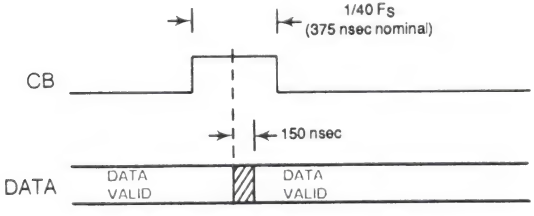


FIGURE 13. CONVERTER BUSY TIMING

ENCODER EMULATION

The RDC-19220 can be made to emulate incremental optical encoder output signals, where such an interface is desired. This is accomplished by tying $\overline{EL}$ to -5V, whereby CB becomes Zero Index (ZI) Logic 1 at all 0s, the LSB becomes A, and the exclusive-or of the LSB and next-to-LSB become B emulating A QUAD B signals as illustrated in figure 14.

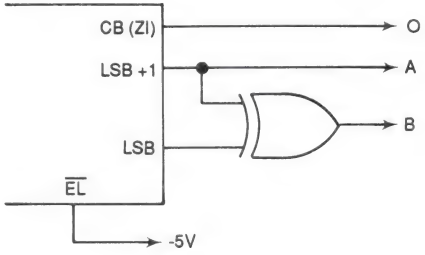


FIGURE 14. INCREMENTAL ENCODER EMULATION

TYPICAL -5V CIRCUITS

Since the 28 and 40 pin DDIP RDC-19220 and RDC-19221 do not have a pinout for the -5V inverter, it may be necessary to create a -5V from other supplies on the board. Figure 15 illustrates several possibilities.

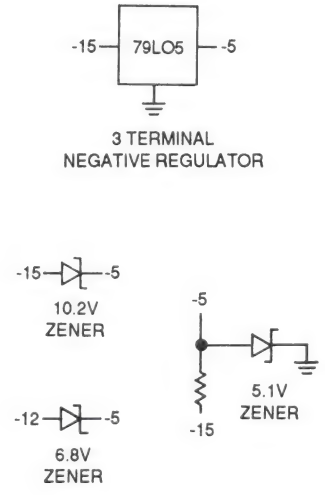


FIGURE 15. TYPICAL -5V CIRCUITS

TABLE 5. PIN OUT (40 PIN) RDC-19220

#	NAME	DESCRIPTION	#	NAME	DESCRIPTION
1	A	Resolution Control	40	+5V	Power Supply
2	B	Resolution Control	39	$\overline{EL}$	Enable LSBs (see note)
3	$\overline{INH}$	Inhibit	38	Bit 16	LSB
4	+REF	+Reference Input	37	Bit 8	
5	-REF	-Reference Input	36	Bit 15	
6	-VCO	Neg VCO Input	35	Bit 7	
7	-VSUM	Vel Sum Point	34	Bit 14	
8	VEL	Velocity Output	33	Bit 6	
9	+C	Signal Input	32	Bit 13	
10	COS	Signal Input	31	Bit 5	
11	-C	Signal Input	30	Bit 12	
12	+S	Signal Input	29	Bit 4	
13	SIN	Signal Input	28	Bit 11	
14	-S	Signal Input	27	Bit 3	
15	-5V	Power Supply	26	Bit 10	
16	R_S	Sampling Set	25	Bit 2	
17	R_C	Current Set	24	Bit 9	
18	$\overline{EM}$	Enable MSBs	23	Bit 1	MSB
19	A GND	Analog Ground	22	CB	Converter Busy
20	GND	Ground	21	$\overline{BIT}$	Built-In-Test

Note:
When -5V is applied to pin 39 ($\overline{EL}$), Converter Busy (CB) becomes Zero Index (ZI).

TABLE 6. PIN OUT (28 PIN) RDC-19221

#	NAME	#	NAME
1	B	28	A
2	$\overline{INH}$	27	+5V
3	+REF	26	$\overline{EL}$
4	-REF	25	Bits 8/16 (LSB)
5	-VCO	24	Bits 7/15
6	-VSUM	23	Bits 6/14
7	VEL	22	Bits 5/13
8	+C	21	Bits 4/12
9	+S	20	Bits 3/11
10	-5V	19	Bits 2/10
11	R_S	18	Bits 1(MSB) /9
12	R_C	17	CB
13	$\overline{EM}$	16	BIT
14	A GND	15	GND

Note:
When -5V is applied to pin 26 ($\overline{EL}$), Converter Busy(CB) becomes Zero Index (ZI).

TABLE 7. PIN OUT (44 PIN) RDC-19222

#	NAME	#	NAME
1	$\overline{EL}$	44	Bit 16 (LSB)
2	+5V	43	Bit 8
3	A	42	Bit 15
4	B	41	Bit 7
5	$\overline{INH}$	40	Bit 14
6	+REF	39	Bit 6
7	-REF	38	Bit 13
8	-VCO	37	Bit 5
9	-VSUM	36	Bit 12
10	VEL	35	Bit 4
11	+C	34	Bit 11
12	COS	33	Bit 3
13	-C	32	Bit 10
14	+S	31	Bit 2
15	SIN	30	Bit 9
16	-S	29	Bit 1 (MSB)
17	-5V	28	CB
18	R_S	27	$\overline{BIT}$
19	R_C	26	+5C (+5V)
20	$\overline{EM}$	25	+CAP
21	A GND	24	GND
22	-5C(-5V)	23	-CAP

Notes:
1. When -5V is applied to pin 1 ($\overline{EL}$), Converter Busy (CB) becomes Zero Index (ZI).
2. When using the built-in -5V inverter: connect pin 2 to 26, pin 17 to 22, and a 10 µF/10Vdc capacitor from pin 23 (negative terminal) to pin 25 (positive terminal). Connect a 47 µF/10Vdc capacitor from -5V to GND. The current drain from the +5V supply doubles. No external -5V supply is needed.

TABLE 8. PIN OUT (40 PIN, 5V ONLY) RDC-19223

#	NAME	#	NAME
1	$\overline{EL}$	40	Bit 16 (LSB)
2	+5V	39	Bit 8
3	A	38	Bit 15
4	B	37	Bit 7
5	$\overline{INH}$	36	Bit 14
6	+REF	35	Bit 6
7	-REF	34	Bit 13
8	-VCO	33	Bit 5
9	-VSUM	32	Bit 12
10	VEL	31	Bit 4
11	+C	30	Bit 11
12	+S	29	Bit 3
13	-5V	28	Bit 10
14	R_S	27	Bit 2
15	R_C	26	Bit 9
16	$\overline{EM}$	25	Bit 1 (MSB)
17	A GND	24	CB
18	-5C (-5V)	23	$\overline{BIT}$
19	-CAP	22	+5C (+5V)
20	GND	21	+CAP

Notes:
1. When -5V is applied to pin 1 ($\overline{EL}$), Converter Busy (CB) becomes Zero Index (ZI).
2. When using the -5V inverter: connect pin 2 to 22, pin 13 to 18, and a 10 µF/10Vdc capacitor from pin 19 (negative terminal) to pin 21 (positive terminal). Connect a 47 µF/10Vdc capacitor from -5V to GND. The current drain from the +5V supply doubles. No external -5V supply is needed..
3. Signal inputs are single-ended.

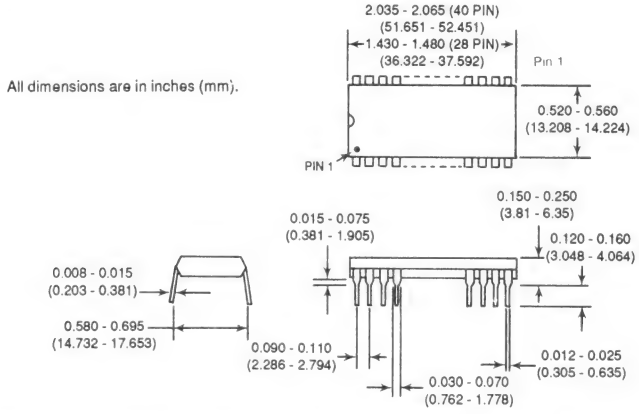


FIGURE 16. RDC-19220/RDC-19223 (40 PIN DDIP) AND RDC-19221 (28 PIN DDIP) MECHANICAL OUTLINE

E

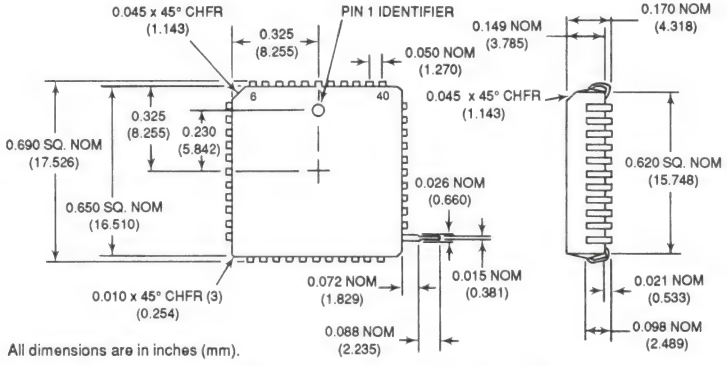


FIGURE 17. RDC-19222 (44 LEAD PLCC) MECHANICAL OUTLINE

ORDERING INFORMATION

RDC- 19220 - 3 0 2

Accuracy:
- 1 = 8 min + 1 LSB (0 to +70°C only)
- 2 = 4 min + 1 LSB
- 3 = 2 min + 1 LSB

Reliability:
- 0 = standard DDC procedures
- 2 = 168 hour burn-in at 125°C (-55 to +125°C only)

Operating Temperature Range:
- 1 = -55 to +125°C
- 2 = -40 to +85°C
- 3 = 0 to +70°C

Package:
- 0 = 40 pin DDIP*
- 1 = 28 pin DDIP ceramic
- 2 = 44 pin PLCC
- 3 = 40 pin DDIP* with 5V-only option

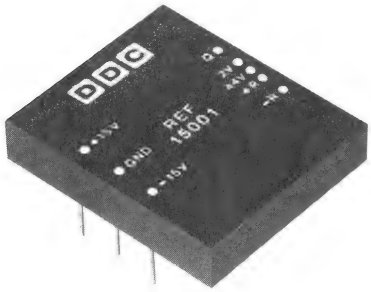
*plastic for -20X and -30X

Consult factory for input thin-film resistor networks.

B

REF-15001 SERIES

SYNCHRO/RESOLVER/INDUCTOSYN REFERENCE OSCILLATOR



DESCRIPTION

The REF-15001 Series provides reference excitation for synchros, resolvers and Inductosyns in systems where an AC reference is not readily available. Pin programmable for three different voltage levels, 11.8V, 4.4V, and 2.0V, the unit can be used with a wide variety of standard synchros, resolvers or Inductosyns. The output is fully protected against over current, short circuits and voltage transients. With a choice of 2.5 KHz or 10 KHz frequencies, the REF-15001 Series can be used in high speed servo systems requiring good dynamic response.

Able to drive up to 6 synchro/resolver/Inductosyn and converter pairs, the unit is ideally suited to computer controlled servos and programmable controllers found in robotics, machine control, and motor control applications.

FEATURES

- *DRIVES UP TO 6 RESOLVERS, SYNCHROS OR INDUCTOSYNS*
- *2.5 KHz OR 10 KHz FOR HIGH SPEED APPLICATIONS*
- *11.8V, 4.4V OR 2.0V OUTPUT*
- *FULLY PROTECTED OUTPUT*
- *15 VDC OPERATION*
- *NO TRIMS OR ADJUSTMENTS*

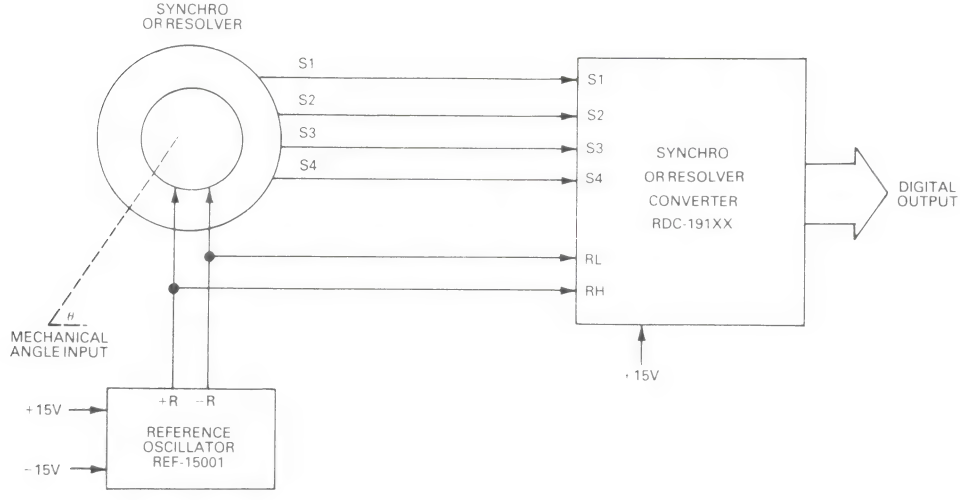


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS Apply over temperature and power supply ranges	
PARAMETER	**VALUE**
FREQUENCY	
REF-15001	2.5 KHz ± 10%
REF-15002	10 KHz ± 10%
OUTPUT	
Voltage	
+R to −R	11.8V rms ± 10%
+R to −GND (4.4 tied to +R)	4.4V rms ± 10%
+R to −GND (2.0 tied to +R)	2.0V rms ± 10%
DC Offset	±20mV, max
Capacitive Load	0.1 μF, max
Current	110 mA, max
Protection	Overcurrent, short circuit and voltage transient
Quadrature Reference	12V rms ± 10% at 1.0 mA
POWER SUPPLIES	
Voltage	±15VDC, ±5%
Current	
No Load	50 mA
Full Load	160 mA
Maximum Voltage (without damage)	±18VDC
TEMPERATURE RANGE	
Operating	0°C to +70°C
Storage	−55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size	1.52 x 1.78 x 0.35 in. (39 x 45 x 9 mm)
Weight	0.9 oz, (25.5 gm)

TECHNICAL INFORMATION

SYNCHRO/RESOLVER APPLICATIONS

The REF-15001 is designed for use with most common synchros, resolvers and converters operating with 11.8V, 4.4V, or 2.0V references at 2500 Hz. It can drive up to 110 mA. It is not intended for use in torque repeater/indicator applications.

A typical interconnection is shown in Figure 1. No trims or adjustments are required. Output voltage levels are pin programmed as specified in Table 1.

TABLE 1 OUTPUT PROGRAMMING

REFERENCE OUTPUT VOLTAGE	AT PINS	JUMPER CONNECTIONS
11.8V rms	+R to −R	None
4.4V rms	+R to GND	Pin 4.4 to +R
2.0V rms*	+R to GND	Pin 2.0 to +R

*Recommended for Inductosyn Applications

The 11.8V rms output is intended for use with resolvers having a 1:1 transformation ratio and operating into a converter requiring a 11.8V L-L input. The 4.4V rms output is intended for use with synchros or resolvers having a transformation ratio of 26:11.8 and operating into a direct input converter requiring 2.0V L-L input. The 2.0V rms output is for use with resolvers having a 1:1 transformation ratio and operating into a converter requiring a 2.0V L-L input.

E

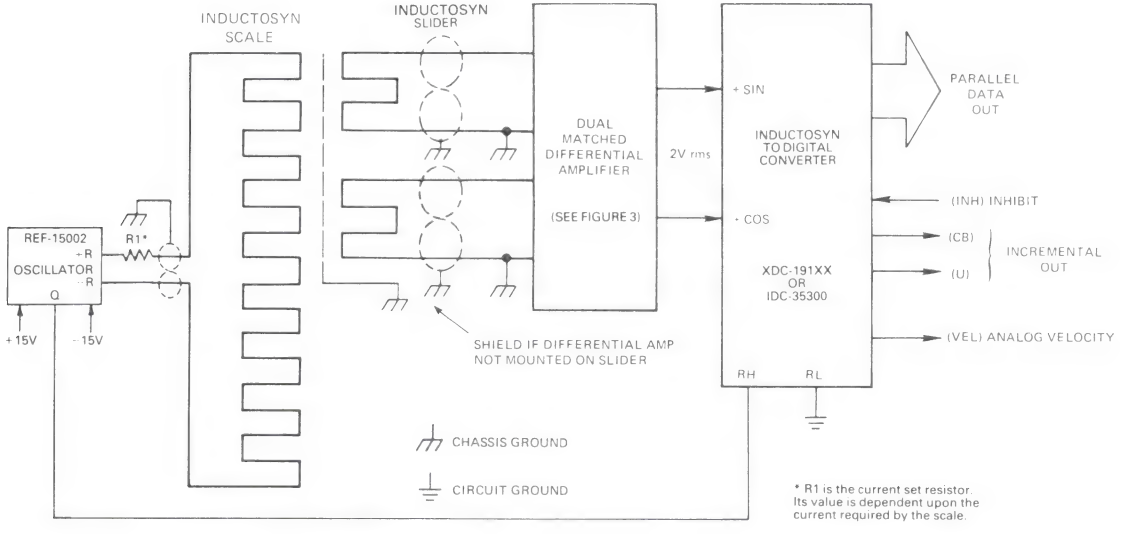
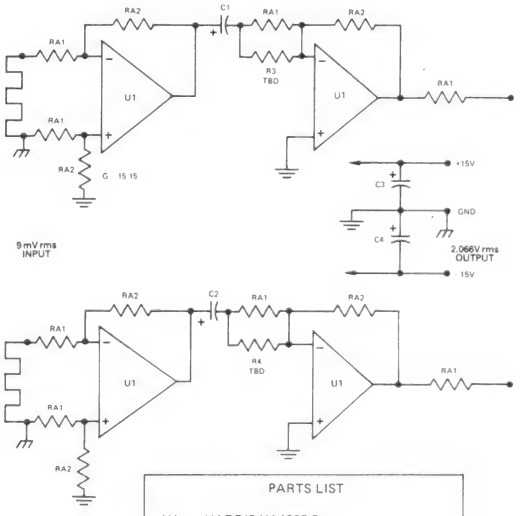


FIGURE 2. TYPICAL INDUCTOSYN CONNECTION.

INDUCTOSYN APPLICATIONS

The REF-15002 can drive up to 110 mA and is designed for use with Inductosyns operating at 10 KHz. It is recommended that the unit be suitably programmed as indicated in Table 1 for the correct current level required for the specific Inductosyn. A typical interconnection is shown in Figure 2. No trims or adjustments are required on the converter. Note the Inductosyn is driven from the +R and −R pins while the converter reference is taken from the Q pin. This is a 12V rms, 1 mA output in quadrature with +R and −R and is correctly compensated for the phase shift of Inductosyns. Figure 3 illustrates the circuit needed between the inductosyn slider and the converter.



PARTS LIST

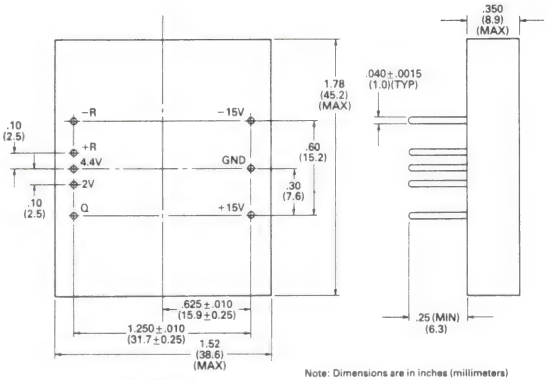
U1	HARRIS HA4605-5
RA1	BECKMAN 698-3-R330D
RA2	BECKMAN 698-3-R5KD OR 699-3-R5KD
C1,2	22 μf 2VDC
C3,4	1 μf 35VDC
R3,4	TBD (NOT USUALLY NEEDED)

NOTES: 1. For other input levels select RA1 and RA2 as required. Standard values are: 100, 200, 330, 470, 500, 1K, 2K, 2.2K, 4.7K, 5K, 10K, 15K, and 20KΩ.

2. For lower input levels use Harris HA-4625-5

FIGURE 3. DUAL MATCHED DIFFERENTIAL AMPLIFIER

MECHANICAL OUTLINE



BOTTOM VIEW

Note: Dimensions are in inches (millimeters)

ORDERING INFORMATION

REF-1500X-300

- Temperature Range (operating): 3=0°C to +70°C
- Options: 1=2.5 KHz, 2=10 KHz

The information provided in this Data Sheet is believed to be accurate; however, no responsibility is assumed by ILC Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

REF-15003/04

15VA PROGRAMMABLE REFERENCE POWER OSCILLATOR

Advance Information

DESCRIPTION

The REF-15003 and REF-15004 are a family of modular 15VA power oscillators. They are digitally programmable for frequency and voltage level or by pin strapping, and ac mains supply the operating power.

APPLICATIONS

With their high reliability, low cost, and accuracy the REF-15003 and REF-15004 are perfect for many synchro and resolver based systems that require high voltage and power. Furthermore, because of their ability to generate the 26 volts and 115 volts at 400Hz, commonly found in military aircraft and shipboard systems, they are ideal for automated test and simulation system use. Other uses for this flexible oscillator include reference source for industrial resolver based encoding systems, incoming and production test set-ups, and as a laboratory synchro/resolver/inductosyn/LVDT/RVDT reference.

Features

- ***Programmable Voltage and Frequency***
- ***REF-15003:***
  0 to 26 volts,
  360 to 10kHz
- ***REF-15004:***
  0 to 115 volts,
  360 to 2kHz
- ***15VA Output***
- ***115/230Vac, 47 to 63Hz Input***

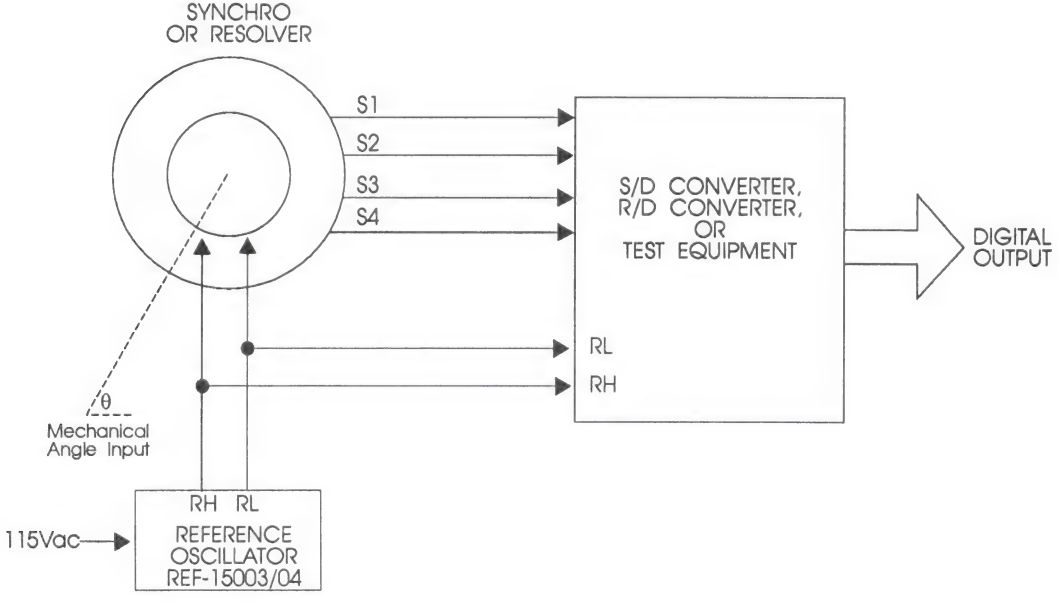
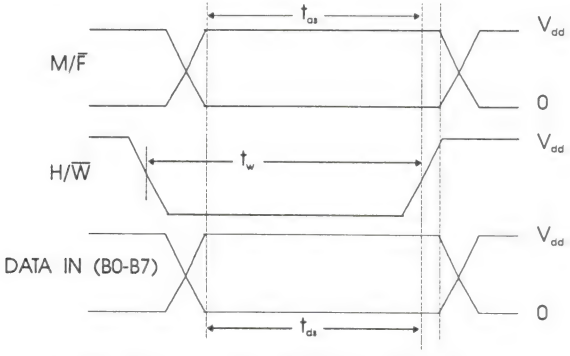


FIGURE1. BLOCK DIAGRAM FOR DRIVING SYNCHRO OR RESOLVER

ADVANCE SPECIFICATIONS		
PARAMETER	**UNIT**	**VALUE**
O UTPUT(OUT/GND)		
Power	W,VA	15 min.
Voltage		
■ REF-15003	V	0-26
■ REF-15004	V	0-115
■ Accuracy	%	±5
Frequency		
■ REF-15003	Hz	360 - 10k
■ REF-15004	Hz	360-2k
■ Accuracy	%	±5
DIGITAL INPUT		
Logic Type		CMOS
Inputs		
■ Logic 0	V	0.8max.
■ Logic 1	V	2.4 min.
■ Loading	µA/pF	10/30 max.
■ Data Bits (B0-B7)		8-bit binary word, B0=LSB, B7=MSB
■ Magnitude/$\overline{\text{Frequency}}$ Select (M/$\overline{\text{F}}$)		Logic 1= volt. magnitude, Logic 0 = freq.
■ Hold/$\overline{\text{Write}}$ (H/$\overline{\text{W}}$)		Logic 1=hold, Logic 0= write or transparent
■ M/$\overline{\text{F}}$ Select to Write Setup Time (t_{as})	ns	300 min. (see figure 2)
■ Data Valid to Write Setup Time (t_{ds})	ns	300 min. (see figure 2)
■ M/$\overline{\text{F}}$ Select to Write Hold Time (t_{ah})	ns	20 min. (see figure 2)
■ Data Valid to Write Hold Time (t_{dh})	ns	20 min. (see figure 2)
■ $\overline{\text{Write}}$ Pulse Width (t_w)	ns	300 min. (see figure 2)
DIGITAL OUTPUT		
$\overline{\text{BIT}}$		Logic 1= normal operation, Logic 0= volt. output overcurrent indicator
MAGNITUDE SELECT		
Digital Control		connect M to MD
Resistor Control		connect M to MR
■ Resistor Value	kOhms	$R=((V_{fs}/V_{sel})-1) \times 8$
FREQUENCY SELECT		Digitally controlled per above, or hardwired D0 - D7 to: GND for logic 0; or V_{dd} for logic 1 (with M/$\overline{\text{F}}$ wired to V_{dd} and H/$\overline{\text{W}}$ wired to GND)
POWER INPUT CHARACTERISTICS		
Voltage	V	115/230
Frequency	Hz	47-63
Current		
■ No Load	mA rms	50/25 max.
■ Load	mA rms	10/5 per VA out
TEMPERATURE RANGES		
Operating	°C	–40 to +85
Storage	°C	–55 to +125
PHYSICAL CHARACTERISTICS		
Size	in(cm)	6 x 3 x 1.4 (15.24 x 7.62 x 3.56)
Weight	lb(kg)	4 max.(1.81)
CONNECTOR		DB25 with male pins

ORDERING INFORMATION

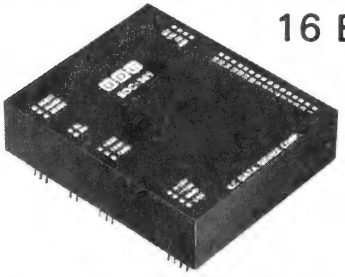
Consult factory



A **FIGURE 2. WRITE CYCLE TIMING DIAGRAM**

DDC
ILC DATA DEVICE CORPORATION

SDC-361/362



16 BIT TWO-SPEED S/D AND R/D CONVERTER
Single Module with Internal Transformers

DESCRIPTION

The SDC-361 is a low-cost, single module synchro to digital and resolver to digital tracking converter. A unique control transformer algorithm is used that provides inherently higher accuracy and jitter-free output. Other features include a BIT logic signal to indicate proper tracking and an analog velocity output. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate, and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustments.

APPLICATIONS

The SDC-361 may be used wherever analog angle data from 1 and 36 speed† synchros or resolvers must be converted rapidly and accurately to digital form for transmission, storage or analysis. Because these units are extremely rugged and stable, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation and collision avoidance systems.

† All references to 1 and 36 speed apply to SDC-361. SDC-362 is 1 and 18 speed.

FEATURES

- *ACCURACY: ±1 LSB = 20 seconds*
- *SIGNAL AND REF INPUTS:*
  Internal transformer isolation
  Broadband input: 350–3000 Hz or 47–3000 Hz
  All common L-L voltage levels
- *LOGIC:*
  TTL compatible
  16 bit parallel binary angle output
  Converter Busy, Inhibit and BIT
- *POWER REQUIRED:*
  ±15V DC and +5V DC

E

SPECIFICATIONS

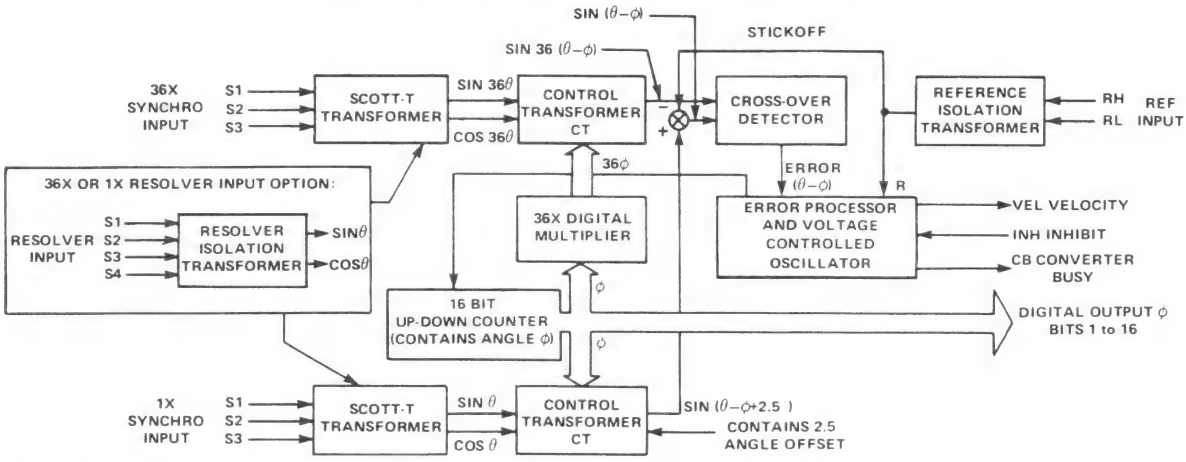
Apply over temperature range, power supply range, reference frequency range, ±10% signal & reference amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 bits
ACCURACY	
SDC-361	±1 LSB (20 sec)
SDC-362	±2 LSB (40 sec)
SIGNAL AND REFERENCE INPUT	
Synchro Input*	Signal Frequency Range / Signal Input Impedance (L-L Balanced, Resistive)
90V L-L, 400 Hz (Option H)	350–3000 Hz / 148 KΩ min
90V L-L, 60 Hz (Option I)	47–3000 Hz / 148 KΩ min
11.8V L-L, 400 Hz (Option L)	350–3000 Hz / 19 KΩ min
Resolver Input*	
90V L-L, 400 Hz (Option H)	350–3000 Hz / 148 KΩ min
26V L-L, 400 Hz (Option M)	350–3000 Hz / 42 KΩ min
11.8V L-L, 400 Hz (Option L)	350–3000 Hz / 19 KΩ min
Reference Input*	Reference Voltage Range / Ref. Input Impedance (Resistive)
Options H, I	40–150V rms / 300 KΩ min
Options M, L	10–50V rms / 80 KΩ min
*Transformer isolated. Other voltages and frequencies available on special order.	
DIGITAL INPUT/OUTPUT	
Logic Type	TTL
Inhibit Input (INH)	Logic "0" inhibits
Loading	0.2 Std. TTL loads plus 18 KΩ min pull-up resistor to +5V supply
Outputs	
16 Parallel Data Bits	Natural binary angle; positive logic
Converter Busy (CB)	1–2.5μsec positive pulse data changes on leading edge
Drive Capability	2 Std. TTL loads (5 Std. load capability available on special order – consult factory)
Bit (Built In Test)	Logic 0 = normal tracking Logic 1 = not tracking within fine speed range
ANALOG VELOCITY OUTPUT	
Scale Factor	±1.0V DC ±30% for 100 /sec at 400 Hz ±1.0V DC ±30% for 25 /sec at 60 Hz
Range	±10V DC min
Loading	±10 KΩ max

PARAMETER	VALUE
DYNAMIC CHARACTERISTICS	
Input Rate for Full Accuracy	
Options H, M, L (400 Hz)	0–1000°/sec minimum
Option I (60 Hz)	0–250°/sec minimum
Acceleration for 1 LSB Lag	
Options H, M, L (400 Hz)	384°/sec² typ
Option I (60 Hz)	23°/sec² typ
Settling Time	
For Normal Tracking (Up to Specified Input Rate)	No lag error
For 179° Step Change (Typical Values)	
Options H, M, L (400 Hz)	
Settling to 1 LSB	400 msec
Settling to Final Value	480 msec
Option I (60 Hz)	
Settling to 1 LSB	1400 msec
Settling to Final Value	1800 msec
Velocity Constant (Type II Servo Loop)	$K_V = \infty$
Acceleration Constant	–
Options H, M, L (400 Hz)	K_A = 70,000 nominal
Option I (60 Hz)	K_A = 4,300 nominal

POWER SUPPLIES	+15V Supply	–15V Supply	+5V Logic Supply
Nominal Voltage			
Voltage Range	+11 to +16.5V	–11 to –16.5V	+4.5 to +5.5V
Max. Voltage Without Damage	+18V	–18V	7V
Current			
Typical	10 mA	35 mA	110 mA
Maximum	15 mA	50 mA	150 mA

TEMPERATURE RANGES	
Operating	
–1 Option	–55°C to +105°C
–3 Option	0°C to +70°C
Storage	–55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 x 2.625 x 0.82 inch (79.4 x 66.7 x 20.8mm)
Weight	7 oz (200 g)



NOTE: Block Diagram Illustrates SDC-361. All References to "36x" are "18x" for SDC-362.

BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

The operation of a two-speed S/D is essentially the same as a single speed except there are two control transformers (CT) which generate two error voltages. These two CTs are fed by a common up-down counter with the counter data multiplied by 36 for the fine speed CT.

Assuming an off-null condition, as when the system is first energized, the crossover detector feeds the coarse (1X) CT error signal output to the demodulator and error processor. The converter seeks a null as it would for a single speed S/D. As null is approached (to within 2.5° nominally) the coarse CT output drops below a preset threshold and the crossover detector then switches the fine (36X) CT error signal into the demodulator and error processor.* Since the counter angle θ is multiplied by 36, the gradient of the fine speed CT is 36X the coarse (1X) CT output. The servo loop then is able to seek an even finer null, using the fine speed CT error signal. The converter will continue to use the fine error signal for continuous tracking, switching back to the coarse signal only when the coarse error exceeds the crossover threshold. In order to eliminate false stable nulls of 180° an angle offset and stickoff voltage are introduced in the coarse channel.

The ±15V power supplies can vary over their specified ranges with no change in the converter specifications except for a proportional change in the maximum ± tracking rates. When testing or evaluating the converters, it is advisable to limit the current to each of the three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specifications table.

To prevent damage to the input transformers, the maximum voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500V.

*SDC-362 is (18x) where all references to (36x) occurs in text and diagrams.

DIGITAL OUTPUTS

Logic outputs are low power Schottky and they can drive remote loads.

The BIT logic output is a built in test derived from the crossover detector. It goes to logic 1 whenever the digital output is not tracking the input signal within the range of the fine speed synchro or resolver.

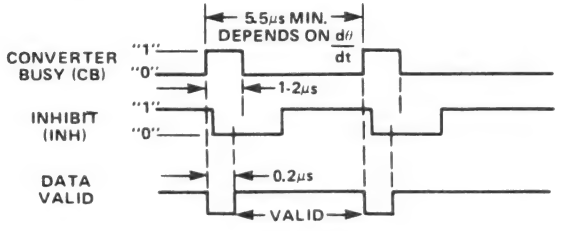
Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	108.75
8	1.405	84.38
9	0.7081	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0379	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	.66
16	0.0055	.33

BIT WEIGHT TABLE

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The output data change is initiated at the leading edge of the CB pulse, and the output is stable within 0.2μsec after the leading edge. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.2μsec, (c) transfer the data, and (d) release the inhibit.



TIMING DIAGRAM

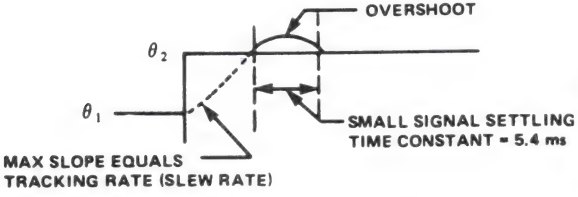
ANALOG VELOCITY OUTPUT

VEL is a DC voltage proportional to the angular velocity $d\theta/dt = d\phi/dt$. The output is derived from an op-amp with low output impedance and is short circuit proof. Other characteristics are listed in the specifications table.

DYNAMIC PERFORMANCE

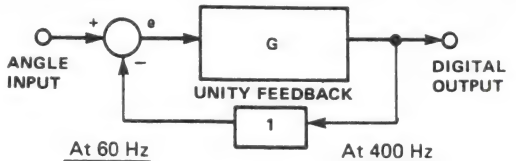
A Type II servo loop ($K_V = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the ±15 VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The +15V supply voltage will determine the positive maximum velocity, and the −15V supply voltage will determine the negative maximum velocity.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal setting time.



RESPONSE TO A STEP INPUT

The loop dynamics of DDC's tracking S/D converters are described by the unity feedback configuration shown. The closed-loop transient response is nominally critically damped, and all loop dynamics can be determined from the diagram and formulas given.



$$G = \frac{66^2\left(\frac{S}{33}+1\right)}{S^2\left(\frac{S}{330}+1\right)} \quad \text{At 60 Hz}$$

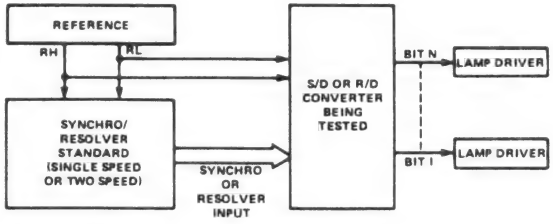
$$G = \frac{266^2\left(\frac{S}{133}+1\right)}{S^2\left(\frac{S}{1330}+1\right)} \quad \text{At 400 Hz}$$

S/D CONVERTER LOOP DYNAMICS

ACCURACY TESTS

Because of the high accuracy of DDC's S/D converters, only laboratory-grade synchro or resolver substitution boxes or standards should be used. If synchro standards are not available, arrangements may be made to witness the final source inspection at the DDC factory.

The figure below shows how to arrange test equipment for measuring the accuracy of S/D converters. A separate lamp driver or suitable readout is required for each of the output data lines. The synchro standard is set to any desired test angle, and the lamps which are on are added according to their bit weights and compared with the test angle.



ACCURACY TEST CIRCUIT

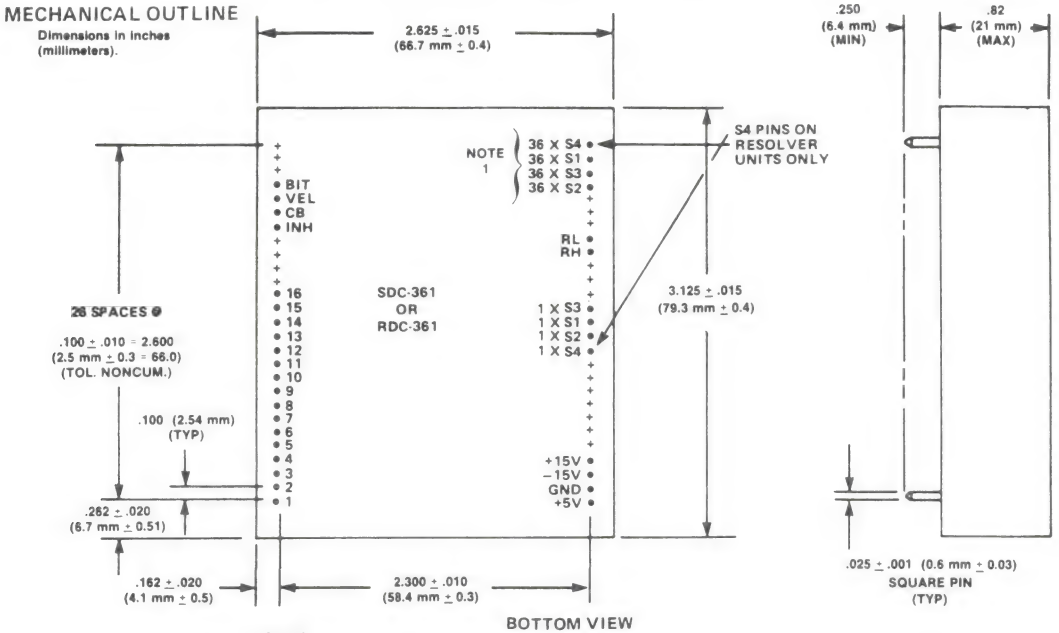
PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

MECHANICAL OUTLINE

Dimensions in inches (millimeters).



BOTTOM VIEW

NOTES:

1. All reference to 36x become 18x on model SDC-362
2. Pin labels on bottom view are for reference only.
3. All dimensions shown are in inches.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type sdg-F.
6. Pins S4 are present on resolver units only.

ORDERING INFORMATION

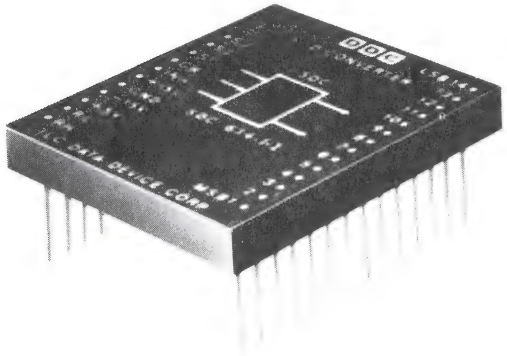
SDC – 361 – H – 1

- Temperature Range:
  1 = –55° C to +105° C
  3 = 0° C to +70° C
- Signal Input Voltage and Frequency:
  H = 90 V L-L, 400 Hz (Synchro or Resolver)
  I = 90 V L-L, 60 Hz (Synchro only)
  M = 26 V L-L, 400 Hz (Resolver only)
  L = 11.8 V L-L, 400 Hz (Synchro or Resolver)
- Speed:
  361 = 1 x 36 Speed
  362 = 1 x 18 Speed
- Input Type:
  SDC = Synchro
  RDC = Resolver

DDC
ILC DATA DEVICE CORPORATION

SDC-630/632/634*

10, 12 OR 14 BIT S/D OR R/D CONVERTER
Low Profile; Internal Transformers



DESCRIPTION

The SDC 630, 632 and 634* series are low cost, low profile synchro to digital and resolver to digital tracking converters with standard pin configurations. They use a unique control transformer algorithm that provides inherently higher accuracy and jitter-free output. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustments or calibrations in the field.

APPLICATIONS

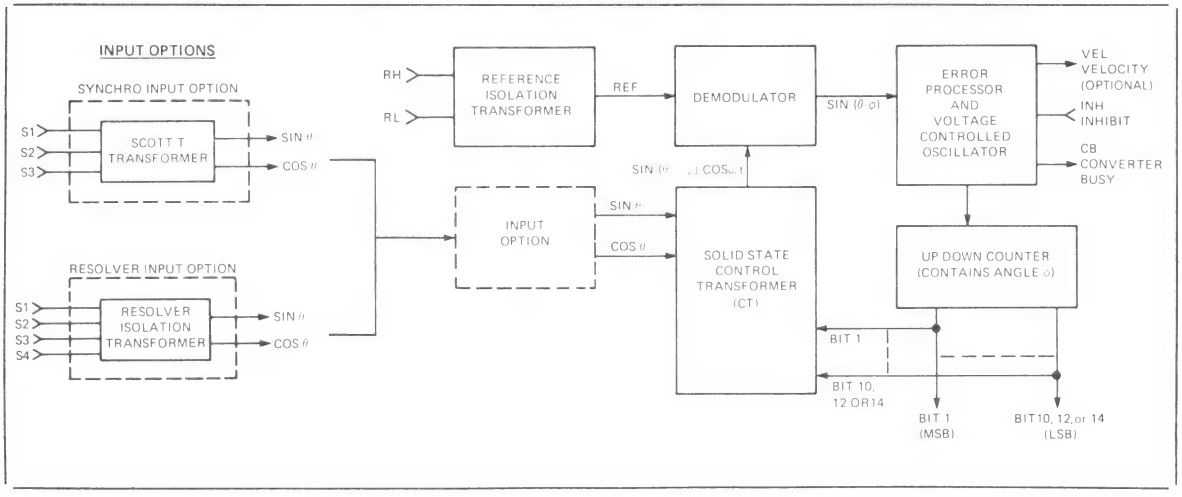
These converters may be used wherever analog angle data from a synchro or resolver must be converted rapidly and accurately to digital form for transmission, storage or analysis. Because these units are extremely rugged and stable, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation, and collision avoidance systems.

FEATURES

- *STANDARD LOW PROFILE CONVERTERS WITH OPTIONAL VELOCITY OUTPUT*
- *ACCURACY:*
  10 BIT: ±21 MINUTES
  12 BIT: ±8.5 MINUTES
  14 BIT: ±4 MIN ±0.9 LSB OR ±2.6 MIN (HIGH ACCURACY)
- *SIGNAL AND REF INPUT:*
  INTERNAL TRANSFORMER ISOLATION
  ALL COMMON L-L LEVELS AND FREQUENCIES
- *LOGIC:*
  TTL COMPATIBLE
  PARALLEL BINARY ANGLE OUTPUT
  CONVERTER BUSY AND INHIBIT
- *POWER REQUIRED:*
  ±15V DC AND +5V DC

*Patented

E



SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE		
	SDC-630	SDC-632	SDC-634
RESOLUTION	10 bits	12 bits	14 bits
ACCURACY			
Standard Units	±21 min	±8.5 min	±4 min ±0.9 LSB
High Accuracy Option	–	–	±2.6 min
SIGNAL AND REFERENCE INPUT			
Synchro Input*:	Signal Frequency Range		Signal Input Impedance (L-L Balanced, Resistive)
90V L-L, 400 Hz (Option H)	350–1000 Hz		148 KΩ min
90V L-L, 60 Hz (Option I)	47–1000 Hz		148 KΩ min
11.8V L-L, 400 Hz (Option L)	350–1000 Hz		19 KΩ min
Resolver Input*:			
90V L-L, 400 Hz (Option H)	350–1000 Hz		**198** KΩ min
26V L-L, 400 Hz (Option M)	350–1000 Hz		**57** KΩ min
11.8V L-L, 400 Hz (Option L)	350–1000 Hz		**26** KΩ min
Reference Input*:	Reference Voltage Range		Ref. Input Impedance (Resistive)
Options H, I	40–150V rms		300 KΩ min
Options M, L	10–50V rms		80 KΩ min
*Transformer isolated. Other voltages and frequencies available on special order.			
DIGITAL/INPUT OUTPUT			
Logic Type	TTL		
Inhibit Input (INH) Loading	Logic "0" inhibits 0.2 Std. TTL loads plus 18 KΩ min pull-up resistor to +5V supply		
Outputs			
Type	Low power Schottky (can drive remote loads)		
10, 12, or 14 Parallel Data Bits	Natural binary angle, positive logic		
Converter Busy (CB)	0.5 to 1.5μsec positive pulse. Data changes on leading edge		
Drive Capability	2 Std. TTL loads		
VELOCITY OUTPUT (ON SPECIAL ORDER ONLY)			
Type	Derived from an op-amp with low impedance output Positive output for increasing angle		
Voltage Range	±10V min		
Scale Factor (For SDC-634 – Others on Request)			
Options H, M, and L	6V per rps nominal (10V ÷ 15 rps)		
Option I	3.3V per rps nominal (10V ÷ 2.7 rps)		

DYNAMIC CHARACTERISTICS	MIN	TYP	MIN	TYP	MIN	TYP
Input Rate for Full Accuracy (Min Range)						
Options H, M, L (400 Hz)	0-22 rps	40	0-40 rps	50	0-10 rps	15
Option I (60 Hz)	0-8 rps	10	0-10 rps	12.5	0-1.25 rps	3
Acceleration for 1 LSB Lag						
Options H, M, L (400 Hz)	12,600 /sec² typ		4500 sec² typ		610 sec² typ	
Option I (60 Hz)	770 /sec² typ		295 sec² typ		20 sec² typ	
Settling Time						
For Normal Tracking (Up to Specified Input Rate)	No lag error		No lag error		No lag error	
For 179° Step Change (Typical Values)						
Options H, M, L (400 Hz)						
Settling to 1 LSB	80 msec		90 msec		150 msec	
Settling to Final Value	100 msec		110 msec		200 msec	
Option I (60 Hz)						
Settling to 1 LSB	300 msec		300 msec		800 msec	
Settling to Final Value	500 msec		360 msec		1000 msec	
Velocity Constant (Type II servo loop)	$K_V = \infty$		$K_V = \infty$		$K_V = \infty$	

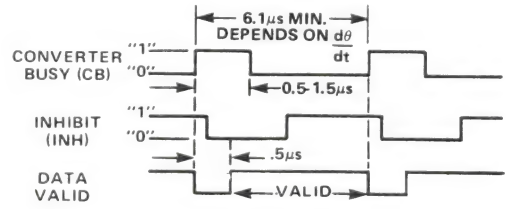
PARAMETER	VALUE		
	SDC-630	SDC-632	SDC-634
DYNAMIC CHARACTERISTICS (Cont'd)			
Acceleration Constant (Nominal Values)			
Options H, M, L (400 Hz)	K_a = 36,000 sec²	K_a = 54,000 sec²	K_a = 27,800 sec²
Option I (60 Hz)	K_a = 2,200 sec²	K_a = 3,600 sec²	K_a = 900 sec²
POWER SUPPLIES			
Nominal Voltage	+15V Supply	-15V Supply	+5V Logic Supply
Voltage Range	+11 to +16.5V	-11 to -16.5V	+4.5 to +5.5V
Max. Voltage Without Damage	+18V	-18V	7V
Current			
SDC-630 (632) Typical	8 mA (4)	18 mA (18)	80 mA (80)
Maximum	13 mA (6)	30 mA (30)	120 mA (120)
SDC-634 Typical	10 mA	20 mA	100 mA
Maximum	15 mA	30 mA	150 mA
TEMPERATURE RANGES			
Operating			
–1 Option	–55°C to +105°C		
–3 Option	0°C to +70°C		
Storage	–55°C to +125°C		
PHYSICAL CHARACTERISTICS			
Size (Encapsulated Module)	3.125 x 2.625 x 0.43 inch (7.94 x 6.67 x 1.07 cm)		
Weight	4 oz (113 g)		

TECHNICAL INFORMATION

TIMING

The figure below shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy impulse (CB). The CB is a positive pulse 0.5 to 1.5μsec long. Data changes on the leading edge of the CB pulse, and data can be transferred 0.5μsec after the leading edge.

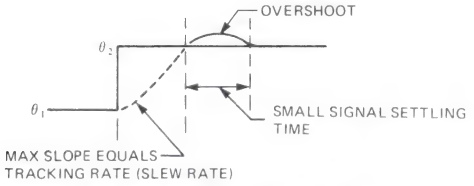
The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.5μs, (c) transfer the data, and (d) release the inhibit. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH.



DYNAMIC PERFORMANCE

A type II servo loop (KV =. ∞) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the +15 VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The +15 V supply voltage will determine the positive maximum velocity, and the −15 V supply voltage will determine the negative maximum velocity.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to a final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The nominal open loop transfer function is given by

$$G = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where the parameters A and B are:

		SDC-630	SDC-632	SDC-634
400 Hz	A	190 sec^{-1}	226 sec^{-1}	167 sec^{-1}
	B	91 sec^{-1}	100 sec^{-1}	56 sec^{-1}
60 Hz	A	46 sec^{-1}	58 sec^{-1}	30 sec^{-1}
	B	23 sec^{-1}	26 sec^{-1}	10 sec^{-1}

POWER SUPPLIES

The main power supplies can vary over their specified ranges with no change in the converter specifications except for a proportional change in the maximum tracking rates.

When testing or evaluating the converters, it is advisable to limit the current to each of the three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specifications table.

TRANSFORMER INPUT

To prevent damage to the input transformers, the maximum steady state voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500 V.

ACCOMMODATING NON-STANDARD INPUT VOLTAGES

The signal and reference input levels of the SDC-630 series can be resistively scaled to accommodate non-standard voltages. A converter should be selected that is the next lower standard voltage and the voltage is then scaled up with resistors in series with the synchro and/or reference inputs.

For a synchro input (SDC), a resistor ^{R}SIG is added in series with S1, S2 and S3 , which is determined as follows:

^{R}SIG = 1.11K (New L-L Voltage − Standard Unit Voltage)

That is, 1.11K for each volt above that for which the standard unit is designed.

Example: An SDC-634-L (11.8V) is to be used at 50V L-L

^{R}SIG - 1.11K (50–11.8) = 42.4K

The closest available high grade resistor with a low temperature coefficient of resistance should be used, and the three resistors should be matched to each other as closely as possible. In general, a 0.1% difference will introduce 1.7 arc minutes of additional error due to the effect on $\frac{SIN}{COS}$ ratio relationship.

The ABSOLUTE value of the resistor is not critical.

In the case of the RESOLVER version (RDC), the equation is:

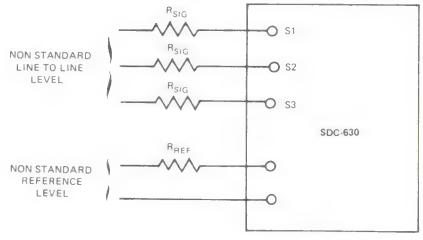
^{R}SIG = 2.2K (New L-L level − Standard Unit L-L level)

The calculated resistors are connected in series with S1 and S2 respectively. Note only two resistors required. The required resistor matching and its effect on accuracy, is the same as for a synchro input (See Figure).

The Reference Voltage treatment is similar, but the value selected is not critical.

^{R}Ref = 2.8K (New ref − standard ref)

Here, even a 10% tolerance is adequate.



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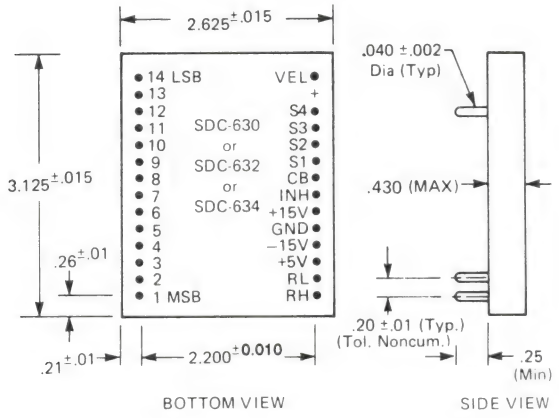
MECHANICAL OUTLINE



Notes:

1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
3. Pins 13 and 14 are omitted for SDC-632, and pins 11, 12, 13 and 14 are omitted for SDC-630.
4. Velocity output pin VEL is present only if requested on special order.
5. Pin S4 is present on Resolver units, and omitted on Synchro units.

ORDERING INFORMATION

If a socket is required, order socket number 9010.

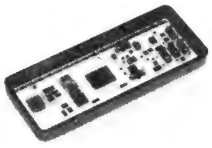
SDC–634–H–1–a–R

- R = Enhanced reliability
- High Accuracy Version
  ±2.6 Minutes (SDC-634 only)
- Temperature Range (operating):
  1 = −55° C to +105° C
  3 = 0° C to +70° C
- Signal Input Voltage and Frequency:
  H = 90V L-L, 400 Hz (Synchro or Resolver)
  I = 90V L-L, 60 Hz (Synchro only)
  M = 26V L-L, 400 Hz (Resolver only)
  L = 11.8V L-L, 400 Hz (Synchro or Resolver)
- Resolution:
  634 = 14 bits
  632 = 12 bits
  630 = 10 bits
- Input Type:
  SDC = Synchro
  RDC = Resolver

DDC
ILC DATA DEVICE CORPORATION

SDC-14531II

PROGRAMMABLE SYNCHRO/RESOLVER TO DIGITAL CONVERTER



DESCRIPTION

The SDC-14531II is a low-cost, high-reliability, programmable synchro/resolver-to-digital converter with Pin Programmable 14 Bit or 16 Bit resolution. Packaged in a 36 pin DDIP, the SDC-14531II features Built-In-Test (BIT) output.

The SDC-14531II series accepts a broadband input of 360 to 2.5kHz. Other features are solid-state signal and reference isolation and high common mode rejection.

The digital angle output from the SDC-14531II is a natural binary code, parallel positive logic and is TTL/CMOS compatible. Synchronization to a computer is accomplished with the Converter Busy (CB) output and/or the Inhibit ($\overline{INH}$) input.

APPLICATIONS

Because of its high reliability, small size, and low power consumption, the SDC-14531II is ideal for military ground or avionics applications. 883B processing is available.

Designed with three state output, the SDC-14531II is especially well suited for use with computer based systems. Among the many possible applications are radar and navigation systems, fire control systems, flight instrumentation, and flight trainers or simulators.

FEATURES

- ***Single 5V Power Supply***
- ***Accuracy to 1.3 Arc-Minutes***
- ***Pin Programmable Synchro/Resolver***
- ***Pin Programmable 14 Bit or 16 Bit***
- ***No 180° False Lock-up***
- ***Internal Synthesized Reference***
- ***Built-In-Test (BIT) Output***
- ***Low Power***
- ***Alternate Source for Model 1006, 1056***

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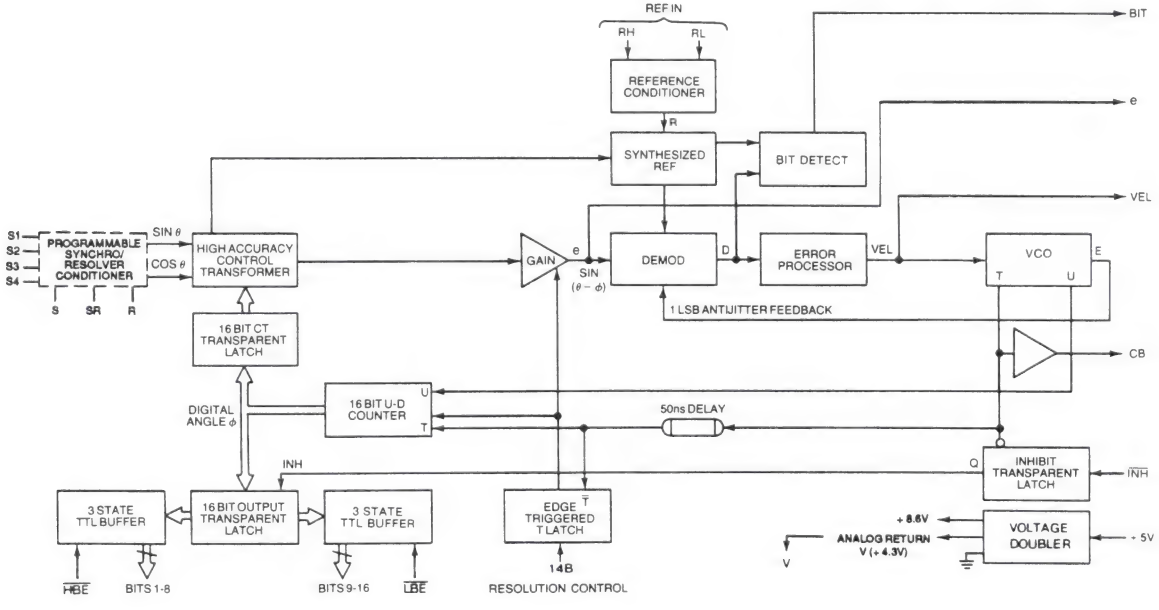


FIGURE 1. SDC-14531II BLOCK DIAGRAM

TABLE1. SDC-14531II SPECIFICATIONS

Specifications apply over temperature range, power supply range, reference frequency, and amplitude range; 15% signal amplitude variation, up to 10% harmonic distortion in the reference, and up to 45° of signal to reference phase shift.

PARAMETER	UNIT	VALUE
RESOLUTION	Bits	14 or 16
ACCURACY	Min	5.2, 2.6, or 1.3
REPEATABILITY	LSB	1max
REFERENCE INPUT CHARACTERISTICS		
Carrier Frequency Ranges:		
Nominal 400Hz Units	Hz	360 - 1000
Model -644	Hz	360 - 2500
Voltage Range	Vrms	4 - 130
Input Impedance:		
Single Ended	Ohm	250k min
Differential	Ohm	500k min
Common Mode Range	V	250 peak max
SIGNAL INPUT CHARACTERISTICS (voltage options and minimum input impedance)		
Input Impedance Inbalance	%	0.2max
		11.8V L-L / 90V L-L
Synchro mode	V	
Zin Line to Line	Ohm	60k / 500k
Zin Each Line to Gnd	Ohm	30k / 250k
Common Mode Range	V	30 max / 180 max
Resolver mode	V	11.8V L-L
Zin Single Ended	Ohm	30k
Zin Differential	Ohm	60k
Zin Each Line to Gnd	Ohm	30k
Common Mode Range	V	30 max
Model-644:		
Resolver mode only	V	11.8V L-L
Zin Single Ended	Ohm	23k
Zin Differential	Ohm	46k
Zin Each Line to Gnd	Ohm	23k
Common Mode Range	V	30 max
REFERENCE SYNTHESIZER		
± Sig/Ref Phase Shift	Deg	60 typ, 45 min
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs:		Logic 0 = 0.8V max Logic 1 = 2.0V min Loading = 10µa max
Inhibit ($\overline{INH}$)		Logic 0 inhibits Data stable within 0.5 µS
Resolution Control (14B)		Logic 1 for 14 bits Pull-up current source to +5V //5pF max CMOS transient protected
Enable Bits 1 to 8 ($\overline{HBE}$) Enable Bits 9 to 16 ($\overline{LBE}$)		Logic 0 enables Data Valid within 150ns Logic 1 = High Z Data High Z within 100ns Pull-down to GND.

TABLE1. SDC-14531II SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT (continued)		
Outputs:		
Parallel Data	Bits	14 or 16 parallel lines; natural binary angles, positive logic
Converter Busy (CB)		0.8 to 3.0µsec positive pulse; leading edge initiates counter update.
BIT		Logic 1 for fault conditons.
Drive Capability		50pF + rated logic drive Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, 0.4 mA at 2.8V min High Z;10 µA//5pF max Logic 0;100mV max driving CMOS Logic 1; +5V supply minus 100mV min driving CMOS
ANALOG OUTPUT:		
Analog Return (V)		+4.3V nom
Velocity (VEL) (see note)		See Table 4. VEL. Char.
AC error (e)		
14 BIT Mode	mV_{rms}	5.5 per LSB of error
16 BIT Mode	mV_{rms}	2.75 per LSB of error
Load	mA	1
DYNAMIC CHARACTERISTICS		See Table 6.
POWER SUPPLY CHARACTERISTICS		
Nominal Voltage	V	+5
Voltage Tolerance	%	±10
Max Voltage w/o Damage	V	+7
Current	mA	30 max
TEMPERATURE RANGES		
Operating	°C	-55 to + 125
Storage	°C	-65 to + 150
PHYSICAL CHARACTERISTICS		
Size	in (mm)	1.9 x 0.78 x 0.21" (48 x 20 x 5.3) 36 Pin Double Dip
Weight	oz(g)	0.7 max (20)

NOTE: VEL polarity is positive voltage for positive angular rate. See table 4 and figure 15.

THEORY OF OPERATION

The SDC-14531II Series are small, 36 pin DDIP synchro to digital hybrid converters. As shown in the block diagram (figure 1) the SDC-14531II can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.

Converter Operation

As shown in figure 1, the converter section of the SDC-14531II contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO),up-down counter, and reference conditioner. The converter produces a digital angle which tracks the analog input angle to within the specified accuracy of the converter.

The control transformer performs the following trigonometric computation:

$$\sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta representing the resolver shaft position.

ϕ is digital angle phi contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) = 0$, so that ϕ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to $\sin(\theta-\phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It's single ended Input Z is 250k Ohms min, 500k Ohms differential.

SPECIAL FUNCTIONS

Reference Synthesizer — Quadrature Voltages.

The synthesized reference section of the SDC-14531II eliminates errors caused by quadrature voltage. Due to the inductive nature of synchros and resovers, their signals typically lead the reference signal (RH and RL) by about 6°. When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. In a 14 bit converter it is not necessary to compensate for the reference signal's phase shift. A 6° phase shift will, however, cause problems for the one minute accuracy converters. As shown in figure 1, the converter synthesizes its own $\cos(\omega t + \alpha)$ reference signal from the $\sin\theta \cdot \cos(\omega t + \alpha)$, $\cos\theta \cdot \cos(\omega t + \alpha)$ signal inputs and from the $\cos\omega t$ reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated. **The synthesized reference circuit also eliminates the 180° false error null hangup.**

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error=(Quadrature Voltage/F.S.signal) • tan(α)

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale sinal is in volts.
α = signal to REF phase shift

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: $\alpha = 6°$

Then: Magnitude of Error = 0.35 min ≅ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the synchro or resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage=(rotational speed/carrier frequency) • F.S.signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the synchro or resolver.
Carrier frequency is the REF in Hz.

Built-In-Test (BIT, Pin 15)

The Built-In-Test output (BIT) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero, if it exceeds approximately 55 LSBs (of the selected resolution) the logic level at BIT will change from a logic 0 to logic 1. This condition will occur during a large step and reset after the converter settles out. BIT will also change to logic 1 for an over-velocity condition, because the converter loop cannot maintain input-output or and if the converter malfunctions where it cannot maintain the loop at a null. BIT will also be set for a Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR).

E

SPECIAL FUNCTIONS - continued

Programmable Resolution (14B, PIN 16)

Resolution is controlled by one logic input, 14B . The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, input 14B is latched internally on the trailing edge of CB (see figure 2).

INTERFACING - INPUT

Signal Input Options

The SDC-14531II series offers programmable synchro or resolver inputs. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta+120^\circ)\cos\omega t$, and $\sin(\theta+240^\circ)\cos\omega t$ are internally converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$.
Figure 3 illustrates synchro and resolver signals as a function of the angle θ.

The solid-state signal and reference inputs are true differential inputs with high AC and DC common mode rejection.
Input impedance is maintained with power off.

Synchro/Resolver Programmable Input option

The Synchro or Resolver Programmable input option is shown in figures 4 and 5.

Solid-State Buffer Input Protection — Transient Voltage Suppression

The solid-state signal and reference inputs are true differential inputs with high AC and DC common rejection , so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the values in Table 2.

INTERFACING - INPUT (continued)

TABLE 2.

Input	Common Mode Maximum	Max Transient Peak Voltage
11.8V L-L	30V Peak	150V
90V L-L	180V Peak	500V
Reference	250V Peak	500V

The 90V line-to-line systems may have voltage transients which exceed the 500V specification listed above. *These transients can destroy the thin film input resistor network in the hybrid.* Therefore, 90V L-L solid-state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver are witched on and off. For instance a 1000V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened. See figure 6.

INTERFACING - DIGITAL OUTPUTS & CONTROLS

Digital Interface

Te digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{\text{INH}}$) command allowing stable data to be read out of the SDC-14531II.

2. Furnishes parallel tri-state data formats.

3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-14531II applying an Inhibit ($\overline{\text{INH}}$) command will lock the data in the inhibit transparent latch without interfering with the continuous tracking of the converter's feedback loop. Therefore the digital angle ϕ is always updated, and the $\overline{\text{INH}}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry.
For further information see the INHIBIT ($\overline{\text{INH}}$, PIN 13) paragraph.

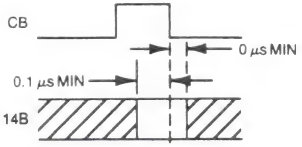
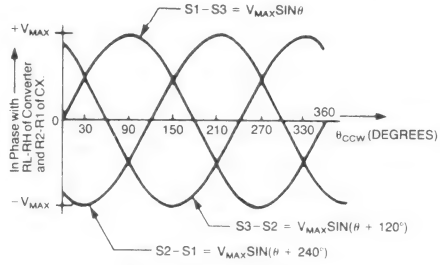
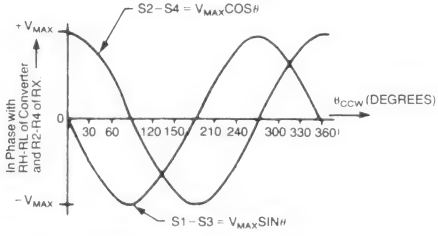


FIGURE 2. RESOLUTION CONTROL TIMING DIAGRAM



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 3. SYNCHRO AND RESOLVER SIGNALS

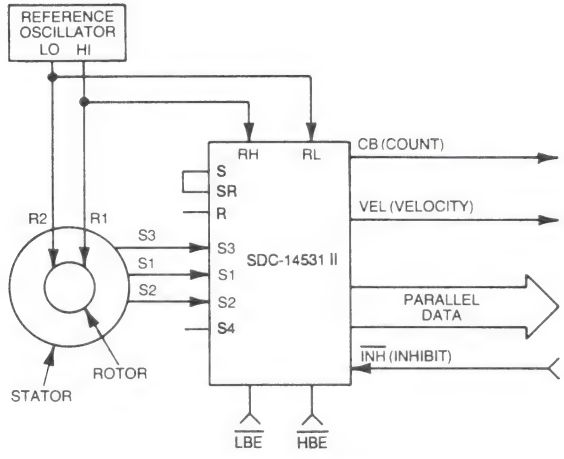


FIGURE 4. SYNCHRO INPUT CONNECTION DIAGRAM

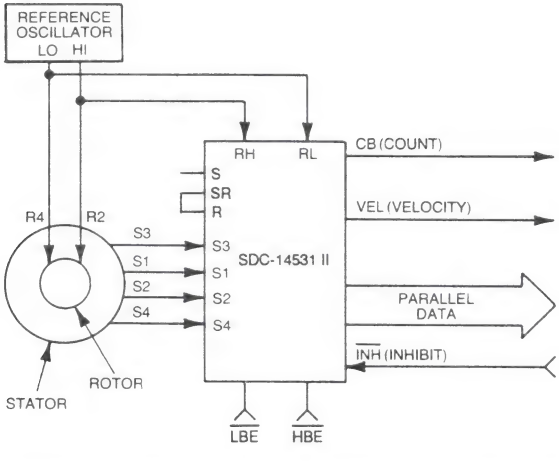


FIGURE 5. RESOLVER INPUT CONNECTION DIAGRAM

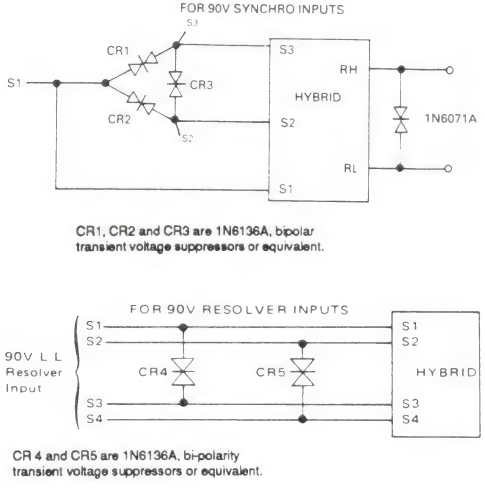


FIGURE 6. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

INTERFACING - DIGITAL OUTPUTS & CONTROLS (continued)

Digital Angle Outputs (Logic Input/Output)

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{HBE}$ (pin 35) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{LBE}$ (pin 17) to a logic 0.

The second byte will contain either bits 9-14 (14 bit resolution) or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 3 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{HBE}$ or $\overline{LBE}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{HBE}$ and $\overline{LBE}$ are set to logic 1(see figure 7). Both enables are internally pulled down.

TABLE 3. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1(MSB ALL MODES)	180	10,8000
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE	0.0055	0.33

Note: $\overline{HBE}$ enables the 8 MSBs and $\overline{LBE}$ enables the LSBs.

Digital Angle Output Timing

The digital angle output is 14 or 16 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive, 0.8 to 3.0 µs pulse.

The digital output data changes approximately 50ns after the leading edge of the CB pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB (see figure 8). The angle is determined by the sum of the bits at logic 1. The digital outputs are valid 150 ns max after $\overline{HBE}$ or $\overline{LBE}$ go low and are high impedance within 100ns max of $\overline{HBE}$ or $\overline{LBE}$ going high.

Inhibit ($\overline{INH}$, Pin 13)

When an Inhibit ($\overline{INH}$) input is applied to the SDC-14531II, the Output Transparent Latch is locked causing the output data bits to remain stable while data is being transferred (see figure 9). The output data bits are stable 0.5µs after $\overline{INH}$ goes to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic 0 and the $\overline{INH}$ latch is transparent; when CB goes to logic 1, the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is: (1) Apply $\overline{INH}$; (2) Wait 0.5 µs min; (3) Transfer the data; (4) Release $\overline{INH}$.

A logic 1 for the $\overline{INH}$ enables the output data to be updated.The time it takes for $\overline{INH}$ to go to a logic 1 should be 100ns minimum before valid data is transferred. To allow the update of the output data with valid information the $\overline{INH}$ must remain at a logic 1 for 1µs minimum (see figure 10 below).

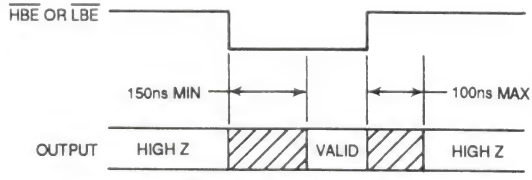


FIGURE 7. TRI-STATE OUTPUT TIMING

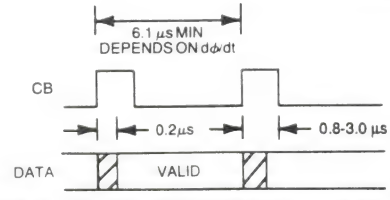


FIGURE 8. CONVERTER BUSY TIMING DIAGRAM

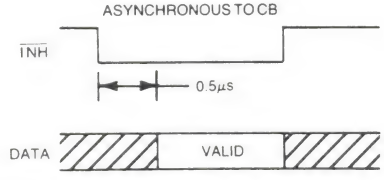


FIGURE 9. INHIBIT TIMING DIAGRAM

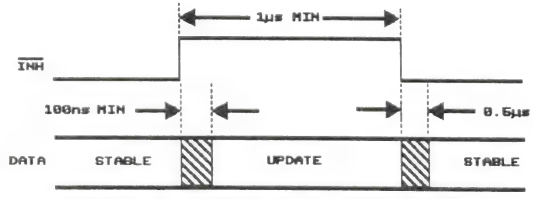


FIGURE 10. OUTPUT DATA UPDATE TIMING

INTERFACING - DIGITAL OUTPUTS & CONTROLS (continued)

Data Transfers

Digital output data from the SDC-14531II can be transferred to 8 bit and 16 bit bus systems. For 8 bit systems, the MSB and LSB bytes are transferred sequentially. For 16 bit systems all bits are transferred at the same time

Data Transfer To 8 Bit Bus

Figures 11 and 12 show the connections and timingfor transferring data from the SDC-14531II to an 8 bit bus

As can be seen by the timing diagram the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500ns before valid data is transferred.

2. $\overline{HBE}$ is set to a low state (logic 0) 350ns MIN after $\overline{INH}$ goes low and must remain low for a minimum of 150ns before the MSB data (1- 8) is valid and transferred.

3. As $\overline{HBE}$ is set to a high state (logic 1), $\overline{LBE}$ is brought low for a 150ns MIN before the LSB data is valid and transferred.

4. $\overline{LBE}$ should go high (to logic 1)at least 100ns MAX before another device uses the bus.

5. $\overline{INH}$ goes high and data transfer is done and the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100ns minimum before valid data is transferred.

Note: for further understanding refer to the beginning of this section (i.e. Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

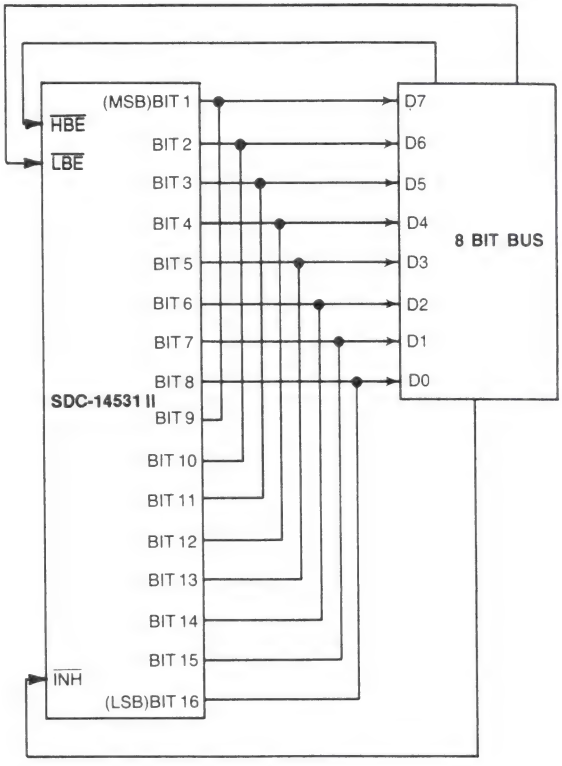


FIGURE 11 . DATA TRANSFER TO 8 BIT BUS

16 Bit Data Transfer

Data transfer to the 16 bit bus is much simpler than the 8 bit bus. Figures 13 and 14 (page 8) show the connections and timingfor transferring data from the SDC-14531II to an 8 bit bus

As can be seen by the timing diagram the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500ns before valid data is transferred.

2. $\overline{HBE}$ and $\overline{LBE}$ are set to a low state (logic 0) 350ns MIN after $\overline{INH}$ goes low and must remain low for a minimum of 150ns before the data (1- 16) is valid and transferred.

3. $\overline{HBE}$ and $\overline{LBE}$ should go high (to logic 1)at least 100ns MAX before another device uses the bus.

4. $\overline{INH}$ goes high and data transfer is done and the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100ns minimum before valid data is transferred.

Note: for further understanding refer to the beginning of this section (i.e. Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

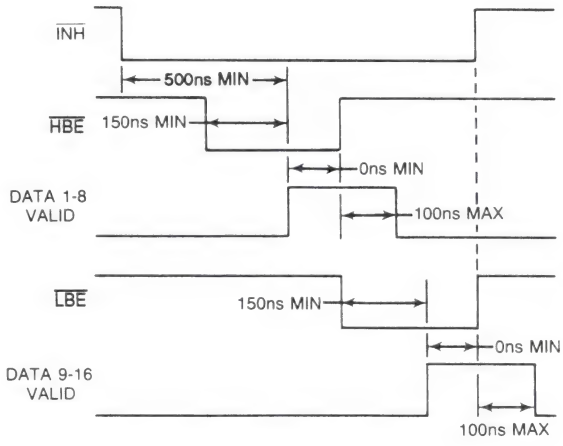


FIGURE 12. DATA TRANSFER TO 8 BIT BUS TIMING

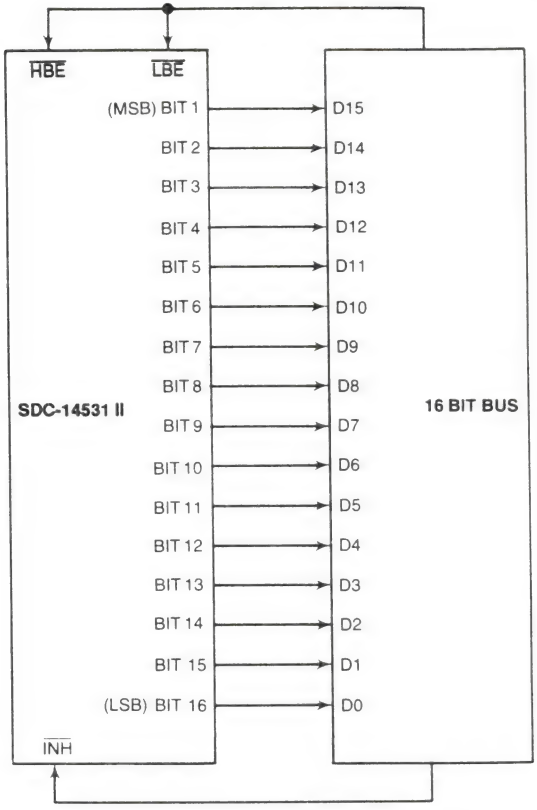


FIGURE 13. 16 BIT DATA TRANSFER

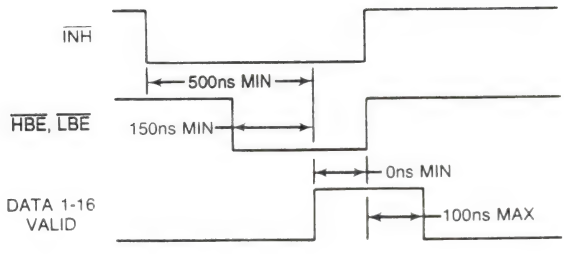


FIGURE 14. 16 BIT DATA TRANSFER TIMING

INTERFACING - ANALOG OUTPUTS

The analog outputs are AC error (e), Analog Return (V), and Velocity (VEL).

AC Error (e, PIN 12)

The AC error is proportional to the difference between the input angle θ and the digital input angle ϕ, (θ - ϕ), with a scaling of:

5.5mVrms/LSB (14 bit mode)
2.75mVrms/LSB (16 bit mode)

The e output can swing ±3V min with respect to Analog Return (V).

Analog Return (V, PIN 10).

This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference and the return for the VEL and e outputs. It is nominally +4.3V and is proportional to the +5VDC supply.

Velocity (VEL, PIN 11)

The velocity output (VEL, pin 11) is a DC voltage proportional to angular velocity dθ/dt. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The VEL output can swing ±1.10V with respect to Analog Return (V). The analog output VEL characteristics are listed in tables 4 and 5.

The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

TABLE 4. VELOCITY CHARACTERISTICS			
PARAMETER	UNITS	TYP	MAX
Polarity	See the note at the bottom of the table.		
Output Voltage	V	1.1	
Voltage scaling	RPS/1.1V	See Vel. Voltage Scaling Table 5.	
Scale Factor	%	10	15
Reversal Error	%	5	8
Linearity	% output	1	2
Zero offset	mV	5	20
Load	mA		1
Note: VEL is positive for positive angular rate and -VEL is negative for positive angular rate if measured per differential circuit (figure 15).			

TABLE 5. VELOCITY VOLTAGE SCALING (values in V/RPS)	
14 BIT	16 BIT
0.11	0.44
Note: If the resolution is changed while the input is changing, then the velocity output voltage and the digital output will have a transient until it settles to the new velocity scaling at a speed determined by the bandwidth	

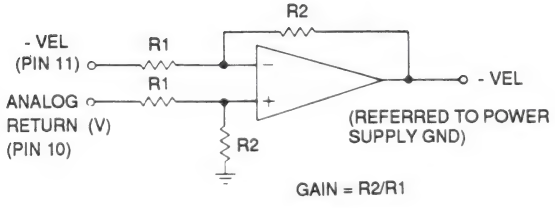


FIGURE 15. DIFFERENTIAL CIRCUIT FOR A -VEL, ANALOG OUTPUT

INTERFACING - DYNAMIC PERFORMANCE

A Type II servo loop ($K_v = \infty$) and very high acceleration constants give the SDC-14531II superior dynamic performance. If the power supply voltage is not the +5VDC nominal value, the specified input rates will increase or decrease in proportion to the fractional change in voltage.

Transfer Functions

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 16) and open and closed loop Bode plots (figures 17 and 18). Values for the transfer function block can be obtained from table 6.

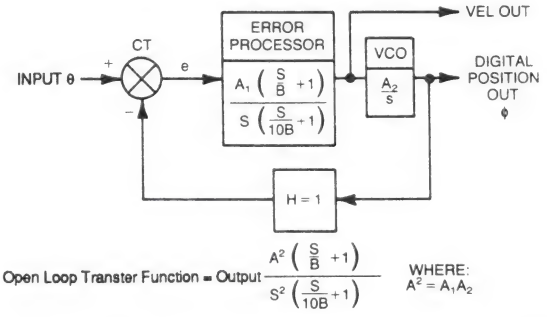


FIGURE 16. TRANSFER FUNCTION BLOCK DIAGRAM

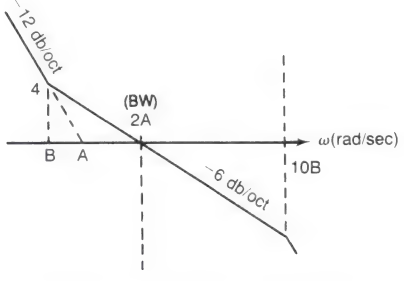


FIGURE 17. OPEN LOOP BODE PLOT

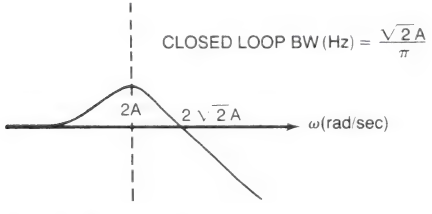


FIGURE 18. CLOSED LOOP BODE PLOT

INTERFACING - DYNAMIC PERFORMANCE (continued)

TABLE 6. DYNAMIC CHARACTERISTICS			
PARAMETER	UNIT	14 Bit Resolution	16 Bit Resolution
Input Freq.(see note)	Hertz	360 - 1000	360 - 1000
Tracking Rate	RPS	10	2.5
Bandwidth,cl	Hertz	100	100
Ka	$1/sec^2$	48,400	48,400
A1	1/sec	0.91	0.91
A2	1/sec	53,000	53,000
A	1/sec	220	220
B	1/sec	110	110
acc-1 LSB lag	Deg/sec^2	1056	264
Settling Time			
180° Step	mS	200	300
1.4° Step	mS	25	35
Note: For model -644 Input Freq. is from 360 - 2500Hz.			

Response Parameters

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 19 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

Faster Settling Time Using BIT to Reduce Resolution

Since the SDC-14531II has higher precision in the 16 Bit mode and faster settling in the 14 Bit mode, the BIT output can be used to program the SDC-14531II for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit.

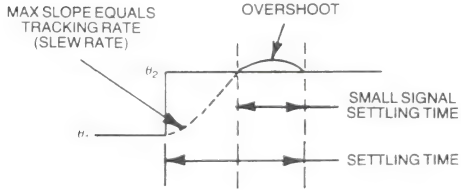


FIGURE 19. RESPONSE TO A STEP INPUT

CONNECTING THE SDC-14531II TO A PC BOARD

The SDC-14531II can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572° F) max, for 10 seconds maximum.

Since the SDC-14531II Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

TABLE 7. SDC-14531II PIN OUTS			
PIN	FUNCTION	PIN	FUNCTION
1	S1(Res) S1(Syn)	36	+5V
2	S2(Res) S2(Syn)	35	$\overline{HBE}$
3	S3(Res) S3(Syn)	34	B1(MSB)
4	S4(Res) ——	33	B2
5	S	32	B3
6	SR	31	B4
7	R	30	B5
8	RL	29	B6
9	RH	28	B7
10	Analog Return (V)	27	B8
11(see note)	VEL	26	B9
12	e	25	B10
13	$\overline{INH}$	24	B11
14	CB	23	B12
15	BIT	22	B13
16	14B	21	B14
17	$\overline{LBE}$	20	B15
18	GND	19	B16(LSB)

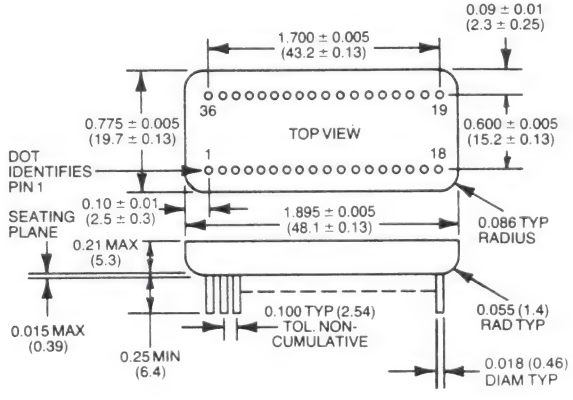
NOTE: See table 4 and figure 15.

ORDERING INFORMATION

SDC-14531II-XXX

- 680/690(note 1) = 11.8V S/R 1.3 MIN
- 681/691(note 1) = 11.8V S/R 2.6 MIN
- 682/692(note 1) = 11.8V S/R 5.2 MIN
- 683/693(note 1) = 90V S/R 1.3 MIN
- 684/694(note 1) = 90V S/R 2.6 MIN
- 685/695(note 1) = 90V S/R 5.2 MIN
- 644 = 11.8V Resolver Only, to 2.5kHz, 1.3MIN

NOTES:
(1) X8X = 883B processing is available but without QCI testing.
X9X = 883B processing is available.
(2) All models have -55°C to + 125°C operating temperature range.



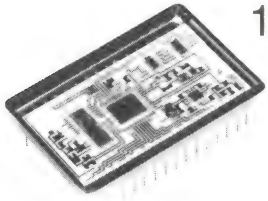
NOTES:
1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ± 0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Package is Kover with electroless nickel plating.
5. Case is electrically floating.

FIGURE 20. SDC-14531II MECHANICAL OUTLINE 36 PIN DDIP

DDC
ILC DATA DEVICE CORPORATION

SDC-14532 MONOBRID® SERIES

12 AND 14 BIT S/D AND R/D CONVERTER



DESCRIPTION

The SDC-14532 is a complete 12 or 14 bit synchro or resolver-to-digital converter packaged in a small 32 pin TDIP hybrid. Features of this series include: ±5.3 minute accuracy, Control Transformer (CT) mode capability, an Inhibit input which, when applied, does not interfere with tracking, and low power consumption.

The SDC-14532 accepts broadband inputs (360 Hz to 2600 Hz), has solid state signal and reference isolation. The output of the SDC-14532 is a natural binary code, parallel positive logic and is CMOS and TTL compatible.

APPLICATIONS

With three-state outputs and an Inhibit that does not stop the tracking process, the SDC-14532 Series is especially well suited for bus multiplexing and microprocessor interfacing. These converters are ideal for remotely located and hard to access equipment where low power consumption, small size, and high MTBF are critical.

FEATURES

- *2ND SOURCE FOR SDC-1740/1/2 SERIES*
- *SOLID STATE INPUTS*
- *MIL-STD-883 SCREENING AVAILABLE*
- *CT MODE CAPABILITY*
- *INHIBIT DOES NOT INTERRUPT TRACKING*
- *ACCURACY TO ±5.3 MIN*
- *THREE-STATE LATCHED OUTPUTS*
- *TTL AND CMOS COMPATIBLE*

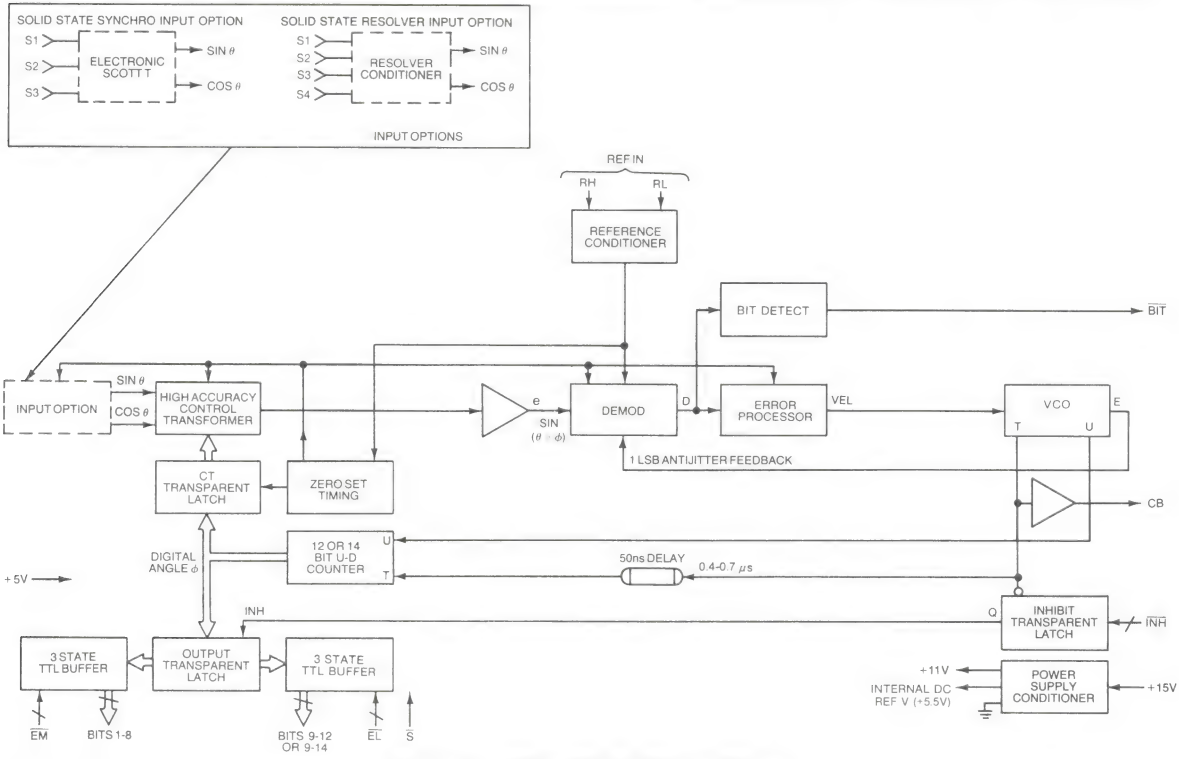


FIGURE 1. SDC-14532 BLOCK DIAGRAM

®Monobrid is a registered trademark of ILC Data Device Corporation.

TABLE 1. SDC-14532 SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency, and amplitude ranges: 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	
RESOLUTION	12 or 14 bits	
ACCURACY	±8.5 min (12 bit) ±5.3 min (14 bit)	
REFERENCE INPUT CHARACTERISTICS		
Carrier Frequency Range	360 to 1200 Hz	
Voltage Range	4 to 130V rms	
Input Impedance		
Single Ended	250K Ohm min	
Differential	500K Ohm min	
Common Mode Range	210V peak max, 500V transient peak	
SIGNAL INPUT CHARACTERISTICS (Voltage options and minimum input impedance balanced)		
Synchro	11.8V L-L	90V L-L
Z_{in} Line-to-Line	17.5K Ohm	130K Ohm
Z_{in} Each Line to Ground	11.5K Ohm	85K Ohm
Resolver	11.8V L-L	26V L-L
Z_{in} Single Ended	23K Ohm	50K Ohm
Z_{in} Differential	46K Ohm	100K Ohm
Z_{in} Each Line to Ground	23K Ohm	50K Ohm
Common Mode Range	60V max	60V max
DIGITAL INPUT/OUTPUT		
Logic Type	TTL/CMOS compatible	
Inputs	Logic 1 = 0.8V max Logic 0 = 2.0V min Loading = 10μA max pull-up current source to +5V/5pF max, CMOS transient protected.	
Inhibit ($\overline{INH}$)	Logic 0 inhibits, data stable after 0.5μs.	
Enable bits 1 to 8 ($\overline{EM}$)	Logic 0 enables, logic 1 high Z.	
Enable bits 9 to 12 ($\overline{EL}$) or bits 9 to 14	Logic 0 enables, logic 1 high Z.	
Output Parallel Data	12 or 14 parallel lines, natural binary angle, positive logic.	
Converter Busy (CB)	0.4 to 0.7μs positive pulse; leading edge initiates counter update.	
Drive Capability	50pF plus rated logic drive. Logic 0: 1 TTL load, 1.6mA at 0.4V max. Logic 1: 10 TTL loads, 0.4mA at 2.8V min. High Z: 10μA/5pF max. Logic 1: +5V supply minus 100mV min driving CMOS.	
Built-In Test ($\overline{BIT}$)	Logic 0 for $\overline{BIT}$ condition.	
DYNAMIC CHARACTERISTICS	See table 3.	
POWER SUPPLY CHARACTERISTICS		
Nominal Voltage	+15V	+5V
Voltage Range	±5%	±10%
Max Voltage w/o Damage	+18V	+8V
Current	20mA max	3mA max
TEMPERATURE RANGES		
Operating		
-3XX	0°C to + 70°C	
-1XX	−55°C to +125°C	
Storage	−65°C to +150°C	

TABLE 1. SDC-14532 SPECIFICATIONS (Continued)

PARAMETER	VALUE
PHYSICAL CHARACTERISTICS	
Size	1.74 x 1.14 x 0.28 in. (44 x 29 x 7.1 mm)
Weight	0.8 max (23 gm)

TECHNICAL INFORMATION

The information in this section describes the structure and operation of the SDC-14532 Series.

E

INTRODUCTION

The circuit shown in the block diagram of figure 1 contains three main parts: the Signal Input; a Feedback Loop, whose elements are the control transformer, demodulator, error processor, VCO and up-down counter; and Digital Interface circuitry including various latches and buffers.

SIGNAL INPUTS

The SDC-14532 offers two input options: synchro or resolver. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta + 120°)\cos\omega t$, and $\sin(\theta + 240°)\cos\omega t$ are internally converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$ (see figure 2).

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection. Input impedance is maintained with power off.

FEEDBACK LOOP

The Feedback Loop produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

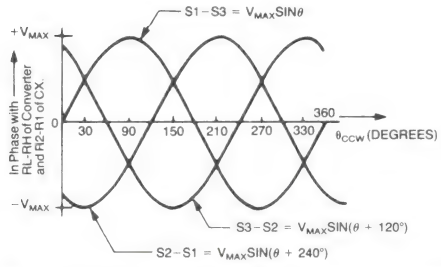
where:

θ is the angle theta, representing the resolver shaft position.
ϕ is the digital angle phi contained in the up/down counter.

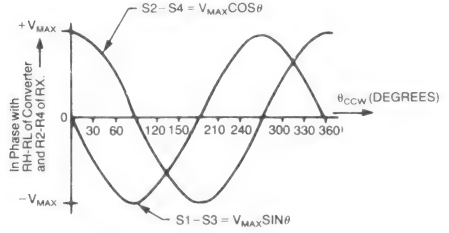
The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \blacktriangleright 0$, so that ϕ will represent the shaft position θ. The output of the demodulator is an analog DC level proportional to $\sin(\theta - \phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives a Voltage Controlled Oscillator (VCO). The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which

make the converter a Type II tracking servo. In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without a lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The converter automatically zero-sets all of the internal op-amps twice per carrier cycle near the zero crossings of the reference. This contributes to the converter's superior dynamic performance.



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. SYNCHRO AND RESOLVER SIGNALS

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the SDC-14532.
2. Furnishes parallel and tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-14532, applying an inhibit command will lock the data in the transparent latch without interfering with the continuous tracking of the feedback loop. Therefore, the digital angle is always updated, and the inhibit can be applied for an arbitrary amount of time. The inhibit transparent latch and the 50ns delay are part of the inhibit circuitry. The inhibit circuitry is described in detail in the logic input/output section.

LOGIC INPUT/OUTPUT

Logic angle outputs consist of 12 or 14 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5 volts. The CB output is a positive, 0.4 to 0.7μs pulse. Data changes about 50ns after the leading edge of the pulse because of an internal delay. Data is valid 0.2μs after the leading edge of CB, the angle is determined by the sum of the bits at logic 1. Digital outputs are three-state and two bytes wide; bits 1-8 (MSBs) are enabled by the signal $\overline{EM}$, bits 9-14 (LSBs) are enabled by the signal $\overline{EL}$. Outputs are valid (logic 1 or 0) 150ns max after setting $\overline{EM}$ or $\overline{EL}$ low and are high impedance within 100 ns max of setting $\overline{EM}$ or $\overline{EL}$ high. Both $\overline{EM}$ and $\overline{EL}$ are internally pulled-up to +5V at 10μA max.

The inhibit ($\overline{INH}$) input locks the transparent latch so the bits will remain stable while data is being transferred (see figure 1). The output is stable 0.5μs after $\overline{INH}$ is driven to logic 0, see figure 3. A logic 0 at the T input latches the data, and a logic 1 applied to T will allow the bits to change. The inhibit transparent latch prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic 0 and the $\overline{INH}$ latch is transparent.

When CB goes to logic 1, the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. Output data change is initiated by the leading edge of the CB pulse, delayed by 50ns, nominal. Valid data is available at the outputs 0.2μs after the leading edge of CB, see figure 4.

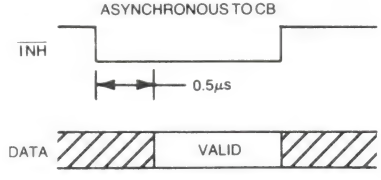


FIGURE 3. INHIBIT TIMING DIAGRAM

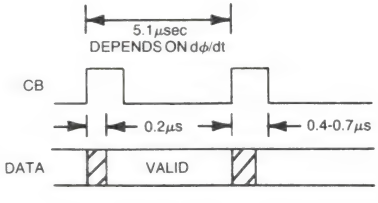


FIGURE 4. CONVERTER BUSY TIMING DIAGRAM

TABLE 2. DIGITAL ANGLE OUTPUTS		
BIT	DEG/BIT	MIN/BIT
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.879	5.27
13	0.439	2.64
14	0.0220	1.32

Note: $\overline{EM}$ enables the MSBs and $\overline{EL}$ enables the LSBs.

Digital angle outputs are buffered and are provided in a two byte format. The first byte always contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 25) to logic 0. Depending on the user programmed resolution, the second byte will have bits 9 through 12 or 9 through 14, while operating at 12 or 14 bit resolution, respectively. Placing $\overline{EL}$ (pin 26) to logic 0 enables the second byte, the LSBs. A logic 0 will be present on all the unused least significant bits. Table 2 lists the deg/bit for the digital angle outputs.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{INH}$.
(2) Wait 0.5μs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 5 shows the response to a step input.

After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

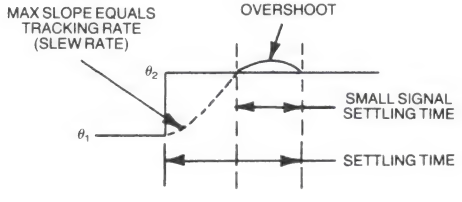


FIGURE 5. RESPONSE TO A STEP INPUT

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-14532 superior dynamic performance, as listed in table 3. If the power supply voltages are not the +15V DC nominal values, the specified input rates will increase or decrease in proportion to the fractional change in voltage. A Control Loop Block Diagram is shown in figure 6, and an Open Loop Bode Plot is shown in figure 7. The values of the transfer function coefficients are shown in table 3.

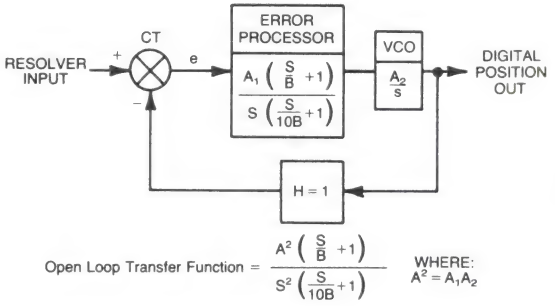


FIGURE 6. CONTROL LOOP BLOCK DIAGRAM

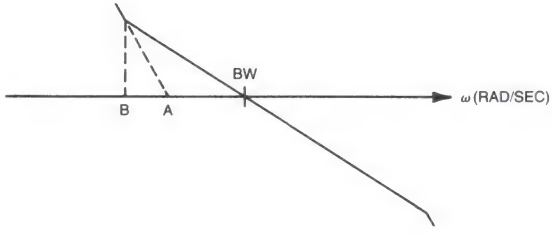
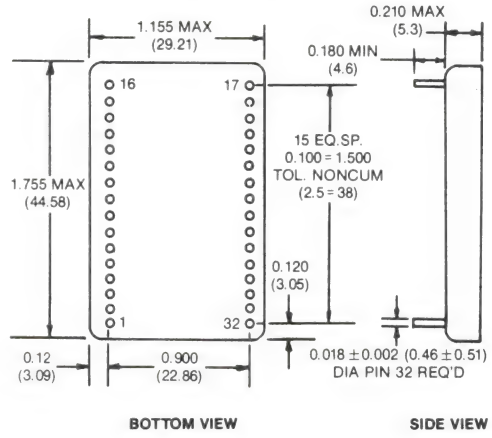


FIGURE 7. OPEN LOOP BODE PLOT

TABLE 3. DYNAMIC CHARACTERISTICS			
PARAMETER	UNITS		
RESOLUTION	Bits	12	14
Input Frequency	Hertz		360-2600
Tracking Rate	RPS min	48	12
Bandwidth	Hertz	135	135
K_a	1/sec^2 nom	90K	90K
A1	1/sec nom	2.05	2.05
A2	1/sec nom	44K	44K
A	1/sec nom	300	300
B	1/sec nom	150	150
Settling Time	ms max	90	150

TABLE 5. SDC-14532 PIN CONNECTION/FUNCTION			
PIN	FUNCTION	PIN	FUNCTION
1	1 (MSB)	17	S4
2	2	18	S3
3	3	19	S2
4	4	20	S1
5	5	21	$\overline{BIT}$
6	6	22	$\overline{S}$
7	7	23	CASE
8	8	24	NC
9	9	25	$\overline{EL}$ (LSB enable)
10	10	26	$\overline{EM}$ (MSB enable)
11	11	27	$\overline{CB}$ (Converter Busy)
12	12 (LSB 12 BIT MODE)	28	$\overline{INH}$
13	13	29	+15V
14	14 (LSB 14 BIT MODE)	30	GND
15	RL	31	NC
16	RH	32	+5V



Notes:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.

FIGURE 8. SDC-14532 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-14532-XXX

Accuracy:
- 2 = ±8.5 min (12 bit)
- 3 = ±5.3 min (14 bit)

Reliability Grade:
- 0 = Standard DDC procedures
- 1 = Fully compliant with MIL-STD-883.
- 2 = Screened to MIL-STD-883 but without QCI testing.

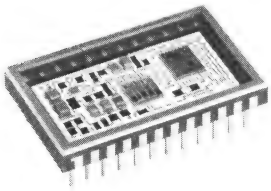
Temperature:
- 3 = 0°C to + 70°C
- 1 = −55°C to +125°C

Format:
- 2 = 11.8V L-L Synchro, 12 bits
- 3 = 90V L-L Synchro, 12 bits
- 4 = 11.8V L-L Resolver, 12 bits
- 5 = 26V L-L Resolver, 12 bits
- 6 = 11.8V L-L Synchro, 14 bits
- 7 = 90V L-L Synchro, 14 bits
- 8 = 11.8V L-L Resolver, 14 bits
- 9 = 26V L-L Resolver, 14 bits

D

SDC-14545

13 BIT, S/D CONVERTER ENHANCED LOSS-OF-SIGNAL



Call Factory For Specifications.

DESCRIPTION

The SDC-14545 is a small, 13 bit tracking 11.8V Synchro-to-Digital converter. A unique feature is its built in detection of any single open line of the five synchro lines.

Based on a single monolithic chip, it is intended for those applications demanding the ultimate in reliability and "fail safe" performance.

It is supplied in a 24 pin hermatic DDIP package. Temperature range is -55°C to +125°C and is available with 883B processing.

APPLICATIONS

Because of its ultra high reliability and high MTBF, the SDC-14545 is ideally suited for critical performance in military and commercial position control systems.

FEATURES

- ***Small Size***
- ***Unique Open Line Detector***
- ***883B Processing Available***

E

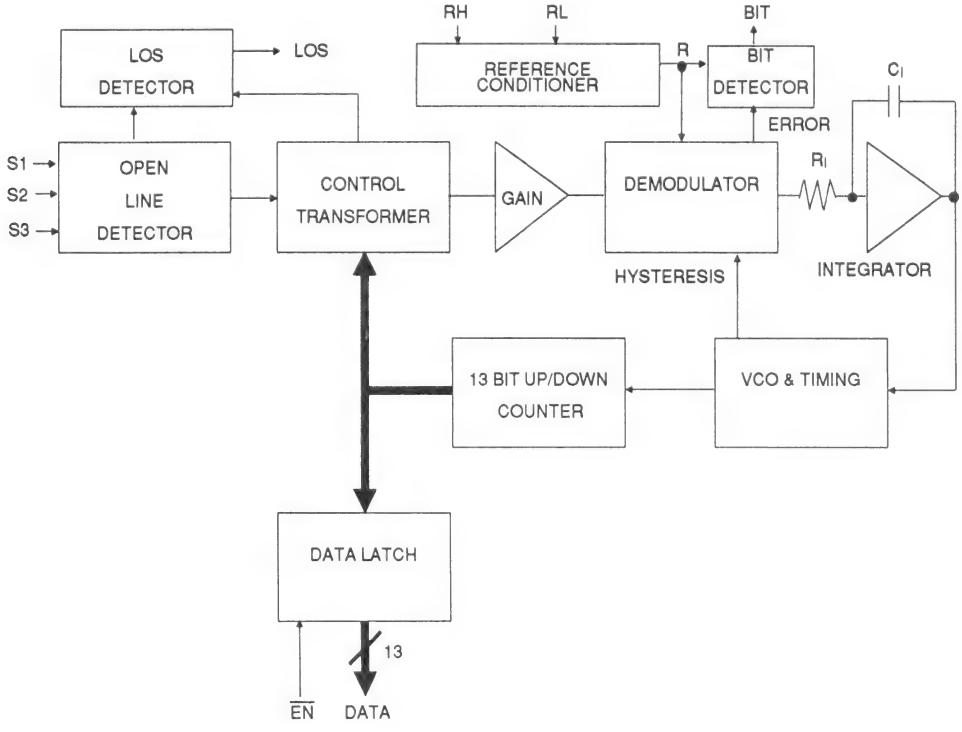
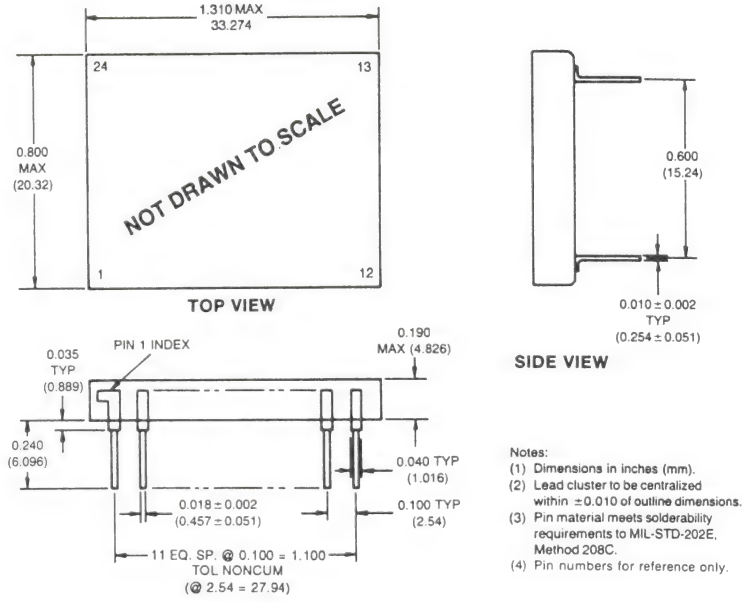


FIGURE 1. SDC-14545 BLOCK DIAGRAM

TABLE 1. SDC-14545 PIN FUNCTIONS			
PIN	FUNCTION	PIN	FUNCTION
1	RH	13	8
2	RL	14	9
3	S1	15	10
4	S2	16	11
5	S3	17	12
6	1	18	13
7	2	19	$\overline{EN}$
8	3	20	BIT
9	4	21	LOS
10	5	22	-5Vdc
11	6	23	GND
12	7	24	+5Vdc



Notes:
(1) Dimensions in inches (mm).
(2) Lead cluster to be centralized within ±0.010 of outline dimensions.
(3) Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
(4) Pin numbers for reference only.

FIGURE 2. SDC-14545 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-14545 - X X 1

Accuracy:

1 = 8 min

Reliability Grade

0 = Standard DDC processing.

1 = Fully compliant with MIL-STD-883B, including full QCI testing.

2 = Screened to MIL-STD-883B, but without QCI Testing.

Operating Temperature Range:

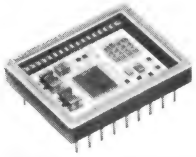
1 = -55°C to +125°C

2 = -25°C to +85°C

3 = 0 to +70°C

A

SDC-14550 SERIES



PROGRAMMABLE SYNCHRO/RESOLVER-TO-DIGITAL CONVERTERS

PRELIMINARY

DESCRIPTION

The SDC-14550 Series are small, low-cost hybrid Synchro- or Resolver-to-Digital converters based on a single-chip monolithic. The completely self-contained unit offers programmable resolution and +5Vdc operation. The package is a 34 pin ceramic package (1.0 x 0.78 x 0.21").

Resolution programming allows selection of 10, 12, 14, or 16 bit modes. This feature allows selection of either low resolution for fast tracking or higher resolution for higher accuracy.

The velocity outputs (VEL) from the SDC-14550 Series, which can be used to replace a tachometer, are ±4V signals referenced to analog ground with a linearity of 1% of output voltage.

The converter series also offers Built-In-Test ($\overline{BIT}$) outputs for each channel.

The SDC-14550 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C. 883B processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14550 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

FEATURES

- ***Single 5V power supply***
- ***10, 12, 14, or 16 bit programmable resolution***
- ***Small 34 Pin Ceramic Package***
- ***$\overline{BIT}$ Output***
- ***Velocity Output Eliminates Tachometer***
- ***High-Reliability Single-Chip Monolithic***
- ***-55°C to +125°C Operating Temperature Range***
- ***883B Processing Available***

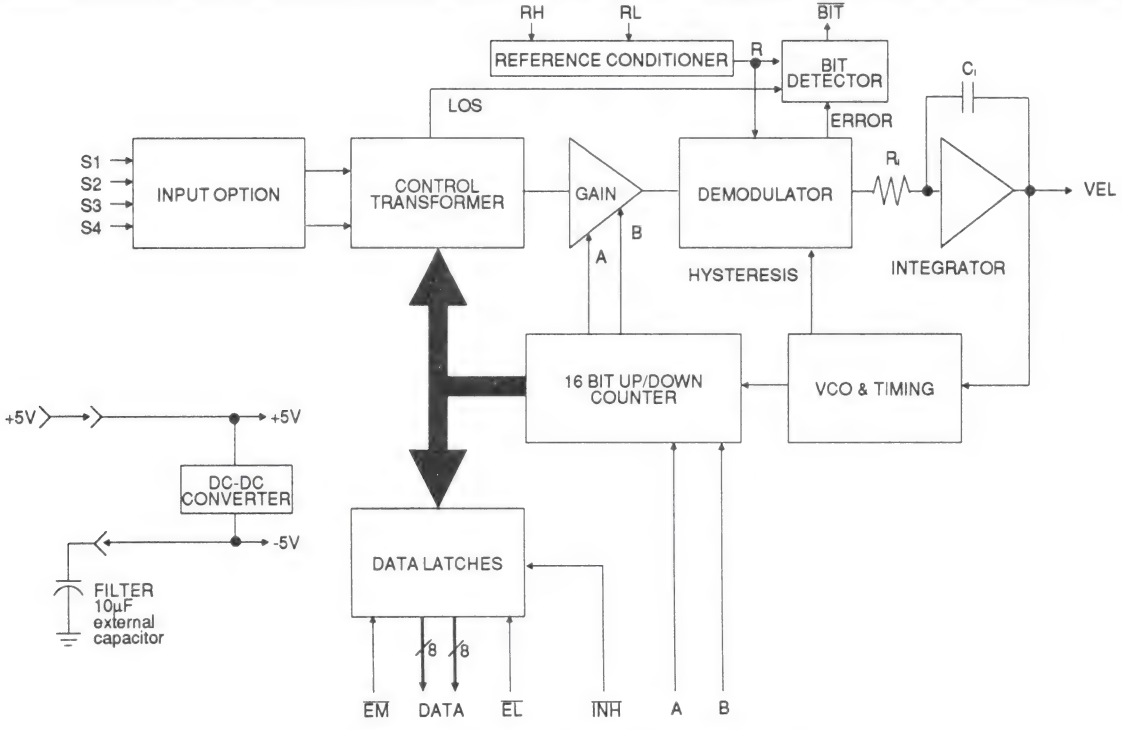


FIGURE 1. SDC-14550 BLOCK DIAGRAM

TABLE 1. SDC-14550 SPECIFICATIONS

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	programmable 10,12,14,or 16	
ACCURACY GRADES	Min	±2 or ±4, + 1LSB (see Table 4)	
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(RH,RL)	
Type		differential	
		2 & 11.8V units	**90V unit**
Voltage Range	Vrms	2 - 35	10-130
Frequency	Hz	360 - 5k	see note
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	V_{peak}	50, 100 transient	200, 300 transient
SIGNAL INPUT CHARACTERISTICS			
90V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	123k	
Z_{in} line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	52k	
Z_{in} line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Z_{in} single ended	Ohm	70k	
Z_{in} differential	Ohm	140k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M // 10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pF max. CMOS transient protected	
Resolution Control (A & B)		See Table 2.	
Inhibit ($\overline{INH}$))		Logic 0 inhibits ; Data stable within 0.5µs	
Enable Bits 1 to 8 ($\overline{EM}$) Enable Bits 9 to 16 ($\overline{EL}$)		Logic 0 enables; Data stable within 150 ns Logic 1 = High Impedance Data High Z within 100 ns	
Outputs			
Parallel Data	bits	16 parallel lines; 2 bytes natural binary angle, positive logic	

TABLE 1. SDC-14550 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT		
Outputs (continued)		
Built -In-Test		Logic 0 = BIT condition. ± 100LSBs of error with a filter of 500µs. LOS or LOR
Drive Capability	TTL	50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, -0.4 mA at 2.8V min
	CMOS	Logic 0; 100mV max Logic 1; +5V supply minus 100mV min
VELOCITY CHARACTERISTICS		
Polarity		Positive for increasing angle
Voltage Range(Full Scale)	±V	4.5 typ 4 min
Scale Factor	±%	10 typ 20 max
Scale Factor TC	ppm/°C	100 typ 200 max
Reversal Error	±%	1 typ 2 max
Linearity	±%	0.5 typ 1 max
Zero Offset	mV	5 typ 10 max
Zero Offset TC	µV/°C	15 typ 30 max
Load	kOhm	20 max
Noise	(Vp/V)%	1 typ 2 max
POWER SUPPLIES		
Nominal Voltage	V	+5
Voltage Range	±%	5
Max Volt. w/o Damage	V	+7
Current	mA	24 typ,34 max
TEMPERATURE RANGE		
Operating		
-30X	°C	0 to +70
-10X	°C	-55 to +125
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in(max)	1.00 x 0.78 x 0.21
	(mm)	(25.4 x 19.8 x 5.3)
Weight	oz	0.44

Note: 47 - 5k for 90V, 60Hz; 360 - 5k for 90V, 400Hz

TABLE 2. RESOLUTION CONTROL (A&B)

Resolution	B	A
10 bit	0	0
12 bit	0	1
14 bit	1	0
16 bit	1	1

THEORY OF OPERATION

The SDC-14550 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology, which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

CONVERTER OPERATION

Figure 1 is the Functional Block Diagram of SDC-14550 Series. The converter operates with a single +5Vdc power supply and internally generates a minus voltage of approximately 5 volts. This minus voltage comes out on pin 5(filter point) — see GENERAL SETUP CONSIDERATIONS. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver, and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic, and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage, which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output), which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the SDC-14550 Series converters:

1) The power supply is +5Vdc.

2) Direct inputs are referenced to A GND.

3) Connect (close to the hybrid) pin 31(Analog Ground) to pin 7 (GND).

4) In 16-bit mode, a 10µF/10Vdc tantalum filter capacitor must be added externally from pin 5(filter point) to pin 7 (ground).

E

SPECIAL FUNCTIONS

PROGRAMMABLE RESOLUTION

Resolution is controlled by Pins 27 and 28. The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist, between counting and changing the resolution, the resolution control is latched internally. Refer to Table 2 for resolution control.

$\overline{\text{BIT}}$, BUILT-IN-TEST

This output is a logic line that will flag an internal fault condition, LOS (Loss-Of-Signal), or LOR (Loss-Of-Reference). The internal fault detector monitors the internal loop error and, when it exceeds ± 100LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500µs filter.) $\overline{\text{BIT}}$ will set for an overvelocity condition because the converter loop can't maintain input/output sync. $\overline{\text{BIT}}$ will also be set if either a LOS or LOR input occurs.

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB"(or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

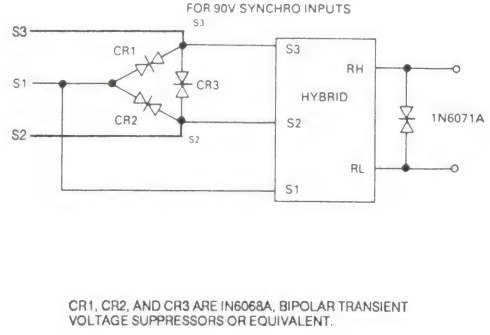
The condition is artificial, as a "real" synchro or resolver can't change its output 180° instantaneously. The condition is most often noticed during wrap-around verification tests, simulations, or troubleshooting.

INTERFACING

SOLID-STATE BUFFER INPUT PROTECTION — TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high ac and dc common rejection , so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent ac peak + dc common mode voltage should not exceed the values in Table 1.

The 90V line-to-line systems may have voltage transients which exceed the 300V specification listed in Table 1. **These transients can destroy the thin-film input resistor network in the hybrid.** Therefore, 90V L-L solid-state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever a synchro is switched on and off. For instance a 1000V transient can be generated when the primary of a CX or TX input is opened. See figure 2.



CR1, CR2, AND CR3 ARE IN6068A, BIPOLAR TRANSIENT VOLTAGE SUPPRESSORS OR EQUIVALENT.

FIGURE 2. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

INHIBIT and ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. The Enable MSB ($\overline{EM}$) is used for the most significant 8 bits and Enable LSB ($\overline{EL}$) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

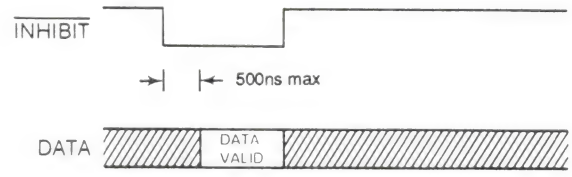


FIGURE 3. INHIBIT TIMING

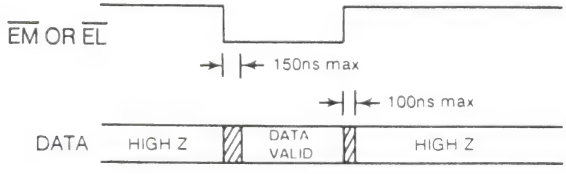


FIGURE 4. ENABLE TIMING

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-14550 superior dynamic performance.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram (figure 1), its transfer function block diagram (figure 5), and its Bode Plots (open and closed loop – figure 6). Values for the transfer function block can be obtained from Table 3.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient

and B is the frequency of lead compensation

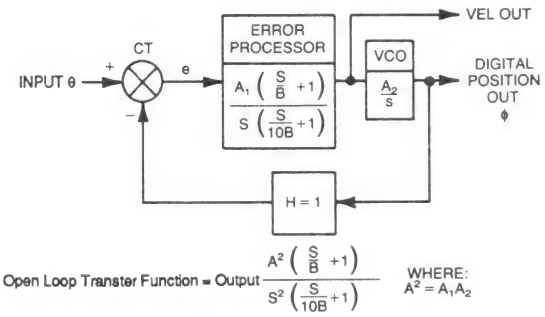


FIGURE 5. TRANSFER FUNCTION BLOCK DIAGRAM

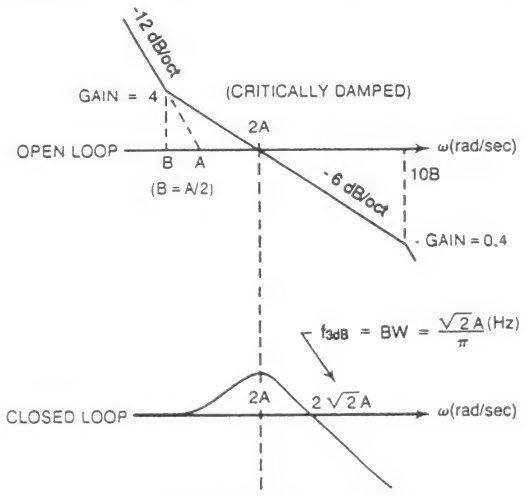


FIGURE 6. BODE PLOTS

E

ACCURACY AND RESOLUTION

Table 4 lists the total accuracy including quantinization for the various resolution and accuracy grades.

TABLE 4. ACCURACY/RESOLUTION

ACCURACY	RESOLUTION (minutes)			
(minutes)	10 BIT	12 BIT	14 BIT	16 BIT
±2 +1LSB	23.1	7.3	3.3	2.3
±4 +1LSB	25.1	9.3	5.3	4.3

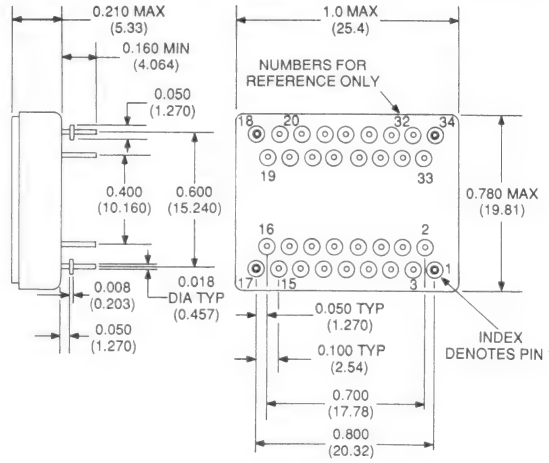
TABLE 3. DYNAMIC CHARACTERISTICS

Each Channel		DEVICE TYPE 60Hz				DEVICE TYPE 400Hz			
Input Frequency	Hz	47 - 5k				360 - 5k			
Bandwidth(Closed Loop)	Hz	15				103			
Ka	$1/s^2$	830				53k			
A1	1/s	0.17				1.33			
A2	1/s	5k				40k			
A	1/s	29				230			
B	1/s	14.5				115			
Resolution	**bits**	**10**	**12**	**14**	**16**	**10**	**12**	**14**	**16**
Tracking Rate (rps) typical	rps	32	8	2	0.5	160	40	10	2.5
minimum	rps	25.6	6.4	1.6	0.4	128	32	8	2
Accelleration (1LSB lag)	deg/s^2	720	180	45	11.3	18,600	4,640	1,160	290
Settling Time (179° step max)	msec	400	500	1,100	2,500	50	60	140	320

TABLE 4. PINOUT					
1	S1(R)	S1(S)	N.C.	34	RH (+ Reference input)
2	S2(R)	S2(S)	COS(D)	33	RL (-Reference Input)
3	S3(R)	S3(S)	SIN(D)	32	N.C.
4	S4(R)	N.C.	N.C.	31	A GND (Analog Ground)
5	Filter Point			30	VEL (Velocity Output)
6	+5V (Power Supply)			29	$\overline{INH}$ (Inhibit)
7	GND (ground)			28	B (Resolution Control B)
8	$\overline{EM}$ (Enable MSBs)			27	A (Resolution Control A)
9	$\overline{BIT}$ (Built-In-Test)			26	$\overline{EL}$ (Enable LSBs)
10	Bit 1 (MSB)			25	Bit 16 (LSB, 16-bit mode)
11	Bit 9			24	Bit 8
12	Bit 2			23	Bit 15
13	Bit 10 (LSB, 10-bit mode)			22	Bit 7
14	Bit 3			21	Bit 14 (LSB, 14-bit mode)
15	Bit 11			20	Bit 6
16	Bit 4			19	Bit 13
17	Bit 12 (LSB, 12-bit mode)			18	Bit 5

Notes:

1. (S) = Synchro; (R) = Resolver; (D) = 2V Resolver Direct
2. Connect (close to the hybrid) pin 31 to pin 7.
3. In 16-bit mode connect a 10µF/10Vdc tantalum filter cap from pin 5 to pin 7.



NOTES:

1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ± 0.005 (0.127) of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is hermetically sealed ceramic package.

FIGURE 7. SDC-14550 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC- 1455X - X X X

Accuracy:
2 = 4 min + 1 LSB
4 = 2 min + 1 LSB

Reliability:
0 = Standard DDC procedures
1 = 883B Processing Available*
2 = 168 hour burn-in at 125°C*

Operating Temperature Range:
1 = -55 to +125°C
3 = 0 to +70°C (standard reliability only)

Input Option:
0 = 11.8V, Synchro, 400Hz
1 = 11.8V, Resolver, 400Hz
2 = 90V, Synchro, 400Hz
3 = 2V, Direct, 400Hz
4 = 90V, Synchro, 60Hz

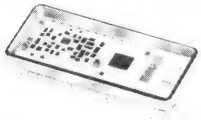
*** -55°C to +125°C temperature range only**

A

DDC
ILC DATA DEVICE CORPORATION

SDC-14560

SYNCHRO TO DIGITAL CONVERTER



DESCRIPTION

The SDC-14560 is a series of high reliability synchro or resolver to digital converters with user programmable resolution of 10, 12, 14, or 16 bits. Other features of the SDC-14560 are high quality velocity output and hermetic seal.

User programmable resolution has been designed into the SDC-14560 to increase the capabilities of modern motion control systems. The precise positioning attained at 16 bits resolution and fast tracking of a 10 bit device are now available from one 36 pin double DIP hybrid. Velocity output (VEL) from the SDC-14560 is a ground based voltage of 0 to ± 10VDC with a linearity to 0.7%. Output voltage is positive for an increasing angle.

The SDC-14560 series accepts broadband inputs: 360Hz to 1kHz, or 47Hz to 1kHz. The digital angle output from the SDC-14560 is a natural binary code, parallel positive logic and is TTL/CMOS compatible. Synchronization to a computer is accomplished via a converter busy (CB) and an inhibit ($\overline{INH}$) input.

APPLICATIONS

Because of its high reliability, accuracy, small size, and low power consumption, the SDC-14560 is ideal for the most stringent and severe industrial and military ground or avionics applications. All models are available with MIL-STD-883 processing as a standard option.

Designed with three state output, the SDC-14560 is especially well suited for use with computer based systems. Among the many possible applications are radar and navigation systems, fire control systems, flight instrumentation, and flight trainers or simulators.

FEATURES

- *PROGRAMMABLE RESOLUTION: 10, 12, 14 OR 16 BITS*
- *HIGH QUALITY VELOCITY OUTPUT*
- *ELIMINATES TACHOMETER*
- *ACCURACY TO ±1.3 ARC MINUTES*
- *SMALL SIZE*
- *SYNCHRO OR RESOLVER INPUT*
- *SYNTHESIZED REFERENCE ELIMINATES 180° LOCK-UP*

E

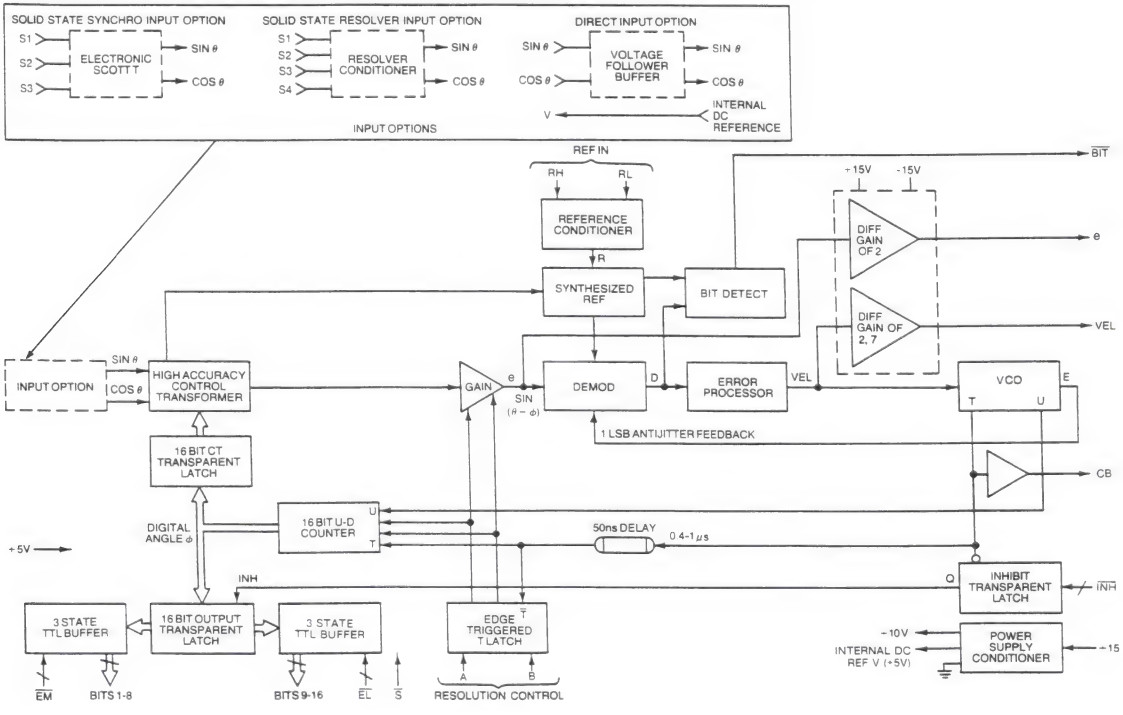


FIGURE 1. SDC-14560 BLOCK DIAGRAM

TABLE 1. SDC-14560 SPECIFICATIONS
Apply over temperature range, power supply range, reference frequency, and amplitude ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	UNIT	VALUE
RESOLUTION(1)	Bits	10, 12, 14, or 16
ACCURACY(2)	Min	±6, ±4, ±2, or ±1 +1 LSB
REPEATABILITY	LSB	1 max
DIFFERENTIAL LINEARITY	LSB	1 max in the 16th bit
REFERENCE INPUT CHARACTERISTICS		
Carrier Frequency Ranges		
Nominal 400 Hz Units	Hz	360-1000
Nominal 60 Hz Units	Hz	47-1000
Voltage Range	Vrms	4-130
Input Impedance		
Single Ended	Ohm	250K min
Differential	Ohm	500K min
Common Mode Range	V	210 peak max 500 transient peak
SIGNAL INPUT CHARACTERISTICS		
(voltage options and minimum input impedance balanced)		
Synchro	V	11.8VL-L 90VL-L
Zin Line to Line	Ohm	17.5K 130K
Zin Each Line to Gnd	Ohm	11.5K 85K
Resolver	V	11.8VL-L 26VL-L
Zin Single Ended	Ohm	23K 50K
Zin Differential	Ohm	46K 100K
Zin Each Line to Gnd	Ohm	23K 50K
Common Mode Range	V	60 max 60 max
Direct (1.0VL-L)		
Input Signal Type		Sin and Cos resolver signals referenced to converter internal DC reference V.
Sin/Cos Voltage Range	Vrms	1V nominal, 1.15V max
Max Voltage w/o Damage		15V continuous
	60	100V Peak Transient
Input Impedance		Zin >20M//10pf voltage follower
REFERENCE SYNTHESIZER		
±Sig/Ref Phase Shift	Deg	60 typ, 45 min
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs		Logic 0 = 0.8V max Logic 1 = 2.0V min Loading = 10μA max P.U. current source to +5V//5pf max CMOS transient protected
Inhibit ($\overline{INH}$)		Logic 0 inhibits Data stable after 0.5μs
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables, Logic 1 High Z
Enable Bits 9 to 16 ($\overline{EL}$).		Logic 0 enables, Logic 1 High Z
$\overline{S}$ (Control Transformer)		Logic 0 for use as CT
Resolution Control (A & B)		B A Resolution 0 0 10 bits 0 1 12 bits 1 0 14 bits 1 1 16 bits
(Unused Output Data Bits Are Set to 0)		

TABLE 1. SDC-14560 SPECIFICATIONS (Contd)

PARAMETER	UNIT	VALUE
Output Parallel Data	bits	10, 12, 14, or 16 parallel lines; natural binary angle, positive logic
Converter Busy (CB)		0.4 to 1 μS positive pulse; leading edge initiates counter update.
$\overline{BIT}$		Logic 0 for fault.
Drive Capability		50 pF plus rated logic drive. Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, 0.4mA at 2.8V min High Z; 10μA/5pF max Logic 0; 100mV max driving CMOS Logic 1; +5V supply minus 100mV min driving CMOS
ANALOG OUTPUTS		
Velocity (VEL)		See tables 3 and 4
AC error (e)	mV rms	50 per LSB of error (10 bit mode) 25 per LSB of error (12 bit mode) 12.5 per LSB of error (14 bit mode) 6.3 per LSB of error (16 bit mode)
Load	KOhm	3 min
DYNAMIC CHARACTERISTICS		See table 3.
POWER SUPPLY CHARACTERISTICS		+15V +5V −15V
Nominal Voltage		+15V +5V −15V
Voltage Range	±%	5 10 5
Max Voltage w/o Damage	V	+18 +8 −18
Current	mA max	25 10 15
TEMPERATURE RANGES		
Operating		
−30X	°C	0 to + 70
−10X	°C	−55 to +125
Storage	°C	−65 to +150
PHYSICAL CHARACTERISTICS		
Size	in. (mm)	1.9 x 0.78 x 0.21 (48.3 x 19.8 x 5.3) 36 Pin Double Dip
Weight	oz	0.7 max (20g)

Note:
(1) Pin programmable.
(2) See table 7.

TECHNICAL INFORMATION

The information in this section describes the structure of the SDC-14560 and its operation.

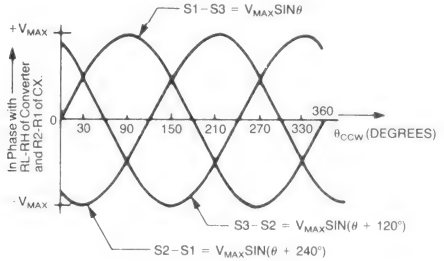
INTRODUCTION

The circuit shown in Figure 1, the SDC-14560 Block Diagram, consists of three main parts: the signal input; a feedback loop, whose elements are the control transformer, demodulator, error processor, VCO and up-down counter; and digital interface circuitry including various latches and buffers.

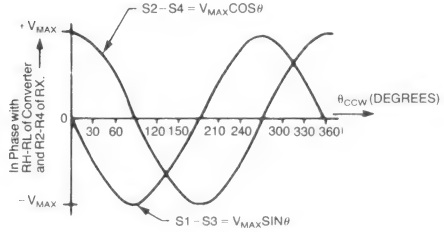
SIGNAL INPUTS

The SDC-14560 series offers three input options: synchro, resolver, and direct. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta + 120°)\cos\omega t$, and $\sin(\theta + 240°)\cos\omega t$ are internally converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Direct inputs accept 1 Vrms inputs in resolver form, ($\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$) and are buffered prior to conversion. Figure 2 illustrates synchro and resolver signals as a function of the angle θ.

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection. *Input impedance is maintained with power off.*



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. SYNCHRO AND RESOLVER SIGNALS

FEEDBACK LOOP

The feedback loop produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

where θ is the angle representing the resolver shaft position, and ϕ is the digital angle contained in the up/down counter. The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \longrightarrow 0$, so that ϕ will represent the shaft position θ. The output of the demodulator is an analog DC level proportional to $\sin(\theta - \phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives a Voltage Controlled Oscillator (VCO). The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a Type II tracking servo. In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without a lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The converter automatically zero-sets all of the internal op amps twice per carrier cycle near the zero crossings of the reference. This contributes to the converter's superior dynamic performance.

SYNTHESIZED REFERENCE

The synthesized reference section of the SDC-14560 eliminates errors caused by quadrature voltage. Due to the inductive nature of synchros and resolvers, their signals lead the reference signal (RH and RL) by about 6°. When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. In a 12 or 14 bit converter it is not necessary to compensate for the reference signal's phase shift. A 6° phase shift will, however, cause problems for the one minute accuracy converters. As shown in figure 1, the converter synthesizes its own $\cos(\omega t + \alpha)$ reference signal from the $\sin\theta\cos(\omega t + \alpha)$, $\cos\theta\cos(\omega t + \alpha)$ signal inputs and from the $\cos\omega t$ reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and −180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated. The synthesized reference circuit also eliminates the 180° false error null hangup.

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

$$\text{Error} = \text{Quad/F.S signal} * \tan(\alpha)$$

Where:
Error is in radians
Quad/F.S. signal is per unit quadrature input level.
α = signal to reference phase shift in degrees.

A typical example of the magnitude of this source of error is as follows:

Quad/F.S. signal = .001
α = 6
Error = .35 min ≃1 LSB in the 16th bit.

Note: Quad/F.S is composed of static quadrature which is specified by the resolver or synchro supplier plus the speed voltage which is given by:

Speed Voltage = rotational speed/carrier frequency

Where:
Speed Voltage is the per unit ratio of electrical rotational speed in RPS divided by carrier frequency in Hz.

This error is totally negligible for up to 14 bit converters. For 16 bit converters where the highest accuracy possible is needed and where the quadrature and phase shift specifications can be higher, this source of error could be significant. The reference

synthesizer circuit in the converter which derives the reference from the input signal essentially sets α to zero resulting in complete rejection of the quadrature.

DIGITAL INTERFACE

The digital interface circuitry has three main functions: to latch the output bits during an inhibit command so that the stable data can be read; to furnish both parallel and three-state data formats; and to act as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-14560, applying an inhibit command will lock the data in the transparent latch without interfering with the continuous tracking of the feedback loop. Therefore, the digital angle is always updated, and the inhibit can be applied for an arbitrary amount of time. The inhibit transparent latch and the 50ns delay are part of the inhibit circuitry. The inhibit circuitry is described in detail in the logic input/output section.

LOGIC INPUT/OUTPUT

Logic angle outputs consist of 10, 12, 14 or 16 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5 volts. The CB output is a positive, 0.4 to 0.7μs pulse. Data changes about 50ns after the leading edge of the pulse because of an internal delay. Data is valid 0.2μs after the leading edge of CB, the angle is determined by the sum of the bits at logic "1". Digital outputs are three-state and two bytes wide; bits 1-8 (MSBs) are enabled by the signal $\overline{EM}$, bits 9-16 (LSBs) are enabled by the signal $\overline{EL}$. Outputs are valid (logic "1" or "0") 150ns max after setting $\overline{EM}$ or $\overline{EL}$ low, and are high impedance within 100ns max of setting $\overline{EM}$ or $\overline{EL}$ high. Both $\overline{EM}$ and $\overline{EL}$ are internally pulled-up to +5V at 10μA max.

The inhibit ($\overline{INH}$) input locks the transparent latch so the bits will remain stable while data is being transferred (see figure 1). The output is stable 0.5μs after $\overline{INH}$ is driven to logic "0", see figure 3. A logic "0" at the T input latches the data, and a logic "1" applied to T will allow the bits to change. The inhibit transparent latch prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic "0" and the $\overline{INH}$ latch is transparent.

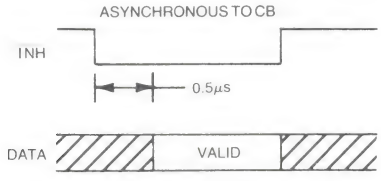


FIGURE 3. INHIBIT TIMING DIAGRAM

When CB goes to logic "1", the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic "0"; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. Output data change is initiated by the leading edge of the CB pulse, delayed by 50ns, nominal. Valid data is available at the outputs 0.2μs after the leading edge of CB, see figure 4.

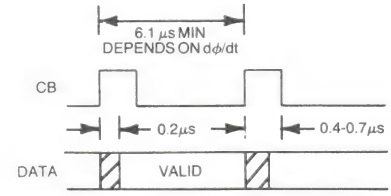


FIGURE 4. CONVERTER BUSY TIMING DIAGRAM

RESOLUTION CONTROL

Resolution control is via two logic inputs, A and B. The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that no race conditions exist between counting and changing the resolution, inputs A and B are latched internally on the trailing edge of CB, as illustrated in figure 5.

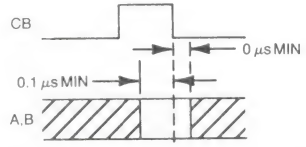


FIGURE 5. RESOLUTION CONTROL TIMING DIAGRAM

Digital angle outputs are buffered and are provided in a two byte format. The first byte always contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 26) to logic "0". Depending on the user programmed resolution, the second byte will have bits 9 and 10, 9 through 12, or 9 through 14, while operating at 10, 12, or 14 bit resolution, respectively. Placing $\overline{EL}$ (pin 25) to logic "0" enables the second byte, the LSBs. A logic "0" will be present on all the unused least significant bits. Table 2 lists the deg/bit for the digital angle outputs.

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.879	5.27
13	0.439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

Note: $\overline{EM}$ enables the MSBs and $\overline{EL}$ enables the LSBs.

BUILT IN TEST

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero, if it exceeds approximately 65 LSBs (of the selected resolution) the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 1 for an over-velocity condition, because the converter loop cannot maintain input-output or and if the converter malfunctions where it cannot maintain the loop at a null. BIT will also be set if a total Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR) occurs.

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-14560 superior dynamic performance, as listed in table 2. If the power supply voltages are not the ±15V DC nominal values, the specified input rates will increase or decrease in proportion to the fractional change in voltage. A Control Loop Block Diagram is shown in Figure 6, and an Open Loop Bode Plot is shown in Figure 7. The values of the transfer function coefficients are shown in table 3.

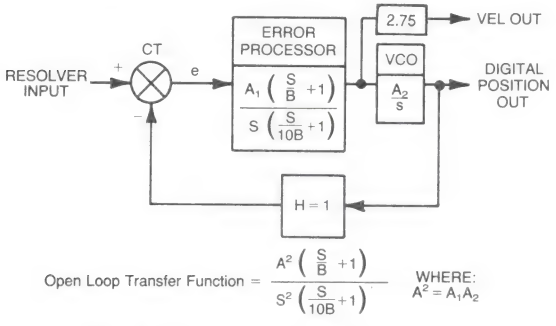


FIGURE 6. CONTROL LOOP BLOCK DIAGRAM

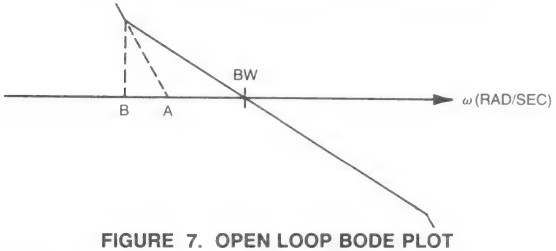


FIGURE 7. OPEN LOOP BODE PLOT

An inhibit input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronously to CB is: (A) apply the inhibit, (B) wait 0.5μs min., (C) transfer the data and (D) release the inhibit.

As long as the converter maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 8 shows the response to a step input.

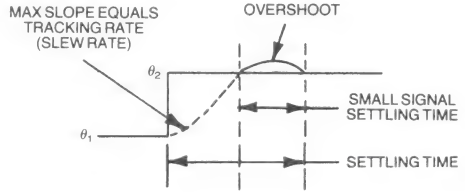


FIGURE 8. RESPONSE TO A STEP INPUT

After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to final value is a function of the small signal settling time. For Velocity output, the simple filter shown in figure 9 will eliminate the one overshoot for step velocity input and will filter the carrier frequency ripple.

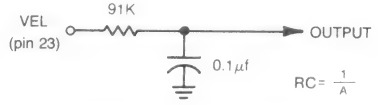


FIGURE 9. VELOCITY FILTER

ANALOG OUTPUTS

The analog outputs are velocity (VEL) and AC error (e). Both outputs can swing ±10V min. with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally if the power supply levels, are not at 15V.

TABLE 3. DYNAMIC CHARACTERISTICS

PARAMETER	UNITS	BANDWIDTH							
		400Hz				60Hz			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	Hertz		360-1000				47-1000		
Tracking Rate	RPS min	160	40	10	2.5	40	10	2.5	0.61
Bandwidth	Hertz	54	*	*	*	14	*	*	*
K_a	1/sec^2 nom	12,500	*	*	*	780	*	*	*
A1	1/sec nom	0.31	*	*	*	0.078	*	*	*
A2	1/sec nom	40K	*	*	*	10K	*	*	*
A	1/sec nom	112	*	*	*	28	*	*	*
B	1/sec nom	52	*	*	*	13	*	*	*
acc-1 LSB lag	Deg/sec^2 nom	17K	4.2K	1.1K	260	1.1K	260	66	17
Settling Time	ms max	90	90	150	350	350	360	600	1000

Note: * means same as value to the left.

The AC error, e, is proportional to the error ($\theta - \phi$) with a scaling of 50mV/LSB (10 bit mode), 25mV/LSB (12 bit mode), 12.5mV/LSB (14 bit mode), and 6.3mV/LSB (16 bit mode). Velocity output characteristics are listed in table 4.

TABLE 4. VELOCITY CHARACTERISTICS

PARAMETER	UNITS	STANDARD		HI LIN	
		TYP	MAX	TYP	MAX
Polarity		Positive for increasing angle.			
Output Voltage	V	±13	±10 min		
Voltage Scaling	RPS/10V	See Voltage Scaling Table 5.			
Scale Factor	%	5	10	5	10
Scale Factor TC	PPM/°C	100	200	100	200
Reversal Error	%	1	2	0.5	0.7
Reversal Error TC	PPM/°C	25	50	25	50
Linearity	% output	1	2	0.5	0.7
Linearity TC	PPM/°C	25	50	25	50
Zero Offset	mv	15	40	15	40
Zero Offset TC	μV/°C	25	50	25	50
Load	K ohm	–	3 min	–	3 min

VELOCITY OUTPUT

The Velocity output (VEL) from the SDC-14560 is a DC voltage proportional to angular velocity $d\theta/dt = d\phi/dt$. The velocity input is the second integrator, as shown in figure 6. Its linearity is dependent solely on the linearity of the voltage controlled oscillator (VCO). Due to the highly linearized VEL output, the electromechanical tachometer can now be eliminated from motion control systems. Bandwidth (BW) and the acceleration constant (K_a) can be determined from the formula shown:

$$BW(Hz) = BW(rad/sec)/2\pi$$
$$K_a = A^2$$

Outputs e and VEL are not required for normal operation of the converter. V is used as an internal DC reference with the direct input option. Maximum loading on V is 40K Ohm; maximum loading for e and VEL is 3K Ohm. The velocity characteristics are shown in tables 4 and 5.

TABLE 5. VELOCITY VOLTAGE SCALING

BW	RESOLUTION (values in RPS/Volt)			
	10	12	14	16
HI	16	4	1	0.25
LO	4	1	0.25	0.063

Note: If the resolution is changed while the input is changing, then the velocity output voltage and the digital output will have a transient until it settles to the new velocity scaling at a speed determined by the bandwidth. If additional information is required, consult the factory.

Output e is not closely controlled or characterized. Consult the factory for further information.

Figures 10, 11 and 12 are the synchro, resolver, and direct input connection diagrams, respectively.

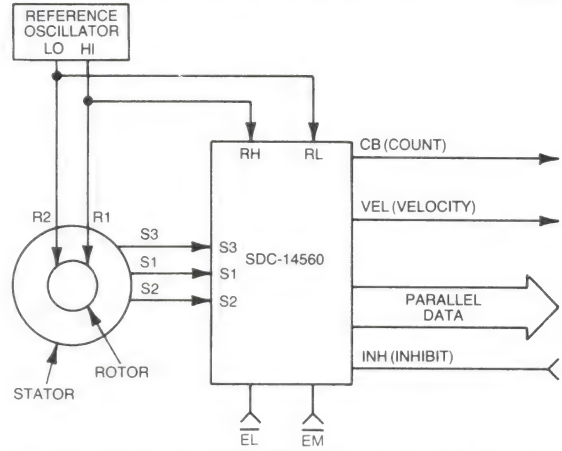


FIGURE 10. SYNCHRO INPUT CONNECTION DIAGRAM

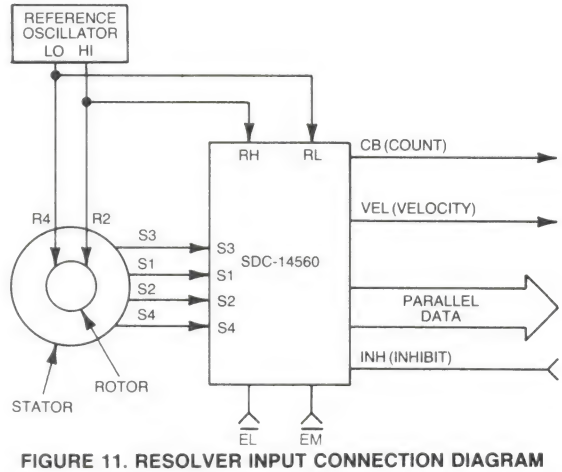


FIGURE 11. RESOLVER INPUT CONNECTION DIAGRAM

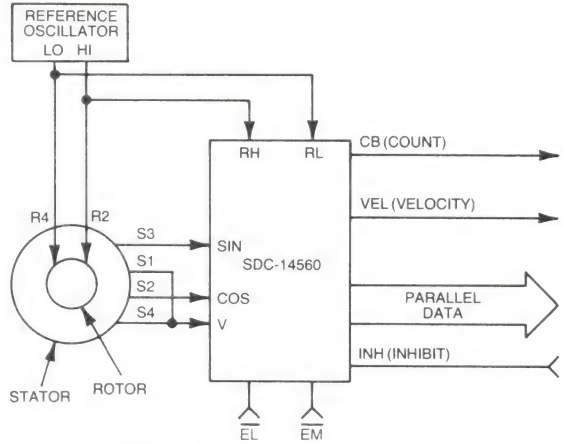


FIGURE 12. DIRECT INPUT CONNECTION DIAGRAM

TABLE 6. SDC-14560 PIN CONNECTION/FUNCTIONS					
PIN NO.	FUNCTION			PIN NO.	FUNCTION
1	S1(R)	S1(S)	V(X)	36	B
2	S2(R)	S2(S)	+C(X)	35	A
3	S3(R)	S3(S)	+S(X)	34	BIT
4	S4(R)	—	—	33	$\overline{INH}$
5	1 (MSB)			32	+15V
6	2			31	−15V
7	3			30	$\overline{S}$
8	4			29	GND
9	5			28	+5V
10	6			27	e
11	7			26	$\overline{EM}$
12	8			25	$\overline{EL}$
13	9			24	CB
14	10 (LSB-10 BIT MODE)			23	VEL
15	11			22	16 (LSB-16 BIT MODE)
16	12 (LSB-12 BIT MODE)			21	15
17	13			20	RL
18	14 (LSB-14 BIT MODE)			19	RH

Note: "(R)" means resolver, "(S)" means synchro, and "(X)" means direct.

TABLE 7. OVERALL ACCURACY (MIN.) VS. RESOLUTION				
ACCURACY GRADE (minutes)	RESOLUTION PROGRAMMED TO:			
	10 bit	12 bit	14 bit	16 bit
±1 +1LSB	22.1	6.3	2.3	1.3
±2 +1LSB	23.1	7.3	3.3	2.3
±4 +1LSB	25.1	9.3	5.3	4.3
±6 +1LSB	27.1	11.3	7.3	6.3

CT MODE

The SDC-14560 can also be used as a solid state Control Transformer. This is analogous to the function of the rotary control transformer except here the rotary shaft input is replaced by a digital angle. Referring to the equation below, the output is an AC voltage (e) which varies as the sine of the difference between the analog input angle and the digital angle.

$$e = \sin(\theta - \phi)\cos\omega t$$

Control transformers are frequently used as error signal generators in closed servo loops. They are useful when digital remote control of a position servo must be accomplished.

Figure 13 illustrates a block diagram of the Control Transformer (CT) mode. The procedure to enable this function is to disable the up-down counter by setting $\overline{S}$ (pin 30) to logic "0" and using the digital output lines (which are bidirectional) as digital inputs.

When the converter is functioning as a CT, the digital inputs are double buffered, $\overline{EM}$ is redefined as $\overline{LM}$ (LATCH MSBs), $\overline{EL}$ is redefined as $\overline{LL}$ (LATCH LSBs) and $\overline{INH}$ becomes $\overline{LA}$ (LATCH ALL.)

TRANSFORMERS

Figure 14 illustrates the Transformer Connection Diagram. These transformers are designed for the voltage follower buffer input option to the SDC-14560. However, the reference transformers may also be used with the solid state buffer input options.

Passive transformers are considerably larger in size for 60Hz than for 400Hz. To minimize size, active transformers are utilized over passive devices for 60Hz. These active 60Hz transformers have op-amp outputs and require connection to a +15V power supply.

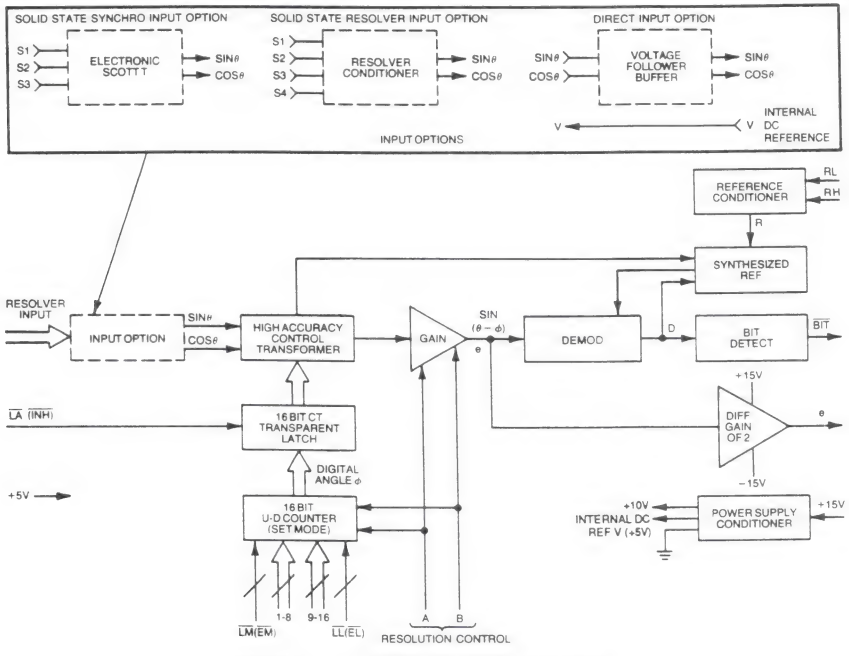
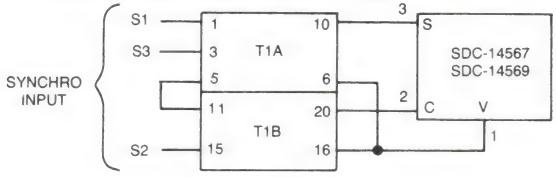
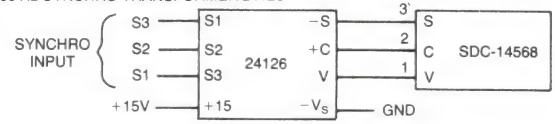


FIGURE 13. CT MODE BLOCK DIAGRAM

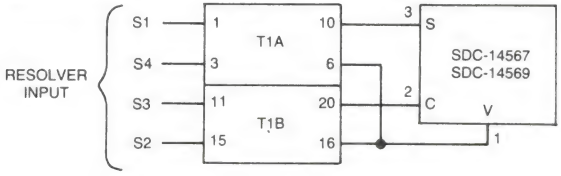
400 Hz SYNCHRO TRANSFORMER T1 21044 OR 21045



60 Hz SYNCHRO TRANSFORMER 24126



400 Hz RESOLVER TRANSFORMER T1 21046 OR 21047 OR 21048



400 Hz REF TRANSFORMER 21049

60 Hz REF TRANSFORMER 24133

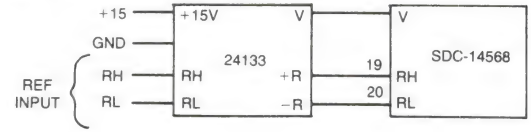
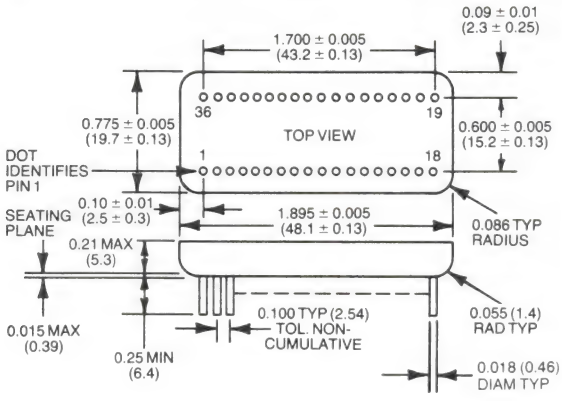


FIGURE 14. TRANSFORMER CONNECTION DIAGRAM



Notes:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is electrically floating.

FIGURE 15. SDC-14560 MECHANICAL OUTLINE, 36 PIN DDIP

ORDERING INFORMATION

SDC-1456X-XXX

Accuracy:
- 1 = 6 min. +1LSB
- 2 = 4 min. +1LSB
- 4 = 2 min. +1LSB
- 5 = 1 min. +1LSB

Reliability Grade:
- 0 = Standard DDC procedures.
- 1 = Fully compliant with MIL-STD-883.
- 2 = Screened to MIL-STD-883 but without QCI testing.

Operation temperature range:
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

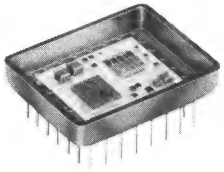
Configuration:
- 0 = 11.8V, 400Hz, Synchro
- 1 = 90V, 400Hz, Synchro
- 2 = 90V, 60Hz, Synchro
- 3 = 11.8V, 400Hz, Synchro, hi lin velocity
- 4 = 26V, 400Hz, Resolver
- 5 = 11.8V, 400Hz, Resolver
- 6 = 11.8V, 400Hz, Resolver, hi lin velocity
- 7 = 1V, 400Hz, Direct Resolver
- 8 = 1V, 60Hz, Direct Resolver
- 9 = 1.0V, 400Hz, Direct Resolver hi lin velocity

Drawings to DESC format available from factory.

K

SDC-14570/75 SERIES

14 & 16 BIT TRACKING S/D CONVERTERS



FEATURES

- *Fixed 14 or 14/16 Bit Programable*
- *$\overline{BIT}$ for ERROR, LOS, or LOR*
- *No 180° Hangup*
- *Small Size 1.0" X 0.8" Package*
- *Low Cost*
- *Velocity Output Eliminates Tachometer*
- *High Reliability Single Chip Monolithic*
- *-55°C to +125°C Operating Temperature Range*
- *883B Processing Available*

DESCRIPTION

The SDC-14570/75 Series are small low cost Synchro- or Resolver-to-Digital Converters based upon a single chip monolithic. A completely self-contained 14- or 16-bit synchro converter is housed in the SDC-14570/75 Series small 1.0" x 0.8" package. The SDC-14570 is fixed at 14 bits, the SDC-14575 is pin-programable 14 or 16 bits.

The velocity output (VEL) from the SDC-14570/75 Series, which can be used to replace a tachometer, is a 4V signal referenced to ground with a linearity of 1% of output voltage.

SDC-14570/75 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and 883B processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14570/75 Series converters are ideal for use in modern, high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

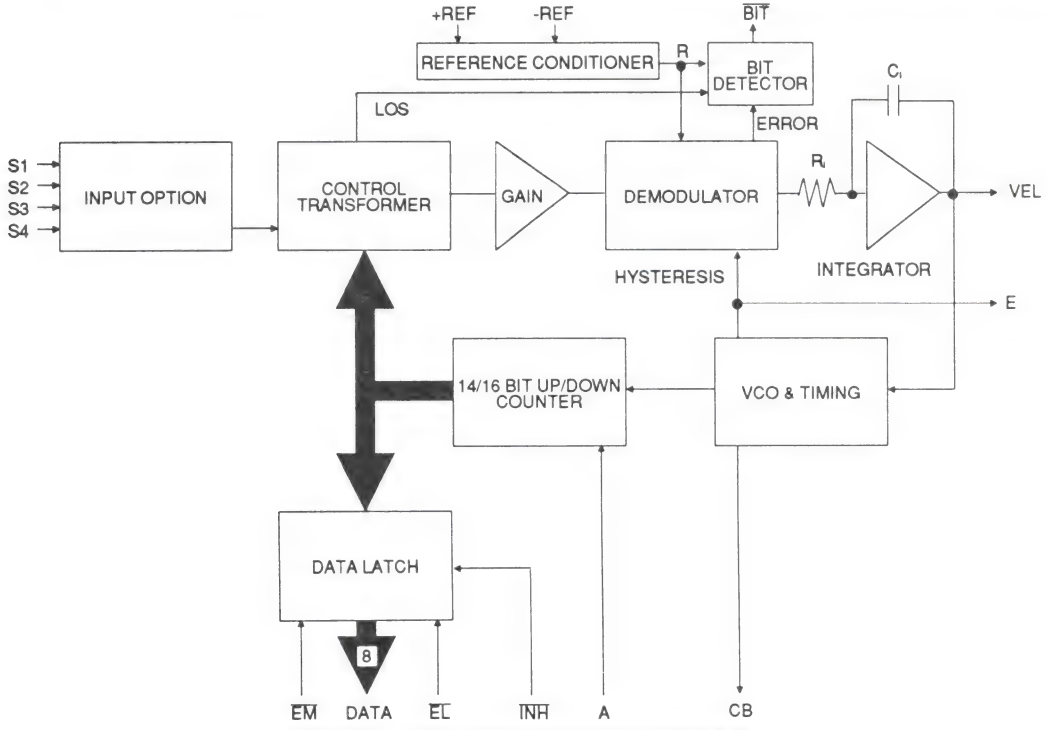


FIGURE 1. SDC-14570/75 BLOCK DIAGRAM

TABLE 1. SDC-14570/75 SPECIFICATIONS

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	14	16
ACCURACY	Min	4 + 1 LSB	2 + 1 LSB
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(+REF, -REF) differential	
Type		**2 & 11.8V units**	**90V unit**
Voltage Range	Vrms	2 - 35	10-130
Frequency	Hz	360 - 5000	47 - 1000
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	V_{peak}	50, 100 transient	200, 300 transient
SIGNAL INPUT CHARACTERISTICS			
90V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	123k	
Z_{in} line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	52k	
Z_{in} line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Z_{in} single ended	Ohm	70k	
Z_{in} differential	Ohm	140k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M // 10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pF max. CMOS transient protected	
Resolution Control (A)		**SDC-14575 Series only.** 30k pull-down to GND. Open = 14 bits; +5V = 16 bits	
Inhibit ($\overline{INH}$)		Logic 0 inhibits ; Data stable within 0.5µs	
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable within 150 ns	
Enable Bits 9 to 14(16) ($\overline{EL}$)		Logic 1 = High Impedance Data High Z within 100 ns	
Outputs			
Parallel Data (1-16)	bits	8 parallel lines; 2 bytes natural binary angle, positive logic	
Converter Busy (CB)	µs	0.3 - 1.0 positive pulse. Data valid 500ns max after leading edge.	

TABLE 1. SDC-14570/75 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT		
Outputs (continued)		
Built-In-Test ($\overline{BIT}$)		Logic 0 = BIT condition. ± 100 LSBs of error with a filter of 500µs. LOS or LOR
Drive Capability		50 pF +
	TTL	Logic 0; 1 TTL load, 1.6 mA at 0.4V max
		Logic 1; 10 TTL loads, -0.4 mA at 2.8V min
	CMOS	Logic 0; 100mV max driving CMOS
		Logic 1; +5V supply minus 100mV min driving CMOS

DYNAMIC CHARACTERISTICS		**Device Type**			
		60Hz		**400Hz**	
Input Frequency	Hz	47 - 1k		360 - 5k	
Bandwidth(Closed Loop)	Hz	15		103	
Ka	$1/s^2$	830		53k	
A1	1/s	0.17		1.33	
A2	1/s	5k		40k	
A	1/s	29		230	
B	1/s	14.5		115	
Resolution	**bits**	**14**	**16**	**14**	**16**
Tracking Rate					
typical	rps	1.25	0.31	10	2.5
minimum	rps	1	0.25	8	2
Accelleration (1LSB lag)	deg/s^2	18	4.5	1160	290
Settling Time (179°step max)	msec	1100	2500	140	320

VELOCITY CHARACTERISTICS			
Polarity		Positive for increasing angle	
Voltage Range(Full Scale)	±V	4.5 typ, 4 min	
Voltage Scaling	rps/FS	10	
Scale Factor	±%	10 typ	20 max
Scale Factor TC	ppm/°C	100 typ	200 max
Reversal Error	±%	1 typ	2 max
Linearity	±%	0.5 typ	1 max
Zero Offset	mV	5 typ	10 max
Zero Offset TC	µV/°C	15 typ	30 max
Load	kOhm		20 max
Noise	(VpV)%	1 typ	2 max
DC ERROR (E)	V	-1.25 per +1LSB error filtered (± 3 LSB range)	
POWER SUPPLIES			
Nominal Voltage	V	+5	-5
Voltage Range	±%	5	10
Max Volt. w/o Damage	V	+7	-7
Current	mA	12 typ,17 max	
TEMPERATURE RANGE			
Operating			
-30X	°C	0 to +70	
-10X	°C	-55 to +125	
Storage	°C	-65 to +150	
PHYSICAL CHARACTERISTICS			
Size	in	0.98 x 0.78 x 0.2	
	(mm)	(24.9 x 19.8 x 5.1)	
Weight	oz	0.66	

THEORY OF OPERATION

The SDC-14570/75 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

Figure 1 is the Functional Block Diagram of SDC-14570 Series. The SDC-14570 Series is fixed at 14 bits. The SDC-14575 is pin programable for 14- or 16-bit operation using resolution control line "A". A logic 0 (open line) will select 14 bits; a logic 1 will select 16-bit operation. The converter operates with ± 5Vdc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram and its Bode Plots (open and closed loop); These are shown in figures 1 and 2.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient
and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod)
- Integrator gain = $\frac{1}{R_iC_i}$ volts per second per volt
- VCO Gain = $\frac{1}{1.25R_VC_V}$ LSBs per second per volt

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the SDC-14570 Series converters:

1) Power supplies are ± 5Vdc. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.
2) Direct inputs are referenced to Analog Ground.
3) Digital Ground should be connected to Analog Ground as close to the package as possible.

E

INHIBIT and ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{EM}$) is used for the most significant 8 bits and Enable LSBs ($\overline{EL}$) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

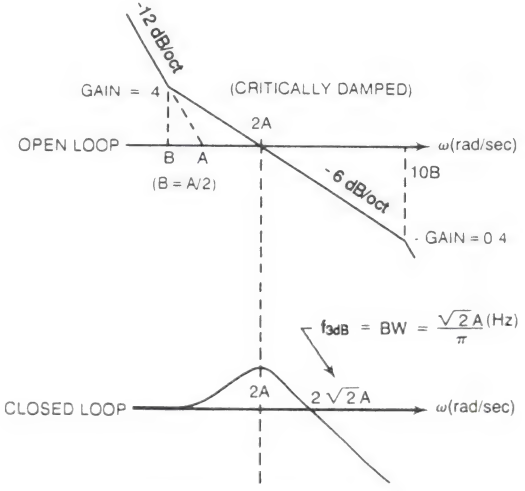


FIGURE 2. BODE PLOTS

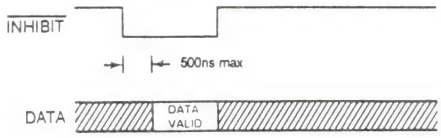


FIGURE 3. INHIBIT TIMING

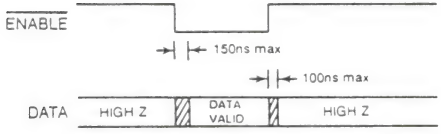


FIGURE 4. ENABLE TIMING

BIT, BUILT-IN-TEST

This output is a logic line that will flag an internal fault condition, LOS (Loss-Of-Signal), or LOR (Loss-Of-Refernce). The internal fault detector monitors the internal loop error and, when it exceeds ± 100LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500µs filter.) $\overline{BIT}$ will set for an overvelocity condition because the converter loop can't maintain input/output sync. $\overline{BIT}$ will also be set if either a LOS or LOR input occurs.

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB"(or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

The condition is artificial, as a "real" synchro or resolver can't change its output 180° instantaneously. The condition is most often noticed during wrap-around verification tests, simulations, or troubleshooting.

TABLE 2. PINOUT (26 PIN)*

1	S1(S)	S1(R)	N.C	26	+REF	(+Reference Input)
2	S2(S)	S2(R)	+COS(D)	25	- REF	(-Reference Input)
3	S3(S)	S3(R)	+SIN(D)	24	Analog Ground	
4	N.C.	S4(R)	N.C.	23	$\overline{EM}$	(Enable MSBs)
5	A (Resolution Control)**			22	E	(DC Error Output)
6	Digital Ground			21	VEL	(Velocity Output)
7	- 5V	(Power Supply)		20	$\overline{INH}$	(Inhibit)
8	+5V	(Power Supply)		19	$\overline{EL}$	(Enable LSBs)
9	Bit 1(MSB)		/Bit 9	18	$\overline{BIT}$	(Built-In-Test)
10	Bit 2		/Bit 10	17	CB	(Converter Busy)
11	Bit 3		/Bit 11	16	Bit 8	/Bit 16**
12	Bit 4		/Bit 12	15	Bit 7	/Bit 15**
13	Bit 5		/Bit 13	14	Bit 6	/Bit 14

* Note: (S) = Synchro; (R) = Resolver; (D) = 2V Resolver Direct

** Note: SDC-14575 Series only

Dimensions are in inches (millimeters).

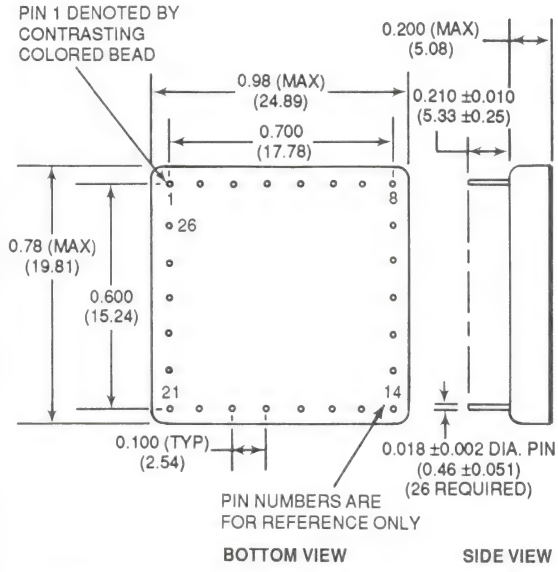


FIGURE 5. SDC-14570/75 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC- 1457X - X X X

Accuracy:
- 2 = 4 min + 1 LSB
- 4 = 2 min + 1 LSB

Reliability:
- 0 = Standard DDC procedures
- 1 = 883B Processing Available*
- 2 = 168 hour burn-in at 125°C*

Operating Temperature Range:
- 1 = -55 to +125°C
- 3 = 0 to +70°C (standard reliability only)

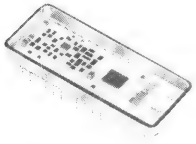
Input Option:
- 0 = 11.8V, Synchro, 14 bit, 400Hz
- 1 = 11.8V, Resolver, 14 bit, 400Hz
- 2 = 90V, Synchro, 14 bit, 400Hz
- 3 = 2V, Direct, 14 bit, 400Hz
- 4 = 90V, Synchro, 14 bit, 60Hz
- 5 = 11.8V, Synchro, 14/16 bit, 400Hz
- 6 = 11.8V, Resolver, 14/16 bit, 400Hz
- 7 = 90V, Synchro, 14/16 bit, 400Hz
- 8 = 2V, Direct, 14/16 bit, 400Hz
- 9 = 90V, Synchro, 14/16 bit, 60Hz

* -55° to +125°C Temperature range only.

B

DDC
ILC DATA DEVICE CORPORATION

SDC-14580



PROGRAMMABLE SYNCHRO/RESOLVER TO DIGITAL CONVERTER

DESCRIPTION

The SDC-14580 Series are versatile state-of-the-art synchro to digital converters featuring programmable resolution and a velocity output voltage.

Based on the popular SDC-14560 Series, the SDC-14580 offers a higher carrier frequency of 1 to 5kHz and a higher bandwidth of 540Hz. Tracking rate has also been increased and settling times decreased.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with commensurate accuracies up to 1 minute +1 LSB. Resolution programming combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in one package.

The velocity output (VEL) from the SDC-14580 is a ground based voltage of 0 to ±10Vdc with a linearity of 2%. Output voltage is positive for an increasing angle.

The digital angle output from the SDC-14580 is a natural binary code, parallel positive logic and is TTL/CMOS compatible.

APPLICATIONS

Because of its high reliability, accuracy, small size, and low power consumption, the SDC-14580 Series are ideal for the most stringent and severe industrial and military ground or avionics applications. 883B processing is available.

Designed with three-state outputs, the SDC-14580 is especially well suited for use with computer based systems. Among the may applications are: radar and navigation systems, fire control systems, flight instrumentation, and flight trainers/simulators.

FEATURES

- *Wide Bandwidth*
- *High Carrier Frequency*
- *Programmable Resolution: 10, 12, 14, or 16 Bits*
- *High Quality Velocity Output Eliminates Tachometer*
- *Accuracy To ±1.3 Arc Min.*
- *Synchro, Resolver, or Direct Inputs*
- *Synthesized Reference Eliminates 180° Lock-up*
- *883B Processing Available*

E

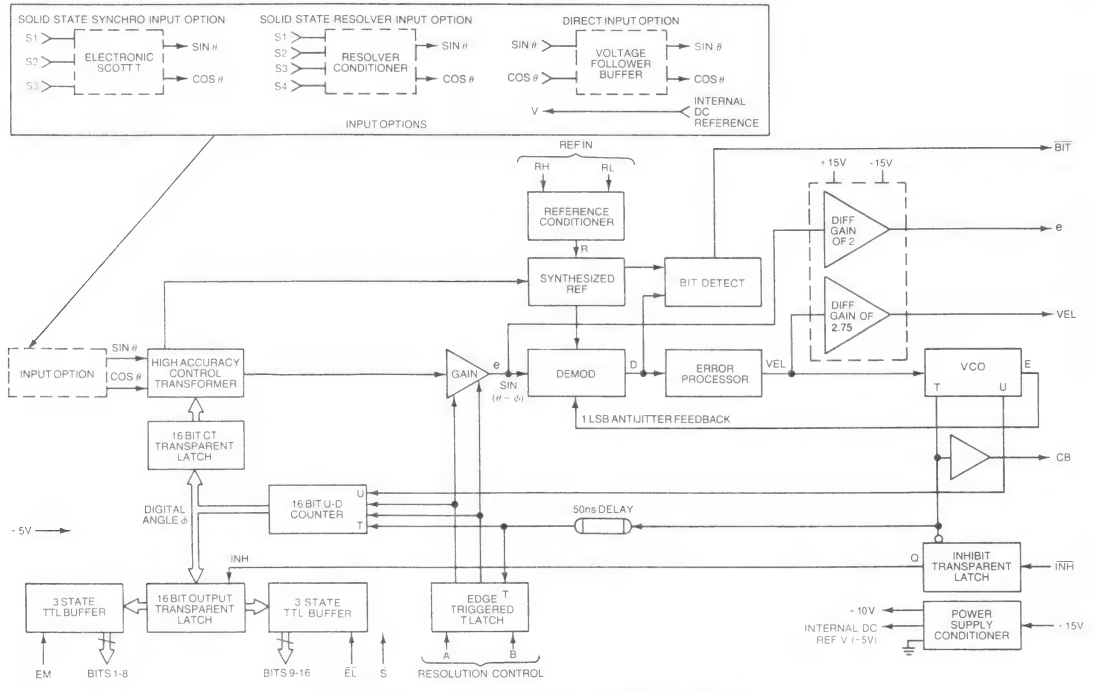


FIGURE 1. SDC-14580 BLOCK DIAGRAM

TABLE 1. SDC-14580 SPECIFICATIONS

These specifications apply over temperature range, power supply range, reference frequency, and amplitude range; 10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	COMMENT
RESOLUTION	10, 12, 14, or 16 bits	Pin Programmable
ACCURACY GRADES	±6, ±4, ±2, or ±1 minutes	Max +1 LSB of selected resolution, see Table 7 and Ordering Information.
DIFFERENTIAL LINEARITY	1 LSB max in the 16th bit	
REPEATABILITY	1 LSB max	
REF INPUT CHARACTERISTICS		
Voltage Range	1-35 Vrms	
Carrier Frequency Ranges		
10, 12, or 14 bit	1 - 5 kHz (full accuracy)	Up to 10 kHz with reduced accuracy
16 bit	2 - 5 kHz	
Input Impedance		
Single Ended Input	50k Ohm min	
Differential	100k Ohm min	
Common Mode Range	50V peak max, 200V transient peak	
SIGNAL INPUT CHARACTERISTICS		Voltage options and minimum input impedance, balanced.
Synchro	**11.8V L-L**	
Zin Line to Line	17.5k Ohm	
Zin Each line to ground	11.5k Ohm	
Common Mode Range	60V max	
Resolver	**11.8V L-L**	
Zin Single Ended	23k Ohm	
Zin Differential	46k Ohm	
Zin Each line to ground	23k Ohm	
Common Mode Range	60V max	
Direct (2.0V L-L)		
Input Signal Type		Sin and cos resolver signals referenced to converter internal DC reference voltage, V.
Sin/Cos Range	2Vrms nom, 2.2Vrms max	
Max Voltage Without Damage	**15V continuous, 100V peak transient**	
Input Impedance	Zin >20M // 10pF	
REFERENCE SYNTHESIZER		
±Sig/Ref Phase Shift	60° typ, 45° min	
DIGITAL INPUTS		
Logic Type		TTL/CMOS compatible
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Max Input Voltage w/o Damage	**-0.3Vdc to +8Vdc**	
Loading	10 µA max	Pull-up current source to +5V//5pf max, CMOS transient protected.
$\overline{INH}$ (Inhibit)		Logic 0 inhibits, Logic 1 enables, Data stable within 0.3 µs.
$\overline{EM}$ (Enable bits 1-8) and $\overline{EL}$ (Enable bits 9-16)		Logic 0 enables, Logic 1 high Z within 100 ns, Data valid within 150 ns.
$\overline{S}$ (Control Transformer)		Logic 0 for Control Transformer, Logic 1 for normal tracking.
Resolution Control	**B (pin 36)** / **A (pin 35)**	
10 Bit	0 / 0	
12 Bit	0 / 1	Unused output bits are at logic 0
14 Bit	1 / 0	
16 Bit	1 / 1	
DIGITAL OUTPUTS		
Parallel Data	10, 12, 14, or 16 bits	Natural binary angle, positive logic.
CB (Converter Busy)	0.4 µs to 1.0 µs	Positive pulse; leading edge initiates counter update.
$\overline{BIT}$ (Built-In-Test)		Logic 0 for $\overline{BIT}$ condition.

TABLE 1. SDC-14580 SPECIFICATIONS (continued)

These specifications apply over temperature range, power supply range, reference frequency, and amplitude range; +10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	COMMENT
DIGITAL OUTPUTS (continued)		
Drive Capability		
50pF plus rated logic drive.		
Logic 0	-1.6mA at 0.4V max	1 TTL Load
Logic 1	0.4mA at 2.8V min	10 TTL Loads
Logic 0	100mV max	driving CMOS
Logic 1	+5V supply minus 100mV min	driving CMOS
High Z	10uA/5pf max	
ANALOG OUTPUTS		
VEL (Velocity)		See Table 4, Velocity Output Characteristics
e (AC error)		
10 bit mode	50mVrms	per LSB of error
12 bit mode	25mVrms	per LSB of error
14 bit mode	12.5mVrms	per LSB of error
16 bit mode	6.3mVrms	per LSB of error
Load	3K Ohm min	
DYNAMIC CHARACTERISTICS		See Table 7, Dynamic Characteristics.
POWER SUPPLY CHARACTERISTICS		
Nominal Voltage and Range	+15Vdc ±5% / +5Vdc ±10%	-15Vdc ±5%
Max Voltage w/o Damage	**+18V** / **+8V**	**-18V**
Max Current	25mA / 10mA	15mA
TEMPERATURE RANGES		
Operating		
–30X	0°C to +70°C	
–10X	-55°C to +125°C	
Storage	-65°C to +150°C	
PHYSICAL CHARACTERISTICS		36 pin DDIP(Double Dip)
Size	1.9 x 0.78 x 0.21 inches	
Weight	(48.3 x 19.8 x 5.3mm) 0.7 oz (20 gm)	

TABLE 2. MAXIMUM RATINGS WITHOUT DAMAGE

PARAMETER	VALUE	COMMENT
Reference Inputs	65Vrms	**All power (i.e., power supply and signal inputs) should be removed from the circuit when adding or removing the converter.**
Direct signal Inputs	15V continuous, 100V peak transient	
Digital Inputs	-0.3Vdc to +8Vdc above the +5V supply	
Supply Voltage	+15Vdc +18V / +5Vdc +8V / -15Vdc -18V	
Storage Temperature	-65°C to +150°C	
Lead Temperature (soldering, ten seconds)	300°C	
Thermal Resistance: Junction to Case (θ_{JC}) Case to Ambient (θ_{CA})	8°C/W 20°C/W	

THEORY OF OPERATION

The SDC-14580 Series are small, 36 pin DDIP synchro to digital hybrid converters. As shown in the block diagram (figure 1) the SDC-14580 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.

Converter Operation

As shown in figure 1, the converter section of the SDC-14580 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO),up-down counter, and reference conditioner. The converter produces a digital angle which tracks the analog input angle to within the specified accuracy of the converter.

The control transformer performs the following trigonometric computation:

$$\sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta representing the resolver shaft position.

ϕ is digital angle phi contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) = 0$, so that ϕ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to $\sin(\theta-\phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It's single ended Input Z is 50k Ohms min, 100k Ohms differential.

SPECIAL FUNCTIONS

Reference Synthesizer — Quadrature Voltages.

The synthesized reference section of the SDC-14580 eliminates errors caused by quadrature voltage. Due to the inductive nature of synchros and resovers, their signals typically lead the reference signal (RH and RL) by about 6°. When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. In a 12 or 14 bit converter it is not necessary to compensate for the reference signal's phase shift. A 6° phase shift will, however, cause problems for the one minute accuracy converters. As shown in figure 1, the converter synthesizes its own $\cos(\omega t + \alpha)$ reference signal from the $\sin\theta \cdot \cos(\omega t + \alpha)$, $\cos\theta \cdot \cos(\omega t + \alpha)$ signal inputs and from the $\cos\omega t$ reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated. **The synthesized reference circuit also eliminates the 180° false error null hangup.**

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error=(Quadrature Voltage/F.S.signal) • $\tan(\alpha)$

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale sinal is in volts.
α = signal to REF phase shift

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: $\alpha = 6°$

Then: Magnitude of Error = 0.35 min ≅ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the synchro or resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage=(rotational speed/carrier frequency) • F.S.signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the synchro or resolver.
Carrier frequency is the REF in Hz.

SPECIAL FUNCTIONS - continued

Built-In-Test ($\overline{BIT}$, Pin 34)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero, if it exceeds approximately 65 LSBs (of the selected resolution) the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 1 for an over-velocity condition, because the converter loop cannot maintain input-output or and if the converter malfunctions where it cannot maintain the loop at a null. BIT will also be set if a Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR) occurs.

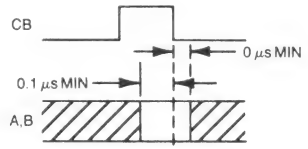


FIGURE 2. RESOLUTION CONTROL TIMING DIAGRAM

E

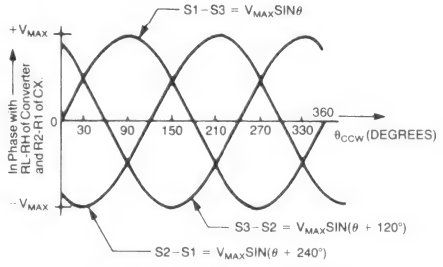
Programmable Resolution (A, PIN 35; B, PIN 36)

Resolution is controlled by two logic input, A and B (see Table 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are latched internally on the trailing edge of CB (see figure 2) For more information refer to the Accuracy and Resolution section.

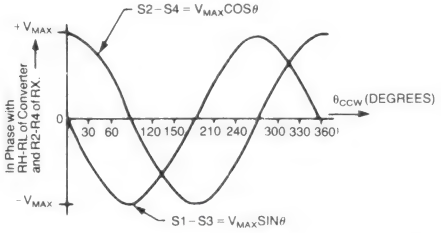
TABLE 3. RESOLUTION CONTROL

B (pin 36)	A (pin35)	RESOLUTION
0	0	16 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Note: All unused digital outputdata bits are at logic 0.



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 3. SYNCHRO AND RESOLVER SIGNALS

INTERFACING - INPUT

Signal Input Options

The SDC-14580 series offers 3 input options: synchro, resolver, or direct resolver input. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta+120^\circ)\cos\omega t$, and $\sin(\theta+240^\circ)\cos\omega t$ are internally converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Direct Resolver inputs accept 2Vrms inputs in resolver form, ($\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$) and are buffered prior to conversion. Figure 3 illustrates synchro and resolver signals as a function of the angle θ.

INTERFACING - INPUT (continued)

Signal Input Options (continued)

The solid-state signal and reference inputs are true differential inputs with high AC and DC common mode rejection.
Input impedance is maintained with power off.

The Synchro and Resolver input options are shown in figures 4 and 5.

The direct resolver inputs are transient protected voltage followers which accept 2.0Vrms resolver inputs as shown in figure 6.

Resistor Programming For Non-Standard Input Voltages

When applyng voltages greater than 2.0Vrms to the direct input option, a simple voltage divider can be used to attenuate both the sin and cos inputs. Since the converter inputs are voltage followers there will be no loading on the resistor dividers .
(See figure 7.)

The resolver input conditioner consists of two differential amplifiers. The input is currently scaled down with 23kohm resistors for the 11.8V resolver. When applying resolver input voltages greater than the rated voltages, four additional resistors are used to scale down the voltage. These resistors are placed one in series with each input line (see figure 8).

INTERFACING - DIGITAL OUTPUTS & CONTROLS

Digital Interface

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the SDC-14580.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-14580 applying an Inhibit ($\overline{INH}$) command will lock the data in the inhibit transparent latch without interfering with the continuous tracking of the converter's feedback loop. Therefore the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry.
For further information see the INHIBIT ($\overline{INH}$, PIN 33) paragraph.

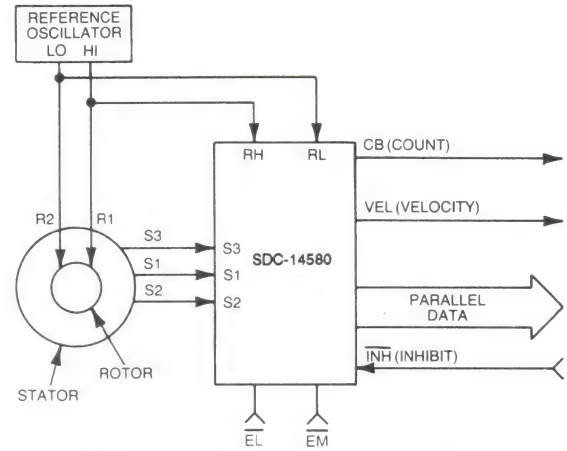


FIGURE 4. SYNCHRO INPUT CONNECTION DIAGRAM

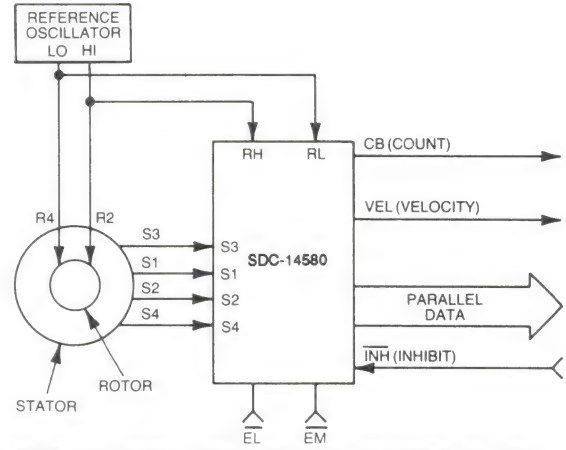


FIGURE 5. RESOLVER INPUT CONNECTION DIAGRAM

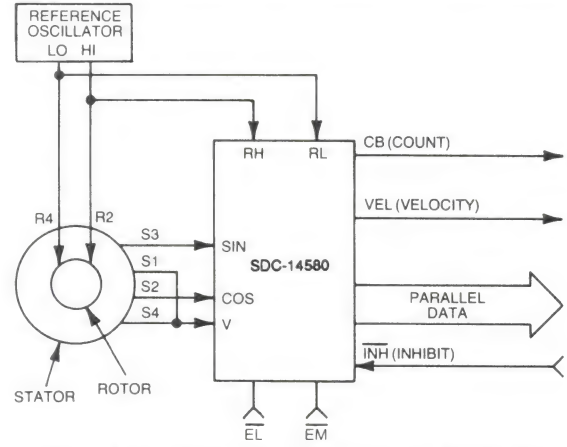
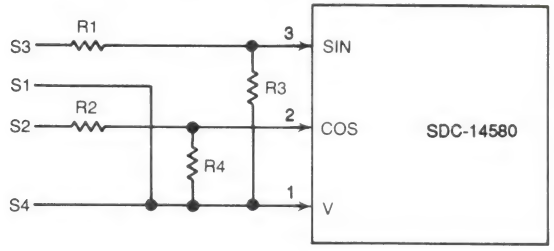


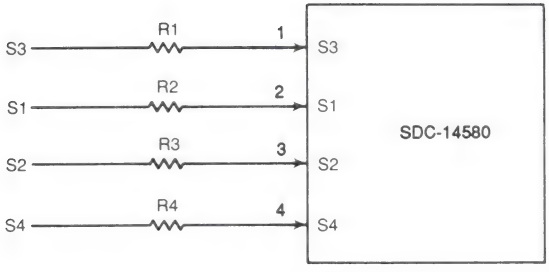
FIGURE 6. DIRECT INPUT CONNECTION DIAGRAM



$$\frac{\text{Input Voltage L-L}}{2V} = \frac{R1 + R3}{R3}$$

Notes:
(1) R1 = R2; R3 = R4 to 0.1% match.
(2) R1 + R3 and R2 + R4 should be as high as possible to minimize resolver loading.

FIGURE 7. DIRECT INPUT RESISTOR SCALING



$$\frac{R + 23K}{23K} = \frac{\text{Input Voltage L-L}}{11.8V}$$

Notes:
(1) Input Voltage L-L is greater than 11.8V.
(2) R = R1 = R2 = R3 = R4 to 0.1% match.

FIGURE 8. RESOLVER INPUT RESISTOR SCALING

INTERFACING - DIGITAL OUTPUTS & CONTROLS (continued)

Digital Angle Outputs (Logic Input/Output)

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 26) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 25) to a logic 0.

The second byte will contain either 9-10 (10 bit resolution), bits 9-12 (12 bit resolution), bits 9-14 (14 bit resolution), or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 4 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EM}$ and $\overline{EL}$ are set to logic 1 (see figure 9). Both enables are internally pulled up to +5V // 5pf max current sources.

E

TABLE 4. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1(MSB ALL MODES)	180	10,8000
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10 (LSB 10 BIT MODE)	0.3516	21.09
11	0.1758	10.55
12 (LSB 12 BIT MODE)	0.0879	5.27
13	0.0439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE	0.0055	0.33

Note: $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs.

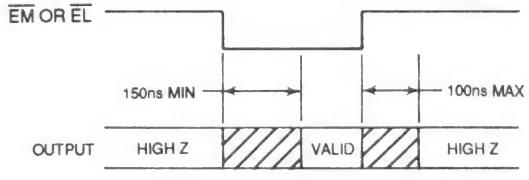


FIGURE 9. TRI-STATE OUTPUT TIMING

INTERFACING - DIGITAL OUTPUTS & CONTROLS (continued)

Digital Angle Output Timing

The digital angle output is 10, 12, 14, or 16 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive, 0.4 to 1.0 µs pulse.

The digital output data changes approximately 50ns after the leading edge of the CB pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB (see figure 10). The angle is determined by the sum of the bits at logic 1. The digital outputs are valid 150 ns max after $\overline{EM}$ or $\overline{EL}$ go low and are high impedance within 100ns max of $\overline{EM}$ or $\overline{EL}$ going high.

Inhibit ($\overline{INH}$, Pin 33)

When an Inhibit ($\overline{INH}$) input is applied to the SDC-14580, the Output Transparent Latch is locked causing the output data bits to remain stable while data is being transferred (see figure 11). The output data bits are stable 0.5µs after $\overline{INH}$ goes to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic 0 and the $\overline{INH}$ latch is transparent; when CB goes to logic 1, the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is: (1) Apply $\overline{INH}$; (2) Wait 0.5 µs min; (3) Transfer the data; (4) Release $\overline{INH}$.

A logic 1 for the $\overline{INH}$ enables the output data to be updated. $\overline{INH}$ must remain at a logic 1 for 1µs minimum (see figure 12).

Data Transfers

Digital output data from the SDC-14580 can be transferred to 8 bit and 16 bit bus systems. For 8 bit systems, the MSB and LSB bytes are transferred sequentially. For 16 bit systems all bits are transferred at the same time

Data Transfer To 8 Bit Bus

Figures 13 and 14 show the connections and timingfor transferring data from the SDC-14580 to an 8 bit bus

As can be seen by the timing diagram the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500ns before valid data is transferred.
2. $\overline{EM}$ is set to a low state (logic 0) 150ns MIN after $\overline{INH}$ goes low and must remain low for a minimum of 150ns before the MSB data (1- 8) is valid and transferred.
3. As $\overline{EM}$ is set to a high state (logic 1), $\overline{EL}$ is brought low for a 150ns MIN before the LSB data is valid and transferred.
4. $\overline{EL}$ should go high (to logic 1)at least 100ns MAX before another device uses the bus.
5. $\overline{INH}$ goes high and data transfer is done and the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100ns minimum before valid data is transferred.

Note: for further understanding refer to the beginning of this section (i.e. Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

16 Bit Data Transfer

Data transfer to the 16 bit bus is much simpler than the 8 bit bus. Figures 15 and 16 show the connections and timingfor transferring data from the SDC-14580 to an 8 bit bus

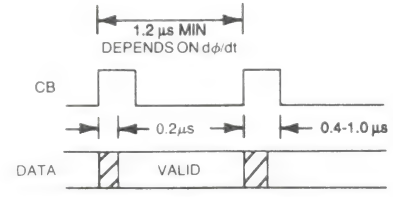


FIGURE 10. CONVERTER BUSY TIMING DIAGRAM

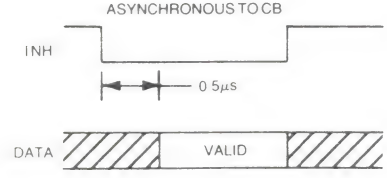


FIGURE 11. INHIBIT TIMING DIAGRAM

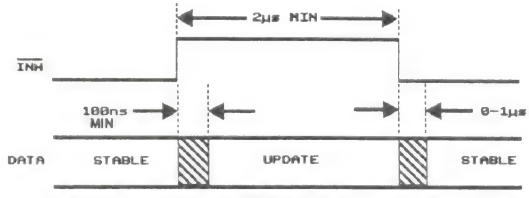


FIGURE 12. OUTPUT DATA UPDATE TIMING

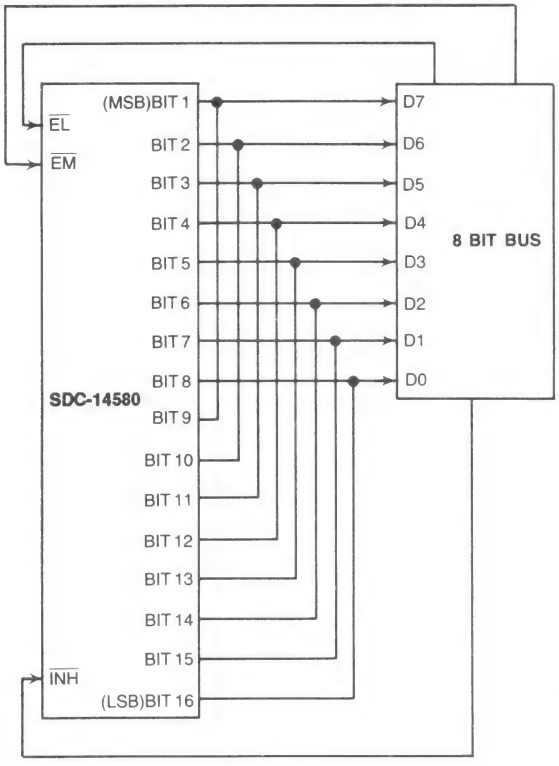


FIGURE 13. DATA TRANSFER TO 8 BIT BUS

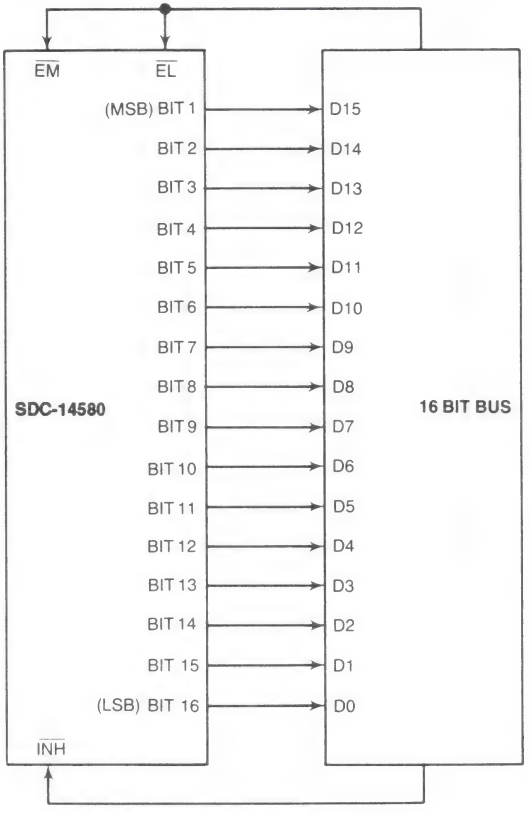


FIGURE 15. 16 BIT DATA TRANSFER

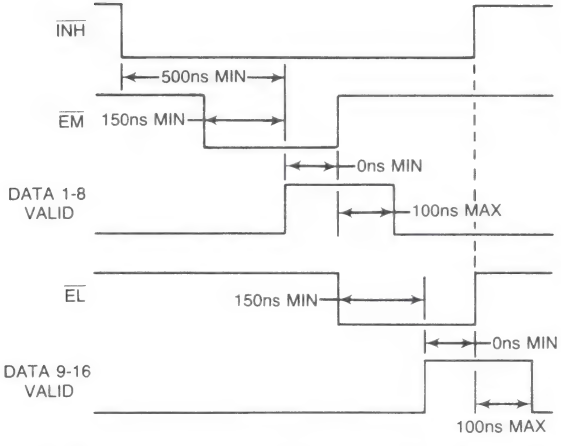


FIGURE 14. DATA TRANSFER TO 8 BIT BUS TIMING

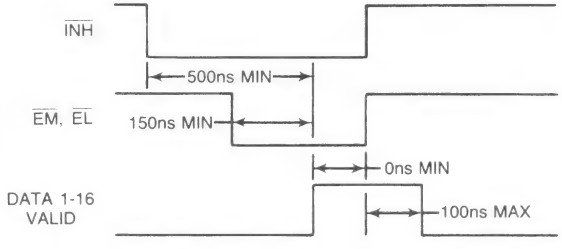


FIGURE 16. 16 BIT DATA TRANSFER TIMING

INTERFACING - DIGITAL OUTPUTS & CONTROLS (continued)

16 Bit Data Transfer (continued)

As can be seen by the timing diagram (page 9, Figure 16) the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500ns before valid data is transferred.

2. $\overline{EM}$ and $\overline{EL}$ are set to a low state (logic 0) 150ns MIN after $\overline{INH}$ goes low and must remain low for a minimum of 150ns before the data (1- 16) is valid and transferred.

3. $\overline{EM}$ and $\overline{EL}$ should go high (to logic 1)at least 100ns MAX before another device uses the bus.

4. $\overline{INH}$ goes high and data transfer is done and the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100ns minimum before valid data is transferred.

Note: for further understanding refer to the beginning of this section (i.e. Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

INTERFACING - ANALOG OUTPUTS

The analog outputs are AC error (e), Internal DC Reference Voltage, and Velocity (VEL).

AC Error (e, PIN 27)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the input angle θ and the digital input angle ϕ, $(\theta - \phi)$, with a scaling of:

50mVrms/LSB (10 bit mode)
25mVrms/LSB (12 bit mode)
12.5mVrms/LSB (14 bit mode)
6.3mVrms/LSB (16 bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10V min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level.

Internal DC Reference Voltage (V, PIN1)

This internal voltage is not required externally for normal operation of the converter. It is used as the internal dc reference common with the direct input option. It is nominally +5V and is proportional to the +15Vdc supply.

Velocity (VEL, PIN 23)

The velocity output (VEL, pin 23) is a dc voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The VEL output can swing ±10V with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in tables 4 and 5.

The VEL output has dc tachometer quality specs such that it can be used as the velocity feedback in servo applications.

TABLE 4. VELOCITY CHARACTERISTICS

PARAMETER	UNITS	TYP	MAX
Polarity		Positive for increasing angle	
Output Voltage	V	±13	±10 min
Voltage scaling	RPS/10V	See voltage scaling table 5	
Scale Factor	%	5	10
Scale Factor TC	PPM/°C	100	200
Reversal Error	%	1	2
Reversal Error TC	PPM/°C	25	50
Linearity	% output	1	2
linearity TC	PPM/°C	25	50
Zero offset	mV	15	40
Zero offset TC	µV/°C	25	50
Load	K Ohms	—	3 min

TABLE 5. VOLTAGE SCALING RESOLUTION (values in RPS/Volt)

10 BIT	12 BIT	14 BIT	16 BIT
80	20	5	1.25

Note: If the resolution is changed while the input is changing, then the velocity output voltage and the digital output will have a transient until it settles to the new velocity scaling at a speed determined by the bandwidth. If additional information is required, consult the factory.

Velocity Response

A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. The VEL filter is shown in figure 17.

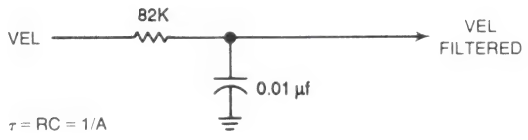


FIGURE 17. VEL OUTPUT FILTER

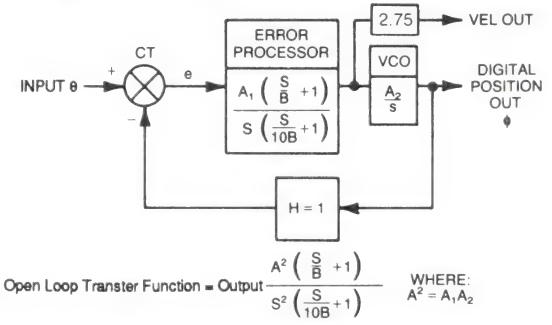


FIGURE 18. TRANSFER FUNCTION BLOCK DIAGRAM

E

INTERFACING - DYNAMIC PERFORMANCE

A Type II servo loop ($K_v = \infty$) and very high acceleration constants give the SDC-14580 superior dynamic performance. If the power supply voltages are not the +5Vdc nominal value, the specified input rates will increase or decrease in proportion to the fractional change in voltage.

Transfer Functions

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 18) and open and closed loop Bode plots (figures 19 and 20). Values for the transfer function block can be obtained from table 6.

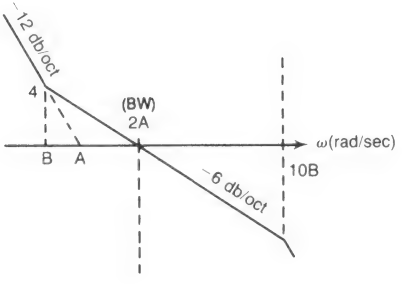


FIGURE 19. OPEN LOOP BODE PLOT

TABLE 6. DYNAMIC CHARACTERISTICS

PARAMETER	UNITS	BANDWIDTH			
RESOLUTION	BITS	10	12	14	16
Input Freq.	kHz	1-5	1-5	1-5	2-5
Tracking Rate	RPS min	800	200	50	12.5
Bandwidth	Hz	540	←	←	←
K_a	$1/sec^2$	1.5M	←	←	←
A_1	1/sec	6.2	←	←	←
A_2	1/sec	200k	←	←	←
A	1/sec	1.2k	←	←	←
B	1/sec	600	←	←	←
acc-1 LSB lag	Deg/sec^2	512k	128k	32k	8k
Settling Time	ms max	15	20	35	70
←Same as value to left					

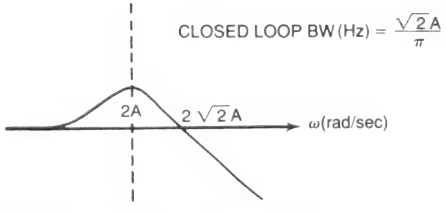


FIGURE 20. CLOSED LOOP BODE PLOT

INTERFACING - DYNAMIC PERFORMANCE (continued)

Response Parameters

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 21 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

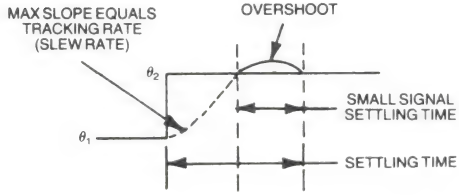


FIGURE 21. RESPONSE TO A STEP INPUT

Accuracy and Resolution

Table 7 lists the total accuracy including quantinization for the various resolution and accuracy grades.

TABLE 7. ACCURACY/RESOLUTION

ACCURACY	RESOLUTION (minutes)			
(minutes)	10 BIT	12 BIT	14 BIT	16 BIT
±1 +1LSB	22.1	6.3	2.3	1.3
±2 +1LSB	23.1	7.3	3.3	2.3
±4 +1LSB	25.1	9.3	5.3	4.3
±6 +1LSB	27.1	11.3	7.3	6.3

Faster Settling Time Using $\overline{BIT}$ to Reduce Resolution

Since the SDC-14580 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the SDC-14580 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit.

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

SPECIAL APPLICATIONS

Control Transformer (CT) Mode

The SDC-14580 can also be used as a Control Transformer (CT). The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the analog input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.

Referring to the equation below, the output is an AC voltage (e) which varies as the sine of the difference between the analog input angle and the digital angle.

$$e = \sin(\theta - \phi)\cos \omega t$$

The is analogous to the function of the rotary control transformer except in this case the rotary shaft input is replaced by a digital signal.

Figure 22 illustrate the CT block diagram. The CT mode is enabled by placing $\overline{S}$ (pin 30) to a logic 0 and by using the digital output lines (now bi-directional) as digital inputs.

When the SDC-14580 functions as a CT the digital inputs are double buffered, $\overline{EM}$ is redefined as $\overline{LM}$ (Latch MSBs), $\overline{EL}$ is redefined as $\overline{LL}$ (Latch LSBs) and $\overline{INH}$ becomes $\overline{LA}$ (Latch All).

Control transformers are frequently used as error signal generators in closed servo loops. The CT mode can be applied in servo systems, as shown in figure 23. In this application, changes in position are commanded by the microcomputer through signals fed to the CT. The CT then drives the motors through dc power amplifiers.

Using the SDC-14580 as an S/D with VEL to Stabilize Position Loop

Figure 24 illustrates a typical use of a SDC-14560 connected as an S/D using the VEL output to stabilize the position loop.

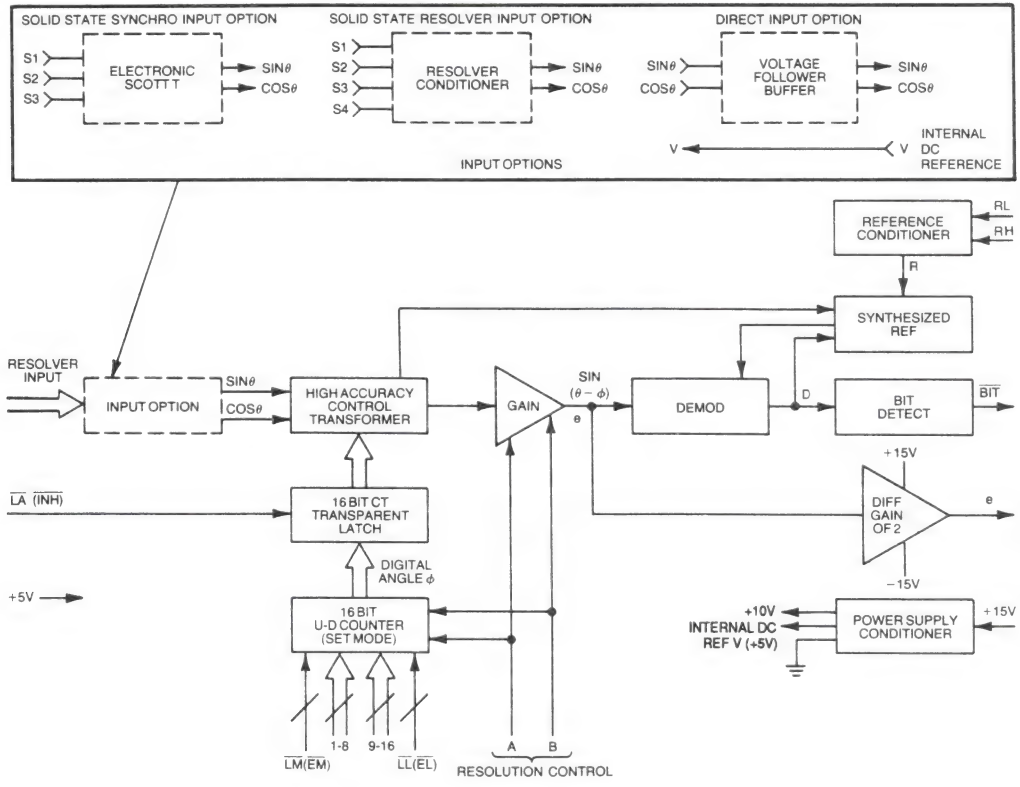


FIGURE 22. CT MODE BLOCK DIAGRAM

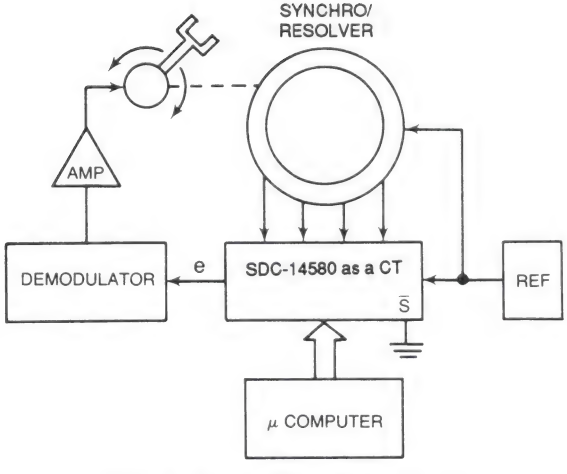


FIGURE 23. CT MODE APPLICATION

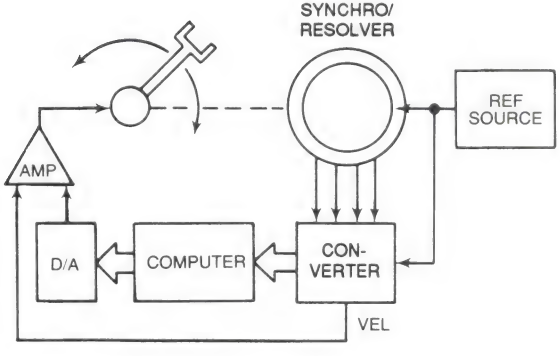


FIGURE 24.CONVERTER WITH VEL TO STABILIZE POSITION

SDC-14580 PIN DESIGNATIONS

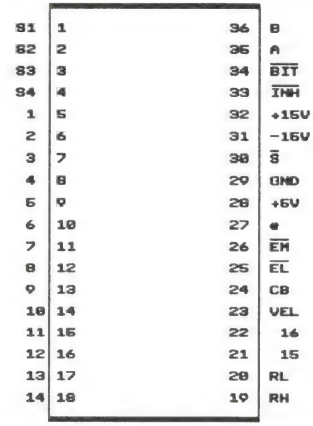


FIGURE 25. SDC-14580 PIN POSITIONS

TABLE 8. SDC-14580 PIN FUNCTIONS

PIN NO.	TITLE	I/O	FUNCTION
1	S1(S) S1(R) V(X)	I	(S)=Synchro input; (R)=Resolver input; (X)=Direct input.
2	S2(S) S2(R) +C(X)	I	(S)=Synchro input; (R)=Resolver input; (X)=Direct input.
3	S3(S) S3(R) +S(X)	I	(S)=Synchro input; (R)=Resolver input; (X)=Direct input
4	S4(R)	I	(R)=Resolver input.
5	1	O	Digital Output Bit 1 (MSB)
6	2	O	Digital Output Bit 2
7	3	O	Digital Output Bit 3
8	4	O	Digital Output Bit 4
9	5	O	Digital Output Bit 5
10	6	O	Digital Output Bit 6
11	7	O	Digital Output Bit 7
12	8	O	Digital Output Bit 8
13	9	O	Digital Output Bit 9
14	10	O	Digital Output Bit 10 (LSB - 10BIT MODE)
15	11	O	Digital Output Bit 11
16	12	O	Digital Output Bit 12 (LSB - 12 BIT MODE)
17	13	O	Digital Output Bit 13
18	14	O	Digital Output Bit 14 (LSB - 14 BIT MODE)
19	RH	I	AC Reference Input. Used to drive internal demodulator.
20	RL	I	AC Reference Input. Used to drive internal demodulator.
21	15	O	Digital Output Bit 15
22	16	O	Digital Output Bit 16 (LSB - 16 BIT MODE)
23	VEL	O	Velocity. DC voltage proportional to angular velocity.
24	CB	O	Converter Busy. Indicates digital output update.
25	$\overline{EL}$	I	Enable LSBs. Logic0 enables digital output bits 9-16. Logic 1 disablesthese bits.
26	$\overline{EM}$	I	Enable MSBs. Logic0 enables digital output bits 1-8. Logic 1 disablesthese bits.
27	e	O	AC Error. Used in CT mode; e is proportional to the difference between the input angle θ and the digital input angle ϕ, ($\theta - \phi$).
28	+5V	I	Supply Voltage.
29	GND	—	Ground.
30	$\overline{S}$	I	Control Transformer Set.Logic 1 for normal tracking; logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop bythe differenceangle of the resolver input and the digital input and for presetting the converter to a specific angle to reduce the step response time.
31	-15V	I	Supply Voltage.
32	+15V	I	Supply Voltage.
33	$\overline{INH}$	O	Inhibit. Logic 0 prevents digital output bits from changing.
34	$\overline{BIT}$	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65bits, approx. Also logic 0 for an over-velocity condition.
35	A	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bits dependent on logic level.
36	B	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bits dependent on logic level.

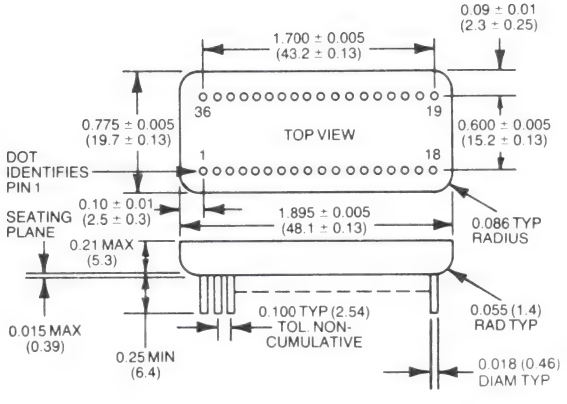
Since the SDC-14580 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

ORDERING INFORMATION

SDC-1458X - X X X

- Accuracy: 1 = 6 min. + 1LSB; 2 = 4 min. + 1LSB; 4 = 2 min. + 1LSB; 5 = 1 min. + 1LSB
- Reliability Grade: 0 = Standard DDC procedures. 1 = 883B processing available. 2 = 883B processing available but without QCI testing
- Operation temperature range: 1 = -55°C to +125°C; 3 = 0°C to 70°C
- Configuration: 0 = 11.8V, Synchro; 5 = 11.8V, Resolver; 7 = 2V, Direct Resolver

Drawings to DESC format available from factory.



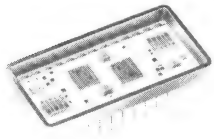
NOTES:
1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ± 0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Package is Kover with electroless nickel plating.
5. Case is electrically floating.

FIGURE 26. SDC-14580 MECHANICAL OUTLINE
36 PIN DDIP

DDC
ILC DATA DEVICE CORPORATION

SDC-14600/05 SERIES

TWO CHANNEL 14 & 16 BIT TRACKING S/D CONVERTERS



DESCRIPTION

The SDC-14600/05 Series are small low cost dual Synchro- or Resolver-to-Digital Converters. The SDC-14600 Series is fixed at 14 bits, the SDC-14605 at 16 bits. The two channels are independent tracking types but share digital output pins and a common reference.

The velocity output (VEL) from the SDC-14600/05 Series, which can be used to replace a tachometer, is a 4V signal referenced to ground with a linearity of 1% of output voltage.

A BIT output is optional and is a logic line that indicates LOR, LOS, or excessive converter error. Due to pin limitations this option will exclude the velocity output (contact factory).

SDC-14600/05 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and 883B processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14600/05 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

FEATURES

- *Fixed 14 or 16 Bit Resolution*
- *Small Size 28 Pin DDIP Package*
- *2 Independent Converters*
- *Low Cost*
- *Velocity Output Eliminates Tachometer*
- *Optional $\overline{BIT}$ Output*
- *High Reliability Single Chip Monolithic*
- *-55°C to +125°C Operating Temperature Range*
- *883B Processing Available*

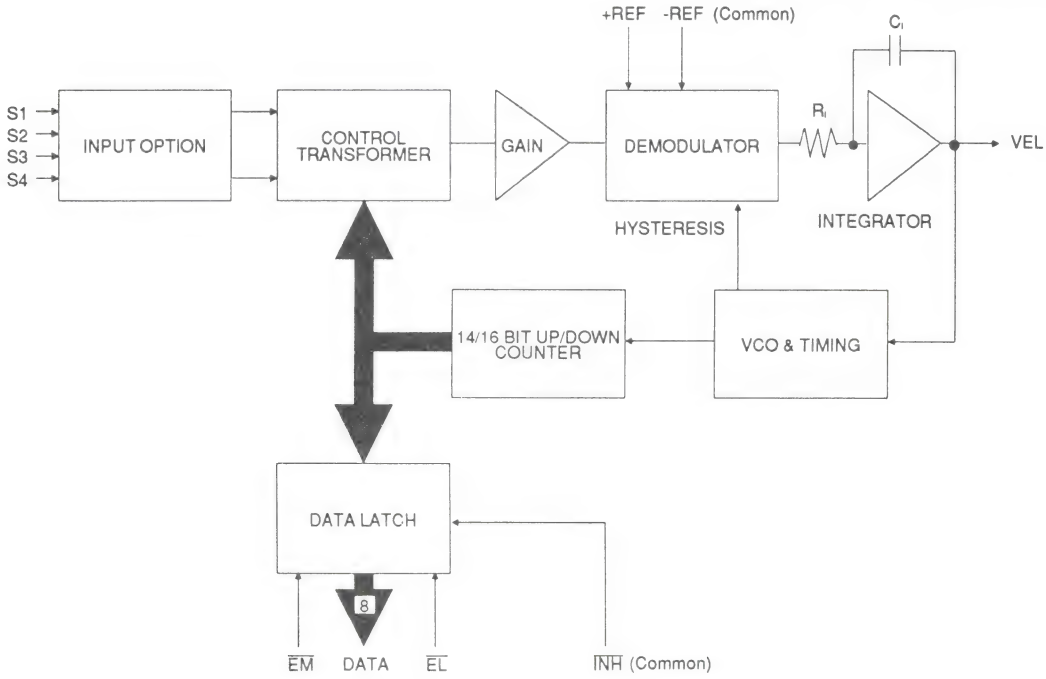


FIGURE 1. SDC-14600/05 BLOCK DIAGRAM (one channel)

TABLE 1. SDC-14600/05 SPECIFICATIONS (Each Channel)

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. **Each Channel unless stated otherwise.**

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	14	16
ACCURACY	Min	4(8) + 1 LSB	2(4) + 1 LSB
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(+REF, -REF), **Common to Both Channels**	
Type		differential	
		2 & 11.8V units	**90V unit**
Voltage Range	Vrms	2 - 35	10-130
Frequency	Hz	360 - 5000	47 - 1000
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	V_{peak}	50, 100 transient	200, 300 transient
SIGNAL INPUT CHARACTERISTICS		**Each Channel**	
90V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	123k	
Z_{in} line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	52k	
Z_{in} line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Z_{in} single ended	Ohm	70k	
Z_{in} differential	Ohm	140k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M // 10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max.	
		Logic 1 = 2.0V min.	
		Loading =10µa max P.U. current source to +5V //5pF max.	
		CMOS transient protected	
		Each Channel	
Inhibit ($\overline{INH}$)(common)		Logic 0 inhibits ; Data stable within 0.5µs	
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable	
Enable Bits 9 to 14(16) ($\overline{EL}$)		within 150 ns	
		Logic 1 = High Impedance	
		Data High Z within 100 ns	
Outputs		**Common to Both Channels**	
Parallel Data (1-14(16))	bits	8 parallel lines; 2 bytes natural binary angle, positive logic	

TABLE 1. SDC-14600/05 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE			
DIGITAL INPUT/OUTPUT					
Outputs (continued)					
		Each Channel			
Drive Capability	TTL	50 pF +			
		Logic 0; 1 TTL load, 1.6 mA at 0.4V max			
		Logic 1; 10 TTL loads, -0.4 mA at 2.8V min			
	CMOS	Logic 0; 100mV max driving CMOS			
		Logic 1; +5V supply minus 100mV min driving CMOS			
DYNAMIC CHARACTERISTICS		**Device Type**			
Each Channel		**60Hz**		**400Hz**	
Input Frequency	Hz	47 - 1k		360 - 5k	
Bandwidth(Closed Loop)	Hz	15		103	
Ka	$1/s^2$	830		53k	
A1	1/s	0.17		1.33	
A2	1/s	5k		40k	
A	1/s	29		230	
B	1/s	14.5		115	
Resolution	**bits**	**14**	**16**	**14**	**16**
Tracking Rate					
typical	rps	1.25	0.31	10	2.5
minimum	rps	1	0.25	8	2
Accelleration (1LSB lag)	deg/s^2	18	4.5	1160	290
Settling Time (179° step max)	msec	1100	2500	140	320
VELOCITY CHARACTERISTICS		**Each Channel**			
Polarity		Positive for increasing angle			
Voltage Range(Full Scale)	±V	4.5 typ, 4 min			
Voltage Scaling	rps/FS	10			
Scale Factor	±%	10 typ		20 max	
Scale Factor TC	ppm/°C	100 typ		200 max	
Reversal Error	±%	1 typ		2 max	
Linearity	±%	0.5 typ		1 max	
Zero Offset	mV	5 typ		10 max	
Zero Offset TC	µV/°C	15 typ		30 max	
Load	kOhm			20 max	
Noise	(Vp/V)%	1 typ		2 max	
POWER SUPPLIES		**Total Device**			
Nominal Voltage	V	+5	-5		
Voltage Range	±%	5	10		
Max Volt. w/o Damage	V	+7	-7		
Current	mA	24 typ,34 max			
TEMPERATURE RANGE					
Operating					
-30X	°C	0 to +70			
-10X	°C	-55 to +125			
Storage	°C	-65 to +150			
PHYSICAL CHARACTERISTICS					
Size	in	1.48 x 0.78 x 0.2			
	(mm)	(37.6 x 19.8 x 5.1)			
Weight	oz	0.66			

E

THEORY OF OPERATION

The SDC-14600/05 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

Figure 1 is the Functional Block Diagram of SDC-14600/05 Series. The converter operates with ±5Vdc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram and its Bode Plots (open and closed loop); These are shown in figures 1 and 2.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient

and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod)
- Integrator gain = $\frac{1}{R_iC_i}$ volts per second per volt
- VCO Gain = $\frac{1}{1.25R_vC_v}$ LSBs per second per volt

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the SDC-14600/05 Series converters:

1) Power supplies are ±5Vdc. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.
2) Direct inputs are referenced to A GND.

INHIBIT and ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in four bytes. The Enable MSB ($\overline{EM\ A}$ or $\overline{EM\ B}$) is used for the most significant 8 bits and Enable LSB ($\overline{EL\ A}$ or $\overline{EL\ B}$) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

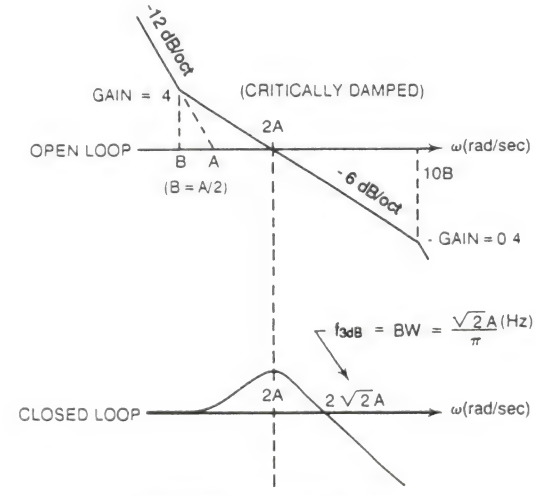


FIGURE 2. BODE PLOTS

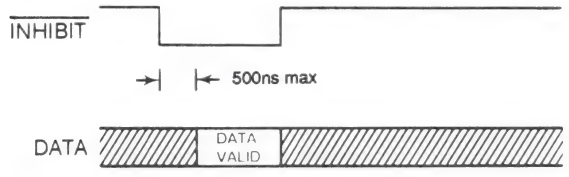


FIGURE 3. INHIBIT TIMING

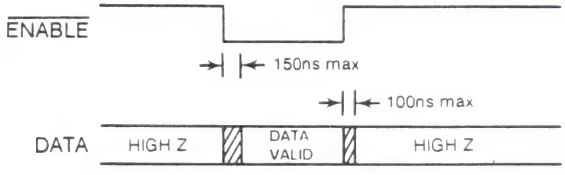


FIGURE 4. ENABLE TIMING

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB"(or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

The condition is artificial, as a "real" synchro or resolver can't change its output 180° instantaneously. The condition is most often noticed during wrap-around verification tests, simulations, or troubleshooting.

TABLE 2. PINOUT (28 PIN)*

1	S1A(S)	S1A(R)	A GND(D)	28	+REF	(+Reference Input)	
2	S2A(S)	S2A(R)	+COS(D)	27	- REF	(-Reference Input)	
3	S3A(S)	S3A(R)	+SIN(D)	26	- 5V	(Power Supply)	
4	N.C.	S4A(R)	N.C.	25	VEL A	(Velocity Output)	
5	Bit 1(MSB)		/Bit 9	24	$\overline{\text{EM A}}$	(Enable MSBs)	
6	Bit 2		/Bit 10	23	$\overline{\text{EL A}}$	(Enable LSBs)	
7	Bit 3		/Bit 11	22	GND	(Ground)	
8	Bit 4		/Bit 12	21	+5V	(Power Supply)	
9	Bit 5		/Bit 13	20	$\overline{\text{EL B}}$	(Enable LSBs)	
10	Bit 6		/Bit 14	19	$\overline{\text{EM B}}$	(Enable MSBs)	
11	Bit 7		/Bit 15**	18	N.C.	S4B(R)	N.C.
12	Bit 8		/Bit 16**	17	S3B(S)	S3B(R)	+SIN(D)
13	$\overline{\text{INH}}$	(Inhibit)		16	S2B(S)	S2B(R)	+COS(D)
14	VEL B	(Velocity Output)		15	S1B(S)	S1B(R)	AGND(D)

* Note: (S) = Synchro; (R) = Resolver; (D) = 2V Resolver Direct

** Note: SDC-14605 Series only

Dimensions in inches (mm).

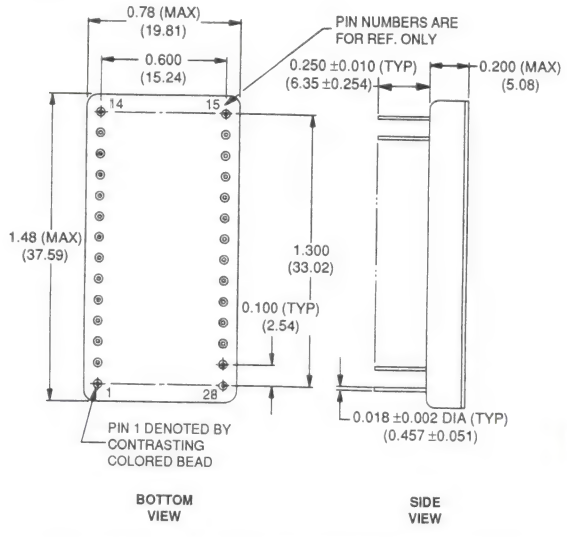


FIGURE 5. SDC-14600/05 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-1460X T - X X X

Accuracy:
- 2 = 4 min + 1 LSB
- 4 = 2 min + 1 LSB

Reliability:
- 0 = Standard DDC procedures
- 1 = 883B Processing Available*
- 2 = 168 hour burn-in at 125°C*

Operating Temperature Range:
- 1 = -55 to +125°C
- 3 = 0 to +70°C (standard reliability only)

Output Option:
- Blank = Standard Velocity Output (VEL)
- T = Built-In-Test Output, instead of VEL

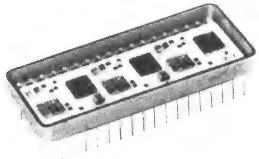
Input Option:
- 0 = 11.8V, Synchro, 14 bit, 400Hz
- 1 = 11.8V, Resolver, 14 bit, 400Hz
- 2 = 90V, Synchro, 14 bit, 400Hz
- 3 = 2V, Direct, 14 bit, 400Hz
- 4 = 90V, Synchro, 14 bit, 60Hz
- 5 = 11.8V, Synchro, 16 bit, 400Hz
- 6 = 11.8V, Resolver, 16 bit, 400Hz
- 7 = 90V, Synchro, 16 bit, 400Hz
- 8 = 2V, Direct, 16 bit, 400Hz
- 9 = 90V, Synchro, 16 bit, 60Hz

* -55° to +125°C Temperature range only.

DDC
ILC DATA DEVICE CORPORATION

SDC-14610/15 SERIES

THREE CHANNEL 14 & 16 BIT TRACKING S/D CONVERTERS



DESCRIPTION

The SDC-14610/15 Series are small low cost triple Synchro- or Resolver-to-Digital Converters. The SDC-14610 Series is fixed at 14 bits, the SDC-14615 at 16 bits. The three channels are independent tracking types but share digital output pins and a common reference.

The velocity output (VEL) from the SDC-14610/15 Series, which can be used to replace a tachometer, is a 4V signal referenced to ground with a linearity of 1% of output voltage.

A BIT output is optional and is a logic line that indicates LOR, LOS, or excessive converter error. Due to pin limitations this option will exclude the velocity output (contact factory).

SDC-14610/15 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and 883B processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14610/15 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

FEATURES

- ***Fixed 14 or 16 Bit Resolution***
- ***Small Size 36 Pin DDIP Package***
- ***3 Independent Converters***
- ***Low Cost***
- ***Velocity Output Eliminates Tachometer***
- ***Optional $\overline{BIT}$ Output***
- ***High Reliability Single Chip Monolithic***
- ***-55°C to +125°C Operating Temperature Range***
- ***883B Processing Available***

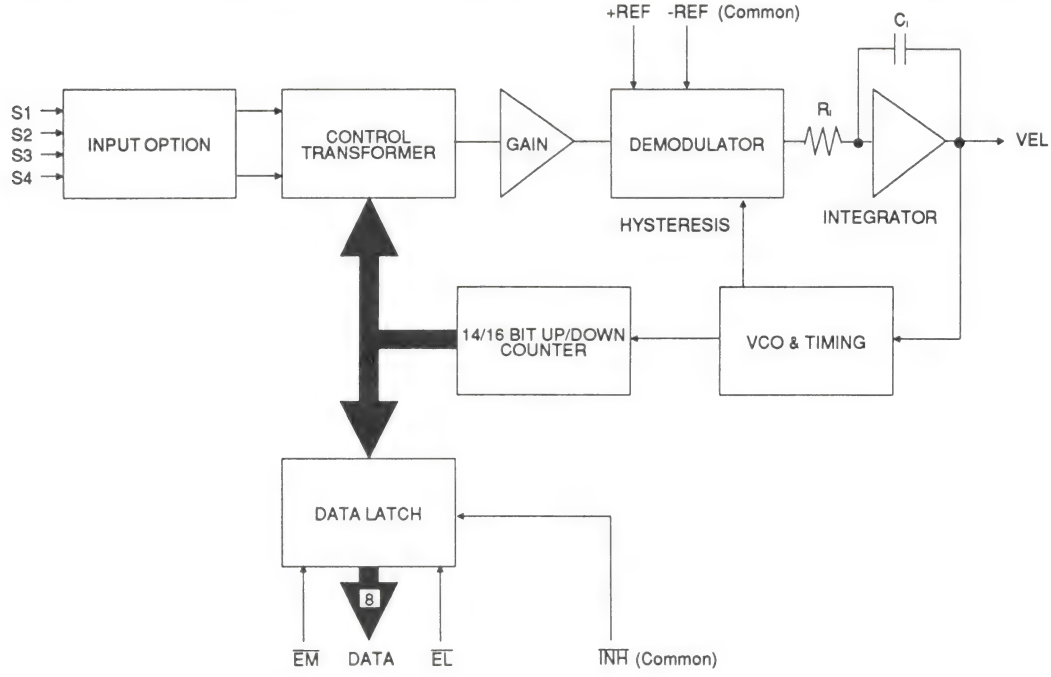


FIGURE 1. SDC-14610/15 BLOCK DIAGRAM (one channel)

TABLE 1. SDC-14610/15 SPECIFICATIONS (Each Channel)

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. **Each Channel unless stated otherwise.**

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	14	16
ACCURACY	Min	4(8) + 1 LSB	2(4) + 1 LSB
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(+REF, -REF), **Common to All Channels**	
Type		differential	
		2 & 11.8V units	**90V unit**
Voltage Range	Vrms	2 - 35	10-130
Frequency	Hz	360 - 5000	47 - 1000
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	V_{peak}	50, 100 transient	200, 300 transient
SIGNAL INPUT CHARACTERISTICS		**Each Channel**	
90V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	123k	
Z_{in} line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	52k	
Z_{in} line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Z_{in} single ended	Ohm	70k	
Z_{in} differential	Ohm	140k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M // 10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pF max. CMOS transient protected	
		Each Channel	
Inhibit ($\overline{INH}$)(common)		Logic 0 inhibits ; Data stable within 0.5µs	
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable	
Enable Bits 9 to 14(16) ($\overline{EL}$)		within 150 ns	
		Logic 1 = High Impedance	
		Data High Z within 100 ns	
Outputs		**Common to All Channels**	
Parallel Data (1-14(16))	bits	8 parallel lines; 2 bytes natural binary angle, positive logic	

TABLE 1. SDC-14610/15 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE			
DIGITAL INPUT/OUTPUT					
Outputs (continued)					
		Each Channel			
Drive Capability	TTL	50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, -0.4 mA at 2.8V min			
	CMOS	Logic 0; 100mV max driving CMOS Logic 1; +5V supply minus 100mV min driving CMOS			
DYNAMIC CHARACTERISTICS		**Device Type**			
Each Channel		**60Hz**		**400Hz**	
Input Frequency	Hz	47 - 1k		360 - 5k	
Bandwidth(Closed Loop)	Hz	15		103	
Ka	$1/s^2$	830		53k	
A1	1/s	0.17		1.33	
A2	1/s	5k		40k	
A	1/s	29		230	
B	1/s	14.5		115	
Resolution	**bits**	**14**	**16**	**14**	**16**
Tracking Rate					
typical	rps	1.25	0.31	10	2.5
minimum	rps	1	0.25	8	2
Accelleration (1LSB lag)	deg/s^2	18	4.5	1160	290
Settling Time (179°step max)	msec	1100	2500	140	320
VELOCITY CHARACTERISTICS		**Each Channel**			
Polarity		Positive for increasing angle			
Voltage Range(Full Scale)	±V	4.5 typ, 4 min			
Voltage Scaling	rps/FS	10			
Scale Factor	±%	10 typ		20 max	
Scale Factor TC	ppm/°C	100 typ		200 max	
Reversal Error	±%	1 typ		2 max	
Linearity	±%	0.5 typ		1 max	
Zero Offset	mV	5 typ		10 max	
Zero Offset TC	µV/°C	15 typ		30 max	
Load	kOhm			20 max	
Noise	(Vp/V)%	1 typ		2 max	
POWER SUPPLIES		**Total Device**			
Nominal Voltage	V	+5	-5		
Voltage Range	±%	5	10		
Max Volt. w/o Damage	V	+7	-7		
Current	mA	36 typ,51 max			
TEMPERATURE RANGE					
Operating					
-30X	°C	0 to +70			
-10X	°C	-55 to +125			
Storage	°C	-65 to +150			
PHYSICAL CHARACTERISTICS					
Size	in	1.70 x 0.78 x 0.21			
	(mm)	(43.2 x 19.8 x 5.3)			
Weight	oz	0.66			

E

THEORY OF OPERATION

The SDC-14610/15 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

Figure 1 is the Functional Block Diagram of SDC-14610/15 Series. The converter operates with ±5Vdc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram and its Bode Plots (open and closed loop); These are shown in figures 1 and 2.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient

and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod)
- Integrator gain = $\frac{1}{R_iC_i}$ volts per second per volt
- VCO Gain = $\frac{1}{1.25R_VC_V}$ LSBs per second per volt

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the SDC-14610/15 Series converters:

1) Power supplies are ±5Vdc. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.
2) Direct inputs are referenced to A GND.

INHIBIT and ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in six bytes. The Enable MSB ($\overline{EM\ A}$, $\overline{EM\ B}$, or $\overline{EM\ C}$) is used for the most significant 8 bits and Enable LSB ($\overline{EL\ A}$, $\overline{EL\ B}$, or $\overline{EL\ C}$) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

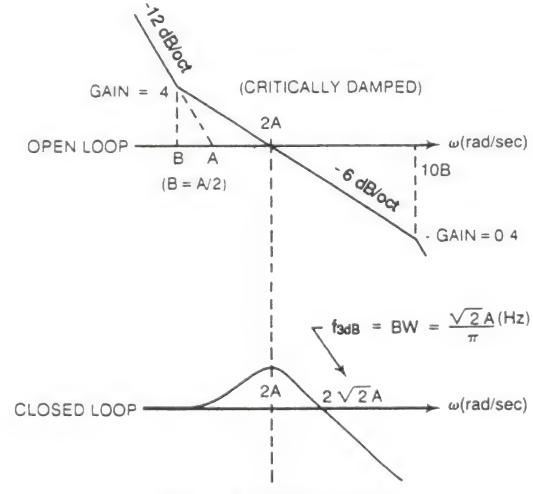


FIGURE 2. BODE PLOTS

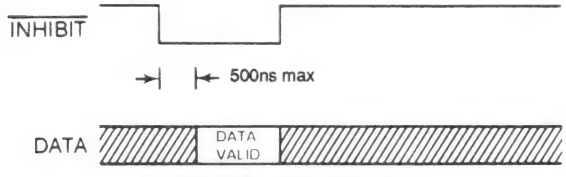


FIGURE 3. INHIBIT TIMING

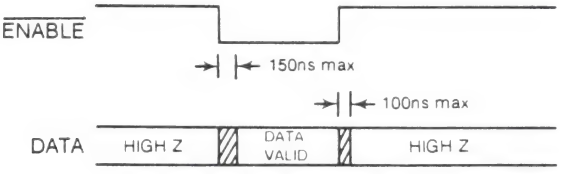


FIGURE 4. ENABLE TIMING

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB"(or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

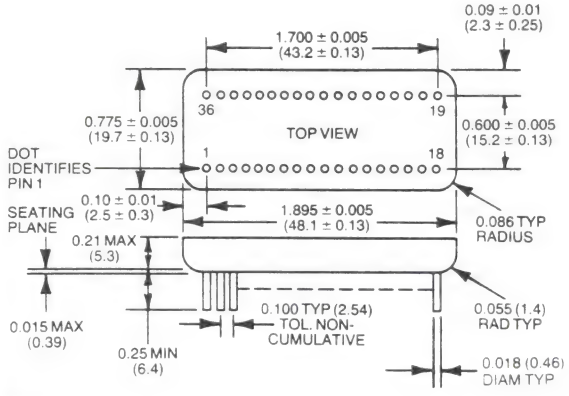
The condition is artificial, as a "real" synchro or resolver can't change its output 180° instantaneously. The condition is most often noticed during wrap-around verification tests, simulations, or troubleshooting.

TABLE 2. PINOUT (36 PIN)*

1	S1A(S)	S1A(R)	N.C.	36	VEL A	(Velocity Output)
2	S2A(S)	S2A(R)	+COSA(D)	35	$\overline{EM\ A}$	(Enable MSBs)
3	S3A(S)	S3A(R)	+SINA(D)	34	$\overline{EL\ A}$	(Enable LSBs)
4	N.C.	S4A(R)	N.C.	33	$\overline{INH}$	(Inhibit)
5	GND	(Ground)		32	VEL B	(Velocity Output)
6	A GND	(Analog Ground)		31	$\overline{EM\ B}$	(Enable MSBs)
7	S1B(S)	S1B(R)	N.C.	30	$\overline{EL\ B}$	(Enable LSBs)
8	S2B(S)	S2B(R)	+COSB(D)	29	Bit 8/Bit 16**	
9	S3B(S)	S3B(R)	+SINB(D)	28	Bit 7/Bit 15**	
10	N.C.	S4B(R)	N.C.	27	Bit 6/Bit 14	
11	- 5V	(Power Supply)		26	Bit 5/Bit 13	
12	+5V	(Power Supply)		25	Bit 4/Bit 12	
13	S1C(S)	S1C(R)	N.C.	24	Bit 3/Bit 11	
14	S2C(S)	S2C(R)	+COSC(D)	23	Bit 2/Bit 10	
15	S3C(S)	S3C(R)	+SINC(D)	22	Bit 1(MSB)/Bit 9	
16	N.C.	S4C(R)	N.C.	21	VEL C	(Velocity Output)
17	- REF	(-Reference Input)		20	$\overline{EL\ C}$	(Enable LSBs)
18	+REF	(+Reference Input)		19	$\overline{EM\ C}$	(Enable MSBs)

* Note: (S) = Synchro; (R) = Resolver; (D) = 2V Resolver Direct

** Note: SDC-14615 Series only



Notes:

1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is electrically floating.

FIGURE 5. SDC-14610/15 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-1461X T - X X X

Accuracy:
- 2 = 4 min + 1 LSB
- 4 = 2 min + 1 LSB

Reliability:
- 0 = Standard DDC procedures
- 1 = 883B Processing Available*
- 2 = 168 hour burn-in at 125°C*

Operating Temperature Range:
- 1 = -55 to +125°C
- 3 = 0 to +70°C (standard reliability only)

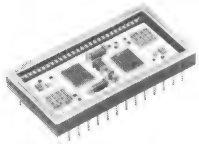
Output Option:
- Blank = Standard Velocity Output (VEL)
- T = Built-In-Test Output, instead of VEL

Input Option:
- 0 = 11.8V, Synchro, 14 bit, 400Hz
- 1 = 11.8V, Resolver, 14 bit, 400Hz
- 2 = 90V, Synchro, 14 bit, 400Hz
- 3 = 2V, Direct, 14 bit, 400Hz
- 4 = 90V, Synchro, 14 bit, 60Hz
- 5 = 11.8V, Synchro, 16 bit, 400Hz
- 6 = 11.8V, Resolver, 16 bit, 400Hz
- 7 = 90V, Synchro, 16 bit, 400Hz
- 8 = 2V, Direct, 16 bit, 400Hz
- 9 = 90V, Synchro, 16 bit, 60Hz

* -55° to +125°C Temperature range only.

DDC
ILC DATA DEVICE CORPORATION

SDC-14620 SERIES



TWO CHANNEL, PROGRAMMABLE SYNCHRO/RESOLVER-TO-DIGITAL CONVERTERS

PRELIMINARY

DESCRIPTION

The SDC-14620 Series are small, low-cost two-channel hybrid Synchro- or Resolver-to-Digital converters based on a single-chip monolithic. The two channels are independent but share the digital outputs and +5Vdc power pins. The package is 54 pin ceramic, the size of a 28 pin DDIP.

Resolution programming allows selection of 10, 12, 14, or 16 bit modes. This feature allows selection of either low resolution for fast tracking or higher resolution for higher accuracy.

The velocity outputs (VEL-A, VEL-B) from the SDC-14620 Series, which can be used to replace a tachometer, are ±4V signals referenced to analog ground with a linearity of 1% of output voltage.

The converter series also offers Built-In-Test outputs for each channel (BIT-A, BIT-B).

The SDC-14620 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C. 883B processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14620 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

FEATURES

- *Single 5V power supply*
- *10, 12, 14, or 16 bit programmable resolution*
- *2 Independent Converters*
- *Small 54 Pin Ceramic Package*
- *$\overline{BIT}$ Output*
- *Velocity Output Eliminates Tachometer*
- *High-Reliability Single-Chip Monolithic per Channel*
- *-55°C to +125°C Operating Temperature Range*
- *883B Processing Available*

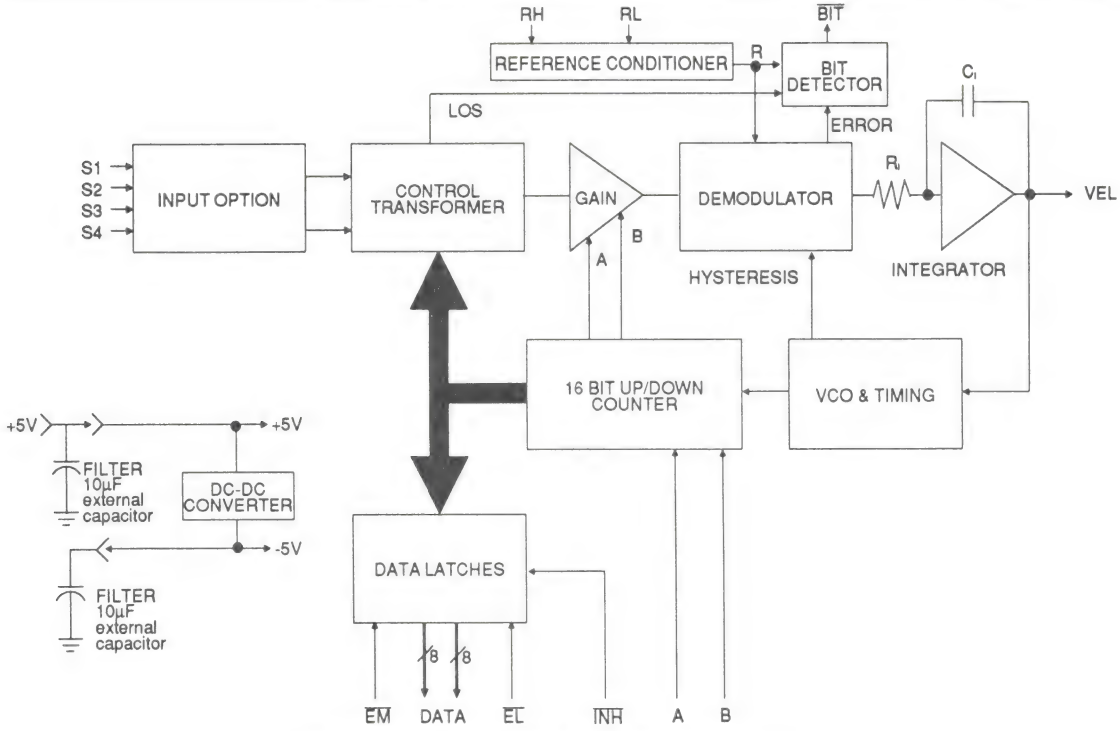


FIGURE 1. SDC-14620 BLOCK DIAGRAM (one channel)

TABLE 1. SDC-14620 SPECIFICATIONS (Each Channel)			
These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. **Each Channel unless stated otherwise.**			
PARAMETER	**UNIT**	**VALUE**	
RESOLUTION	Bits	programmable 10,12,14,or 16	
ACCURACY GRADES	Min	±2 or ±4, + 1LSB (see Table 4)	
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(RH,RL)	
		Each Channel	
Type		differential	
		2 & 11.8V units	**90V unit**
Voltage Range	Vrms	2 - 35	10-130
Frequency	Hz	360 - 5k	see note
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	V_{peak}	50, 100 transient	200, 300 transient
SIGNAL INPUT CHARACTERISTICS		**Each Channel**	
90V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	123k	
Z_{in} line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	52k	
Z_{in} line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Z_{in} single ended	Ohm	70k	
Z_{in} differential	Ohm	140k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M // 10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pF max. CMOS transient protected	
Resolution Control (A & B)		See Table 2.	
Each Channel		**Each Channel**	
Inhibit ($\overline{INH}$)(common)		Logic 0 inhibits ; Data stable within 0.5µs	
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable within 150 ns	
Enable Bits 9 to 16 ($\overline{EL}$)		Logic 1 = High Impedance Data High Z within 100 ns	
Outputs		**Common to Both Channels**	
Parallel Data	bits	16 parallel lines; 2 bytes natural binary angle, positive logic	

TABLE 1. SDC-14620 SPECIFICATIONS (continued)		
PARAMETER	**UNIT**	**VALUE**
DIGITAL INPUT/OUTPUT		
Outputs (continued)		
Each Channel		**Each Channel**
Built -In-Test		Logic 0 = BIT condition. ± 100LSBs of error with a filter of 500µs. LOS or LOR
Drive Capability	TTL	50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, -0.4 mA at 2.8V min
	CMOS	Logic 0; 100mV max Logic 1; +5V supply minus 100mV min
VELOCITY CHARACTERISTICS		**Each Channel**
Polarity		Positive for increasing angle
Voltage Range(Full Scale)	±V	4.5 typ 4 min
Scale Factor	±%	10 typ 20 max
Scale Factor TC	ppm/°C	100 typ 200 max
Reversal Error	±%	1 typ 2 max
Linearity	±%	0.5 typ 1 max
Zero Offset	mV	5 typ 10 max
Zero Offset TC	µV/°C	15 typ 30 max
Load	kOhm	20 max
Noise	(Vp/V)%	1 typ 2 max
POWER SUPPLIES		**Total Device**
Nominal Voltage	V	+5
Voltage Range	±%	5
Max Volt. w/o Damage	V	+7
Current	mA	48 typ, 68 max
TEMPERATURE RANGE		
Operating		
-30X	°C	0 to +70
-10X	°C	-55 to +125
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in(max) (mm)	1.50 x 0.78 x 0.21 (36.75 x 19.81 x 5.33)
Weight	oz	0.66

Note: 47 - 5k for 90V, 60Hz; 360 - 5k for 90V, 400Hz

TABLE 2. RESOLUTION CONTROL (A&B)		
Resolution	**B**	**A**
10 bit	0	0
12 bit	0	1
14 bit	1	0
16 bit	1	1

E

THEORY OF OPERATION

The SDC-14620 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology, which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

CONVERTER OPERATION

Figure 1 is the Functional Block Diagram of SDC-14620 Series. The converter operates with a single +5Vdc power supply and internally generates a minus voltage of approximately 5 volts. This minus voltage comes out on pin 24(channel 'B' filter point) and pin 52(channel 'A' filter point) — see GENERAL SETUP CONSIDERATIONS. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver, and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic, and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage, which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output), which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the SDC-14620 Series converters:

1) The power supply is +5Vdc. For lowest noise performance it is recommended that a 10µF/10Vdc (or larger)tantalum filter capacitor be connected to ground (pin 19) near the converter package.
2) Direct inputs are referenced to A GND.
3) Connect (close to the hybrid) pins 5 & 32(Analog Ground) to pin 19(GND).
4) A 10µF/10Vdc tantalum filter capacitor must be added externally from pin 24(channel 'B' filter point) to pin 19 (ground). Furthermore, a 10µF/10Vdc tantalum filter capacitor must be added externally from pin 52(channel 'A' filter point)to pin 19 (ground).

SPECIAL FUNCTIONS

PROGRAMMABLE RESOLUTION

Resolution is controlled by Pins 49 and 50 for channel A; pins 21 and 22 for channel B . The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist, between counting and changing the resolution, the resolution control is latched internally. Refer to Table 2 for Channel A and B resolution control.

$\overline{\text{BIT}}$, BUILT-IN-TEST

This output is a logic line that will flag an internal fault condition, LOS (Loss-Of-Signal), or LOR (Loss-Of-Reference). The internal fault detector monitors the internal loop error and, when it exceeds ± 100LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500µs filter.) $\overline{\text{BIT}}$ will set for an overvelocity condition because the converter loop can't maintain input/output sync. $\overline{\text{BIT}}$ will also be set if either a LOS or LOR input occurs.

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB"(or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

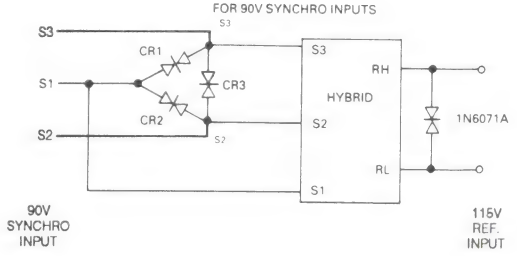
The condition is artificial, as a "real" synchro or resolver can't change its output 180° instantaneously. The condition is most often noticed during wrap-around verification tests, simulations, or troubleshooting.

INTERFACING

SOLID-STATE BUFFER INPUT PROTECTION — TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high ac and dc common rejection , so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent ac peak + dc common mode voltage should not exceed the values in Table 1.

The 90V line-to-line systems may have voltage transients which exceed the 300V specification listed in Table 1. **These transients can destroy the thin-film input resistor network in the hybrid.** Therefore, 90V L-L solid-state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever a synchro is switched on and off. For instance a 1000V transient can be generated when the primary of a CX or TX input is opened. See figure 2.



CR1, CR2, AND CR3 ARE IN6068A, BIPOLAR TRANSIENT VOLTAGE SUPPRESSORS OR EQUIVALENT.

FIGURE 2. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

INHIBIT and ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in four bytes. The Enable MSB ($\overline{EM}$-A or $\overline{EM}$-B) is used for the most significant 8 bits and Enable LSB ($\overline{EL}$-A or $\overline{EL}$-B) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

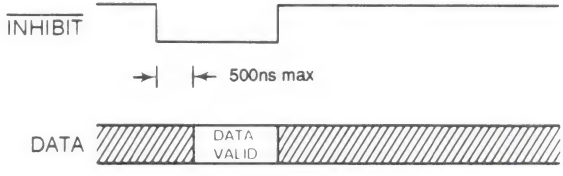


FIGURE 3. INHIBIT TIMING

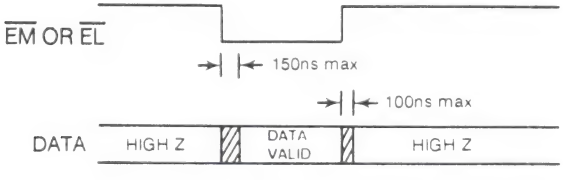


FIGURE 4. ENABLE TIMING

E

DYNAMIC PERFORMANCE

A Type II servo loop ($K_v = \infty$) and very high acceleration constants give the SDC-14620 superior dynamic performance.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram (figure 1), its transfer function block diagram (figure 5), and its Bode Plots (open and closed loop – figure 6). Values for the transfer function block can be obtained from Table 3.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient

and B is the frequency of lead compensation

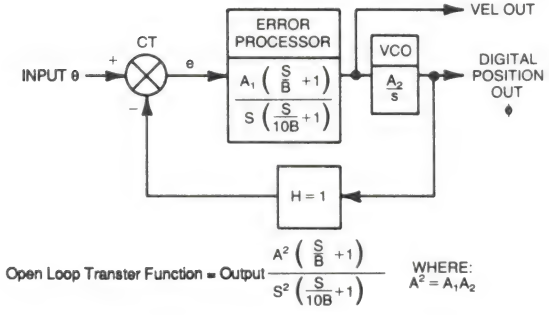


FIGURE 5. TRANSFER FUNCTION BLOCK DIAGRAM

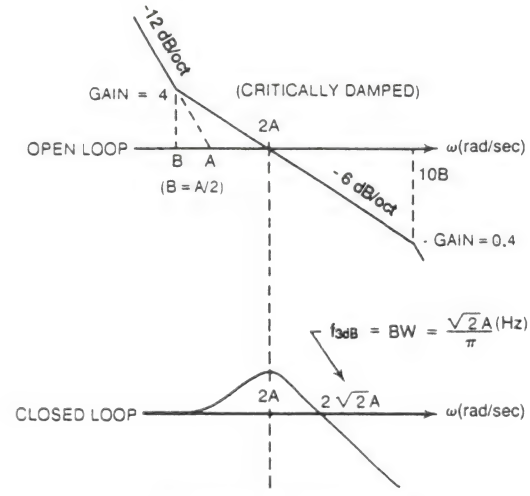


FIGURE 6. BODE PLOTS

ACCURACY AND RESOLUTION

Table 4 lists the total accuracy including quantinization for the various resolution and accuracy grades.

TABLE 4. ACCURACY/RESOLUTION

ACCURACY	RESOLUTION (minutes)			
(minutes)	10 BIT	12 BIT	14 BIT	16 BIT
±2 +1LSB	23.1	7.3	3.3	2.3
±4 +1LSB	25.1	9.3	5.3	4.3

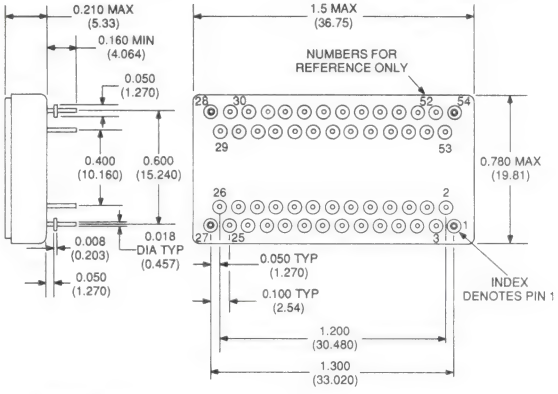
TABLE 3. DYNAMIC CHARACTERISTICS

Each Channel		DEVICE TYPE 60Hz				DEVICE TYPE 400Hz			
Input Frequency	Hz	47 - 5k				360 - 5k			
Bandwidth(Closed Loop)	Hz	15				103			
Ka	$1/s^2$	830				53k			
A1	1/s	0.17				1.33			
A2	1/s	5k				40k			
A	1/s	29				230			
B	1/s	14.5				115			
Resolution	**bits**	**10**	**12**	**14**	**16**	**10**	**12**	**14**	**16**
Tracking Rate (rps)									
typical	rps	32	8	2	0.5	160	40	10	2.5
minimum	rps	25.6	6.4	1.6	0.4	128	32	8	2
Accelleration (1LSB lag)	deg/s^2	720	180	45	11.3	18,600	4,640	1,160	290
Settling Time (179° step max)	msec	400	500	1,100	2,500	50	60	140	320

TABLE 4. PINOUT							
1	S1-A(R)	S1-A(S)	N.C.	54	VEL-A (Velocity Output chan.A)		
2	S2-A(R)	S2-A(S)	COS-A(D)	53	N.C.		
3	S3-A(R)	S3-A(S)	SIN-A(D)	52	Filter Point - Channel A		
4	S4-A(R)	N.C.	N.C.	51	$\overline{INH}$-A (Inhibit chan.B)		
5	A GND-A (analog gnd chan.A)			50	resolution control B (Channel A)		
6	RH-A (+Reference Input)			49	resolution control A (Channel A)		
7	RL-A (-Reference Input)			48	$\overline{EL}$-A (Enable LSBs chan. B)		
8	$\overline{EM}$-A (Enable MSBs chan. A)			47	N.C.		
9	$\overline{BIT}$-A (Built-In-Test chan. A)			46	Bit 16 (LSB, 16-bit mode)		
10	Bit 1 (MSB)			45	Bit 8		
11	Bit 9			44	Bit 15		
12	Bit 2			43	Bit 7		
13	Bit 10 (LSB, 10-bit mode)			42	Bit 14 (LSB, 14-bit mode)		
14	Bit 3			41	Bit 6		
15	Bit 11			40	Bit 13		
16	Bit 4			39	Bit 5		
17	Bit 12 (LSB, 10-bit mode)			38	$\overline{BIT}$-B (Built-In-Test chan. A)		
18	+5V (Power Supply)			37	$\overline{EM}$-B (Enable MSBs chan. B)		
19	GND (Ground)			36	N.C.		
20	$\overline{EL}$-B (Enable LSBs chan. B)			35	RL-B (-Reference Input)		
21	resolution control A (Channel B)			34	RH-B (+Reference Input)		
22	resolution control B (Channel B)			33	N.C.		
23	$\overline{INH}$-B (Inhibit chan.B)			32	A GND-B (analog gnd chan.B)		
24	Filter Point - Channel B			31	N.C.	S4-B(S)	N.C.
25	N.C.			30	S3-B(R)	S3-B(S)	+SIN-B(D)
26	VEL B (Velocity Output chan.B)			29	S2-B(R)	S2-B(S)	+COS-B(D)
27	N.C.			28	S1-B(R)	S1-B(S)	N.C.

Notes:

1. (S) = Synchro; (R) = Resolver; (D) = 2V Resolver Direct
2. Connect (close to the hybrid) pins 5 & 32 to pin 19.
3. Connect a 10µF/10Vdc tantalum filter cap from pins 24 to pin 19.
4. Connect a 10µF/10Vdc tantalum filter cap from pin 52 to pin 19.
5. Connect a 10µF/10Vdc tantalum filter cap from pin 18 to pin 19.



NOTES:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ± 0.005 (0.127) of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is hermetically sealed ceramic package.

FIGURE 7. SDC-14620 MECHANICAL OUTLINE

E

ORDERING INFORMATION

SDC- 1462X - X X X

Accuracy:
- 2 = 4 min + 1 LSB
- 4 = 2 min + 1 LSB

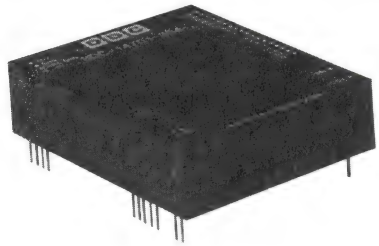
Reliability:
- 0 = Standard DDC procedures
- 1 = 883B Processing Available*
- 2 = 168 hour burn-in at 125°C*

Operating Temperature Range:
- 1 = -55 to +125°C
- 3 = 0 to +70°C (standard reliability only)

Input Option:
- 0 = 11.8V, Synchro, 400Hz
- 1 = 11.8V, Resolver, 400Hz
- 2 = 90V, Synchro, 400Hz
- 3 = 2V, Direct, 400Hz
- 4 = 90V, Synchro, 60Hz

*** -55°C to +125°C temperature range only**

A



5 DECADE SYNCHRO AND RESOLVER TO BCD CONVERTER

FULL DATA SHEET AVAILABLE

DESCRIPTION

The SDC-14700 converter is a pin programmable, high resolution (0.01°) synchro and resolver to BCD tracking converter. It continuously converts 3 wire synchro or 4 wire resolver information into BCD angle format, at rates up to 180° per second. Its operating frequency range is 47 Hz to 1200 Hz. The unit is available in accuracy grades of ±0.03° and ±0.05°.

An SDC-14701 converter, which operates with a 2 V signal, is also available. The SDC-14701 allows for the use of an inexpensive standard 400 Hz, 26/11.8 V or 26/12.6 V resolver at 60 Hz reference.

Both the SDC-14700 and the SDC-14701 are equipped with a ±2° offset adjust for system zeroing (Figure 1).

Digital outputs are CMOS and TTL compatible. The unique control transformer algorithm used in these units provide for inherently higher accuracy and jitter free output. Utilizing a type II servo loop, the converter has no velocity lag up to 180° per second, and the output data is always fresh and continuously available. Each unit is factory trimmed and requires no field adjustments or calibrations.

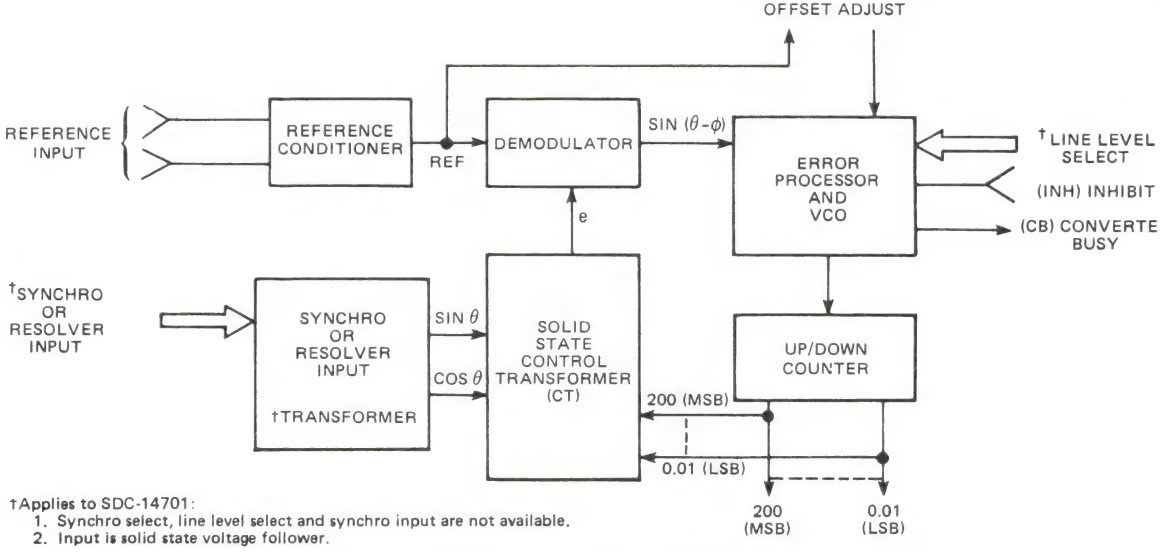
APPLICATIONS

The broad capabilities of the SDC-14700 and the SDC-14701 make them cost effective devices for use in systems where analog angle information must be converted into accurate high resolution BCD data. They are suitable for rugged industrial and commercial applications. Military uses include ground support and avionics, such as ordnance control, radar tracking systems, navigation and collision avoidance systems.

FEATURES

- *HIGH RESOLUTION: 0.01° (5 DECADE)*
- *HIGH ACCURACY: ±0.03° OR ±0.05°*
- *PIN PROGRAMMABLE: ACCEPTS ALL STANDARD SYNCHROS OR RESOLVERS*
- *OFFSET ADJUST FOR SYSTEM ZEROING*
- *FREQUENCY RANGE: 47 Hz TO 1200 Hz*

*Patented

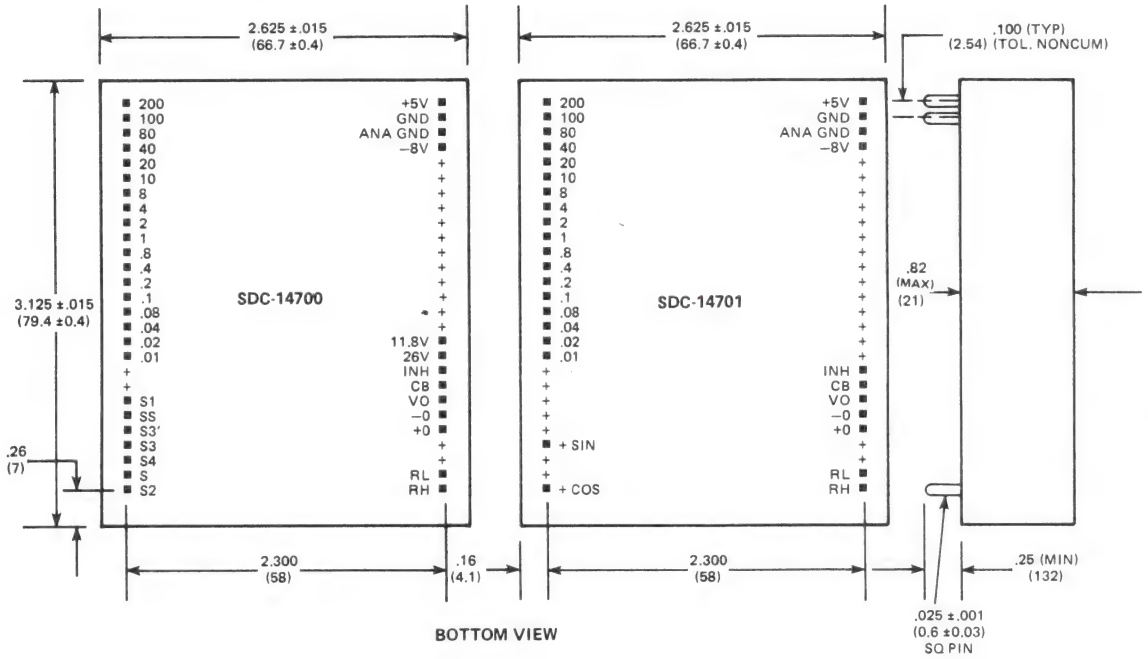


†Applies to SDC-14701:
1. Synchro select, line level select and synchro input are not available.
2. Input is solid state voltage follower.

FIGURE 1. BLOCK DIAGRAM

SDC-14700*

MECHANICAL OUTLINE



NOTES:
1. Pin material meets solderability requirements of MIL-STD-202 method 208.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, type SDG-F.
3. Pin callouts on bottom view for reference only.
4. Dimensions in inches (millimeters).

ORDERING INFORMATION

SDC-14700 - 3 9 4

- Accuracy Grade:
  - 4 = ± 0.05°
  - 5 = ± 0.03°
- Inputs:*
  - 9 = Standard (pin programmable 11.8 V, 26 V or 90 V)
  - 8 = 2 V (for direct input)
- Temperature Range:
  - 3 = 0°C to +70°C
- Type:
  - 0 = Standard
  - 1 = Direct Input
- Family Code

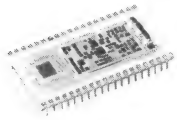
*SDC-14700 available with input option 9 only.
SDC-14701 available with input option 8 only.

B-ABR

DDC
ILC DATA DEVICE CORPORATION

SDC-19204 MONOBRID® SERIES

10, 12, 14, OR 16 BIT INDUSTRIAL SYNCHRO TO DIGITAL CONVERTERS



DESCRIPTION

The SDC-19204 Monobrid Series are versatile state-of-the-art synchro to digital converters featuring programmable resolution and bandwidth and a velocity output voltage.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with commensurate accuracies up to 2 minutes +1 LSB. Resolution programming combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in one package.

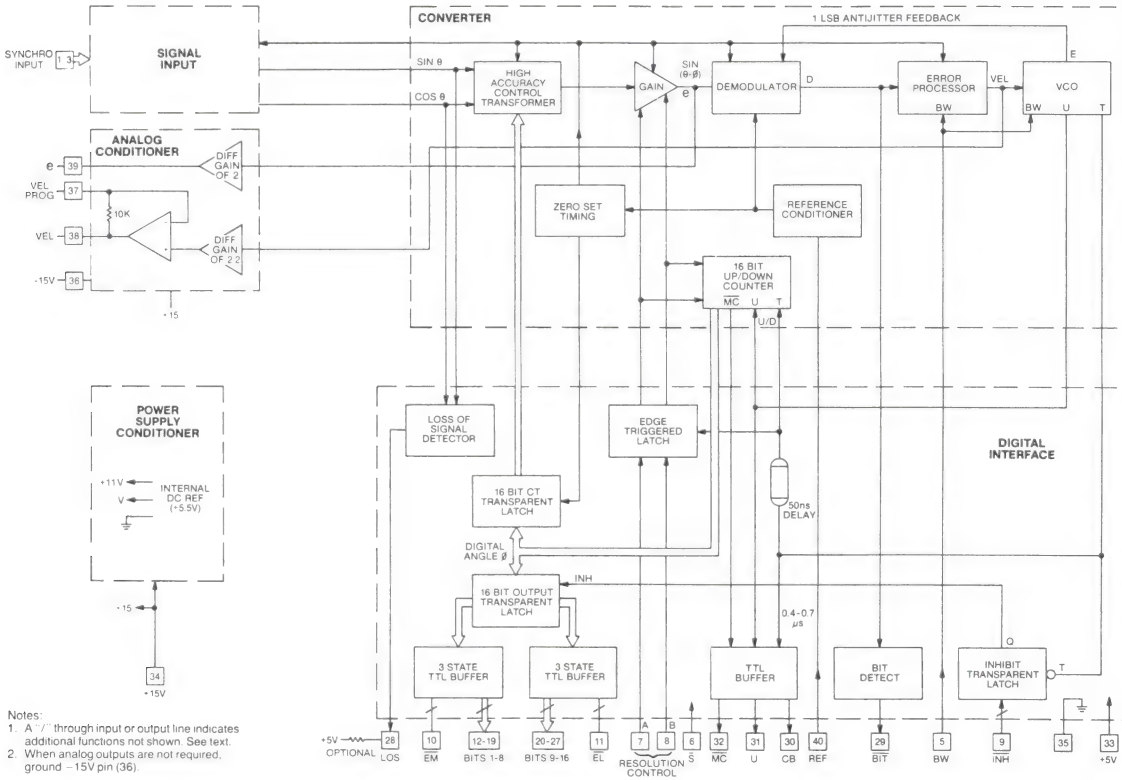
The velocity output (VEL) from the SDC-19204 is a ground based voltage of 0 to ±10VDC with a linearity of 2.0%. VEL may be scaled up by a single external resistor to provide up to ±10VDC for the required maximum tracking rate.

APPLICATIONS

The SDC-19204 Series converters are designed for use in modern high performance commercial and industrial control systems. Applications include motor control, theodolite, radar antenna position information, CNC machine tooling, robot axis control, and process control. With their low cost and superior performance, the SDC-19204 Series converters are ideal for motion control and position monitoring applications.

FEATURES

- *LOW COST*
- *IDEAL FOR MOTOR CONTROL*
- *BUILT-IN-TEST ($\overline{BIT}$) AND LOSS-OF-SIGNAL (LOS) OUTPUTS*
- *VELOCITY OUTPUT ELIMINATES TACHOMETER*
- *PROGRAMMABLE RESOLUTION*
- *PROGRAMMABLE BANDWIDTH*
- *ACCURACY TO ±2.3 ARC MIN.*



Notes:
1. A "/" through input or output line indicates additional functions not shown. See text.
2. When analog outputs are not required, ground -15V pin (36).

FIGURE 1. SDC-19204 BLOCK DIAGRAM

®Monobrid is a registered trademark of ILC Data Device Corporation.

TABLE 1. SDC-19204 SPECIFICATIONS

These specifications apply over temperature range, power supply range, reference frequency and amplitude range; ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	DESCRIPTION
RESOLUTION	10, 12, 14, or 16 bits	Programmable
ACCURACY GRADES	8, 4, 3, 2 minutes	Max +1 LSB of selected resolution, see Ordering Information
DIFFERENTIAL LINEARITY	16, 12, 8, or 4	LSBs in the 16th bit, see Ordering Information
REPEATABILITY	1 LSB max	
REF INPUT CHARACTERISTICS		
Voltage Range	4-130 Vrms	
Single Ended Input Impedance	100K Ohm min, 110K Ohm nom	
Frequency Range	47 Hz to 1 KHz	See Table 4, Dynamic Characteristics
SIGNAL INPUT CHARACTERISTICS		Voltage options and minimum input impedance, balanced.
Synchro	11.8VL-L / 90VL-L	
Zin Line to Line	52K Ohm / 123K Ohm	
Zin Each Line to Ground	70K Ohm / 180K Ohm	
Common Mode Range	25V max / 180V max	
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Max Voltage w/o Damage	−0.3 to 11V	
Loading	−10 μA max	Pull-up current source to +5V//5pf max CMOS transient protected.
$\overline{INH}$ (Inhibit)		Logic 0 inhibits, Logic 1 enables, Data stable within 0.3μs
$\overline{EM}$ (Enable bits 1-8) $\overline{EL}$ (Enable bits 9-16)		Logic 0 enables, data valid within 150 ns. Logic 1 high Z within 100 ns.
$\overline{S}$ (Control Transformer)		Logic 0 for Control Transformer, Logic 1 for normal tracking.
BW (Bandwidth)		Logic 1 = High BW (53 Hz); Logic 0 = Low BW (13 Hz)
Resolution Control 10 Bit 12 Bit 14 Bit 16 Bit		B (pin8) / A (pin 7) 0 / 0 0 / 1 1 / 0 1 / 1 Unused output bits are at logic 0
OUTPUTS		
Parallel Data	10, 12, 14, or 16 bits	Natural binary angle, positive logic
CB (Converter Busy)		0.4 μs to 0.7 μs positive pulse; leading edge initiates counter update.
U (Direction)		Logic 1 counts up, Logic 0 counts down
$\overline{MC}$ (Major Carry)		Logic 0 at $\overline{MC}$
$\overline{BIT}$ (Built in Test)		Logic 0 for $\overline{BIT}$ condition.
LOS (Loss of Signal)		Logic 1 for LOS (1-3μA pull-up to +5V).
Drive Capability	Logic 0: 1 TTL Load Logic 1: 10 TTL Loads High Z: 10μA/5pf max	−1.6mA at 0.4V max 0.4mA at 2.8V min
ANALOG OUTPUTS		
V (Internal DC ref)	+5.5V nom	
VEL (Velocity)		See Table 6, Velocity Characteristics
e (AC error)	50mVrms per LSB of error 25mVrms per LSB of error 12.5mVrms per LSB of error 6.3mVrms per LSB of error	10 bit mode 12 bit mode 14 bit mode 16 bit mode
Dynamic Characteristics		See Table 4, Dynamic Characteristics

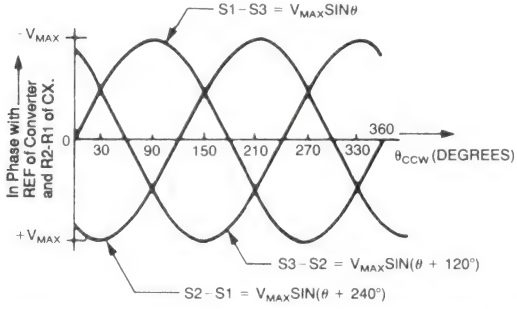
TABLE 1. SDC-19204 SPECIFICATIONS (Continued)

PARAMETER	VALUE			DESCRIPTION
POWER SUPPLY CHARACTERISTICS				
Nominal Voltage and Range	+15VDC ±5%	+5VDC ±10%	−15VDC ±5%	Note: When analog outputs are not required, ground −15V (pin 36).
Max Voltage w/o Damage	+18V	+8V	−18V	
Max Current	25mA	10mA	15mA	
TEMPERATURE RANGES				
Operating	0°C to +70°C			
Storage	−40°C to +120°C			
PHYSICAL CHARACTERISTICS				
Size	1.14 x 2.02 x 0.23 inches (28.96 x 51.3 x 5.84 mm)			40 pin TDIP
Weight	0.46 oz (13 gm)			

TECHNICAL INFORMATION

INTRODUCTION

The SDC-19204 Series are small, 40 pin TDIP synchro to digital hybrid converters. As shown in the block diagram (figure 1), the SDC-19204 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).

FIGURE 2. SYNCHRO SIGNALS

SIGNAL INPUT

In a synchro, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta + 120^\circ)\cos\omega t$ and $\sin(\theta + 240^\circ)\cos\omega t$ are internally converted to resolver format: $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Figure 2 illustrates synchro signals as a function of the angle θ.

INTERNAL DC REFERENCE VOLTAGE (V). This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference common with the direct input option. It is nominally +5.5V and is proportional to the +15VDC supply.

CONVERTER OPERATION

As shown in figure 1, the converter section of the SDC-19204 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, zero-set timing, and reference conditioner. The converter produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter.

The **control transformer** performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta, representing the resolver shaft position.
ϕ is digital angle phi, contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \blacklozenge 0$, so that ϕ will repeat the shaft position θ.

The output of the **demodulator** is an analog DC level proportional to $\sin(\theta - \phi)$. The **error processor** receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the **up/down counter**. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

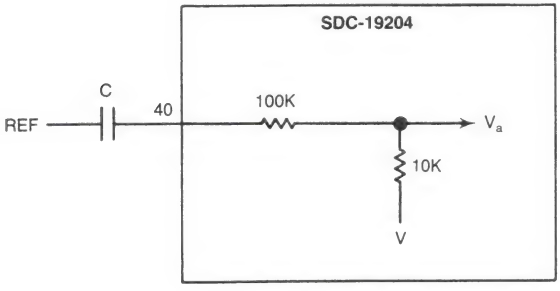
The SDC-19204 has unique **zero-set timing** circuits that cancel out all internal op-amp DC offsets. This zero-setting is done twice a reference input carrier cycle centered around the zero crossings. Each zero-setting cycle lasts for 18μs. During this time, the resolver input is disconnected and a zero input is switched in. The digital input to the control transformer is latched. The resultant DC error at the output of the demodulator is sampled and injected back in during the normal mode of operation.

The result is an effective way of simulating DC offset-free op-amps which ensure a converter whose actual dynamic and large signal performance is the same as its mathematical theoretical

performance. In a somewhat similar manner, the velocity op-amp integrator's DC offset voltage is also cancelled out with this zero-setting scheme.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It is single ended ground based with an input Z of 100K ohms min, 110K ohms nom, resistive.

MINIMIZE ERROR DUE TO QUADRATURE. In those applications where highest accuracy is needed, the REF input can be phase shifted by adding a capacitor in series with the REF input (pin 40) to add a phase lead equal to the nominal phase lead of the synchro input. To determine the capacitor's value, see figure 3.



Note:
Choose C such that the V_a to REF phase lead is equal to the synchro to REF phase lead plus 9μs.

FIGURE 3. PHASE SHIFTING THE REF INPUT

QUADRATURE VOLTAGES. In a resolver, quadrature voltages are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error = (Quadrature Voltage/F.S. signal) • tan(α)

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift.

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: α = 6°
Then: Magnitude of Error = 0.35 min $\simeq$ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier freq) • F.S. signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the resolver.
Carrier frequency is the REF in Hz.

ANALOG CONDITIONER

The Analog Conditioner section performs three functions. It converts analog ground from 5.5V to 0V, provides a gain of 2 for AC Error (e) and a gain of 2.2 for Velocity (VEL). The velocity scaling sensitivity can be increased with an external resistor. Refer to VEL PROGRAMMING section for more information.

POWER SUPPLY CONDITIONER

The power supply conditioner lowers the internal power supply voltage to the custom CMOS chip to +11V from the +15V supply. The +11V will track the +15V. Internal analog ground is one half of 11V or +5.5V, nom.

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the SDC-19204.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-19204, applying an Inhibit ($\overline{INH}$) command will lock the data in the **output transparent latch** without interfering with the continuous tracking of the converter's feedback loop. Therefore, the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 9) paragraph.

The **BIT detect** circuitry monitors the error level (D) from the demodulator and the **LOS (loss of signal) detector** detects disconnected resolver inputs.

LOGIC INPUT/OUTPUT

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 10) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 11) to a logic 0. The second byte will contain either bits 9-10 (10 bit resolution), bits 9-12 (12 bit resolution), bits 9-14 (14 bit resolution) or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 2 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EL}$ and $\overline{EM}$ are set to logic 1. Both enables are internally pulled up to +5V by −10μA max current sources.

TABLE 2. DIGITAL ANGLE OUTPUTS		
BIT	DEG/BIT	MIN/BIT
1 (MSB ALL MODES)	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.5
8	1.405	84.38
9	0.7031	42.19
10 (LSB 10 BIT MODE)	0.3516	21.09
11	0.1758	10.55
12 (LSB 12 BIT MODE)	0.0879	5.27
13	0.0439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE)	0.0055	0.33

Note: $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs.

DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 10, 12, 14, or 16 parallel data bits. All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive, 0.4 to 0.7 μs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay (shown in figure 1). Data is valid 0.2 μs after the leading edge of CB (see figure 4). The angle is determined by the sum of the bits at logic 1.

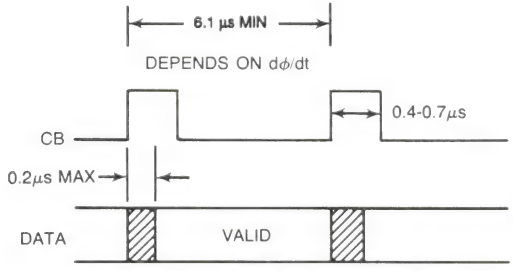


FIGURE 4. CB TIMING

INHIBIT ($\overline{INH}$, PIN 9)

When an Inhibit ($\overline{INH}$) input is applied to the SDC-19204, the Output Transparent Latch is locked, causing the output data bits to remain stable while data is being transferred (see figure 5). The output data bits are stable 0.3 μs after INH is driven to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and INH. While the counter is not being updated, CB is at logic 0 and the INH latch is transparent; when CB goes to logic 1, the INH latch is locked. If CB occurs after INH has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if INH is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and INH where the up-down counter begins to change as an INH is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{INH}$.
(2) Wait 0.3 μs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 6 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

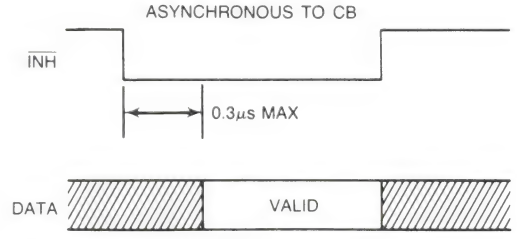


FIGURE 5. INHIBIT TIMING

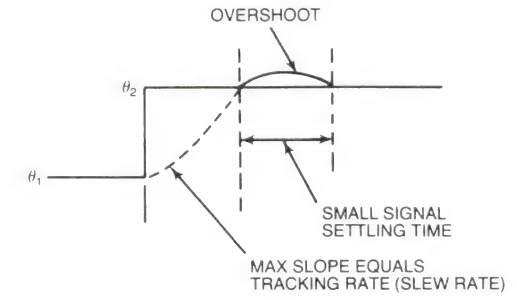


FIGURE 6. RESPONSE TO A STEP INPUT

DATA TRANSFERS

Digital output data from the SDC-19204 can be transferred to 8 bit and 16 bit bus systems. For 8 bit systems, the MSB and LSB bytes are transferred sequentially (see figures 7 and 8). For 16 bit systems, all bits are transferred at the same time (see figures 9 and 10).

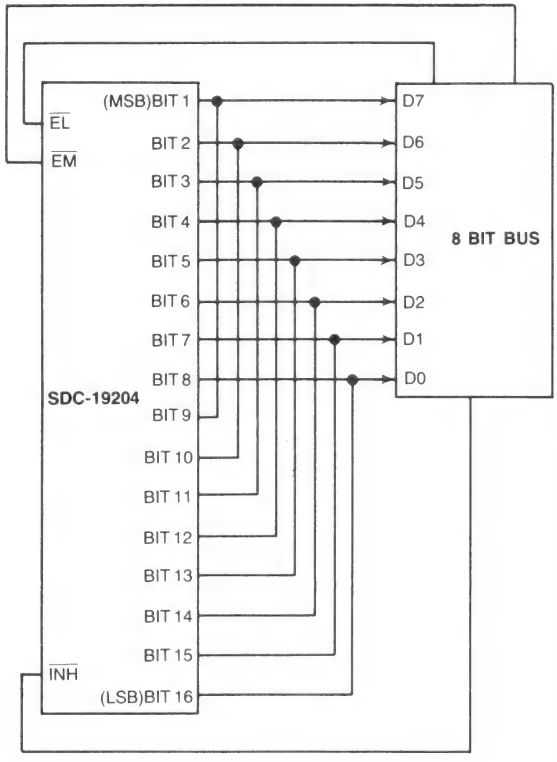


FIGURE 7. DATA TRANSFER TO 8 BIT BUS

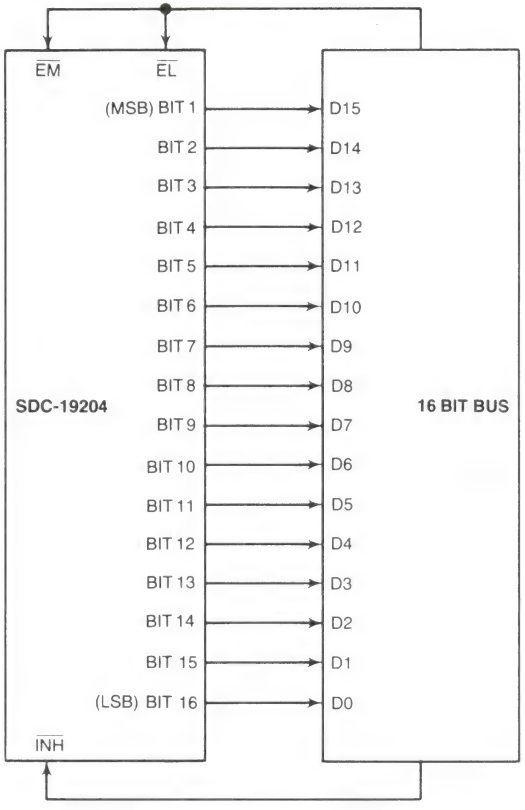


FIGURE 9. 16 BIT DATA TRANSFER

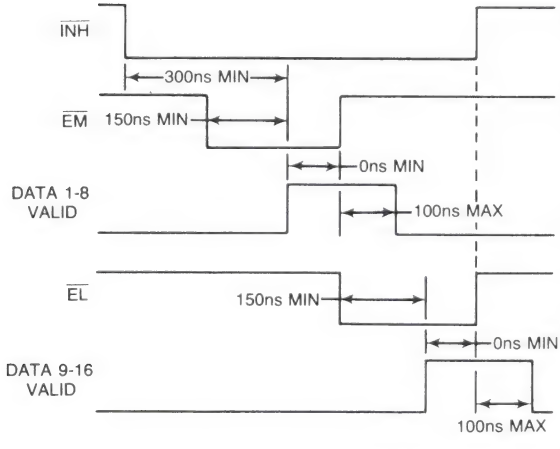


FIGURE 8. DATA TRANSFER TO 8 BIT BUS TIMING

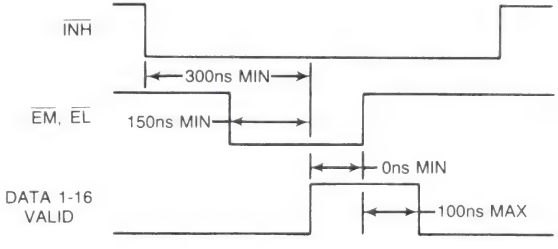


FIGURE 10. 16 BIT DATA TRANSFER TIMING

PROGRAMMABLE RESOLUTION

Resolution is controlled by two logic inputs, A and B (see table 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are transferred through the latch internally on the trailing edge of CB (see figure 11).

TABLE 3. RESOLUTION CONTROL

B (pin 8)	A (pin 7)	RESOLUTION
0	0	10 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Note: All unused digital output data bits are at logic 0.

FASTER SETTLING TIME USING BIT TO REDUCE RESOLUTION

Since the SDC-19204 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the SDC-19204 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

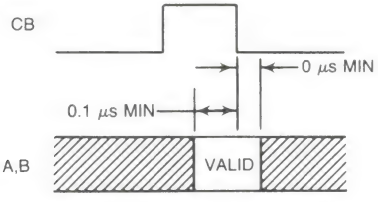


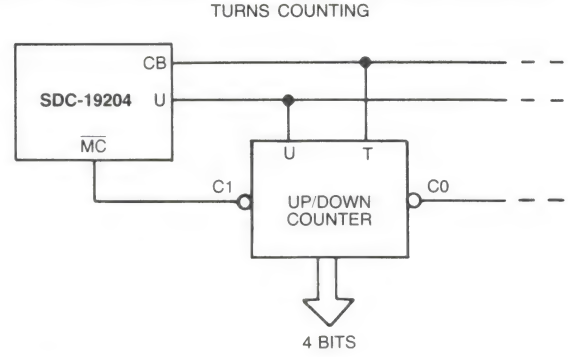
FIGURE 11. RESOLUTION CONTROL TIMING

MAJOR CARRY ($\overline{MC}$, PIN 32)

Major Carry is used with Direction Output (U) for multi-turn applications. This signal is similar to the popular MSI four bit up-down counter CO (Carry Out), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. See figure 12 for a typical interconnection.

DIRECTION OUTPUT (U, PIN 31)

Direction Output (U) is shown in figure 13. It is at logic 1 to count up and logic 0 for down. The logic level at (U) is valid at least 0.5μs before and at least 20ns after the leading edge of CB.



Notes:
(1) For the 4 bit up/down counter, use 74LS169B(TTL) or 4516 (CMOS).
(2) U = up/down line, logic 1 counts up.
(3) T = toggle line, counts on positive edge.

FIGURE 12. TURNS COUNTING CONNECTION DIAGRAM

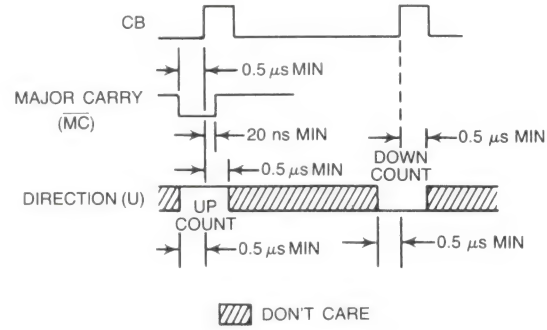


FIGURE 13. DIRECTION OUTPUT (U) TIMING

SYSTEM SELF-TEST

The SDC-19204 provides two useful logic outputs for systems self test, $\overline{BIT}$ and LOS.

BUILT-IN-TEST ($\overline{BIT}$, PIN 29)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition because the converter loop cannot maintain input-output sync or if the converter malfunctions where it cannot maintain the loop at a null. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

LOSS OF SIGNAL (LOS, PIN 28)

The Loss of Signal (LOS) output is used for system safety. The LOS output changes from logic 0 to 1 if both resolver inputs are disconnected. With disconnected resolver inputs, unpredictable converter performance occurs.

PROGRAMMABLE BANDWIDTH (BW, PIN 5)

Either low or high bandwidth can be selected by using the BW logic input. A logic 0 applied to BW selects low bandwidth (13 Hz nom), while a logic 1 selects high bandwidth (53 Hz nom). Bandwidth can be changed during converter operation.

Bandwidth and the acceleration constant (K_a) can be determined from the following formulas:

$$\text{Closed Loop Bandwidth (Hz)} = \sqrt{2}\,A/\pi$$

$$K_a = A^2$$

See Dynamic Characteristics Table 4 and figures 17 to 19 for values.

TABLE 4. DYNAMIC CHARACTERISTICS

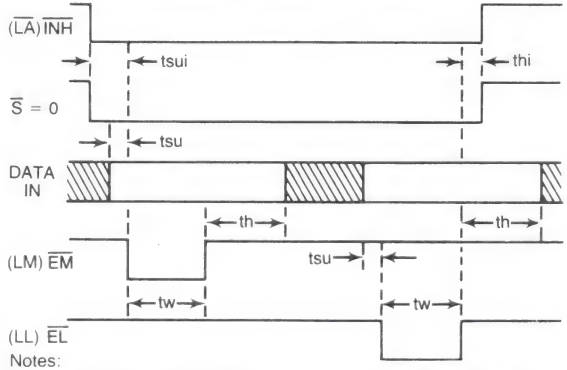
PARAMETER	UNITS	BANDWIDTH							
		HIGH				LOW			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	KHz	.36-1	*	*	*	.047-1	*	*	*
Tracking Rate	RPS†	160	40	10	2.5	40	10	2.5	0.62
Bandwidth, CL	Hz	53	*	*	*	13	*	*	*
K_a	1/sec^2	14.4K	*	*	*	3.6K	*	*	*
A1**	1/sec	0.4	*	*	*	0.1	*	*	*
A2**	1/sec	36K	*	*	*	9K	*	*	*
A**	1/sec	120	*	*	*	30	*	*	*
B**	1/sec	60	*	*	*	15	*	*	*
acc-1 LSB lag	°/sec^2	17K	4.2K	1.1K	260	1.1K	260	66	17
Settling time	msec	110	110	200	500	550	600	750	1100

†RPS minimum
*Same as value to left
**See figure 17 for definitions of A1, A2, A, and B.

CONTROL TRANSFORMER MODE ($\overline{S}$, PIN 6)

The converter will function as a Control Transformer (CT) by placing $\overline{S}$ (pin 6) to logic 0. In the CT mode, the digital inputs are double buffered, $\overline{EM}$ is redefined as LM, $\overline{EL}$ is redefined as LL and $\overline{INH}$ becomes LA (see figures 15 and 20). Figure 14 shows CT mode timing for a two byte transfer.

The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the resolver input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.



Notes:
(1) tw = 100 ns min (pulse width)
th = 50 ns min (hold time)
thui = 0 ns min (hold time inhibit)
tsu = 0 ns min (setup time)
tsui = 300 ns min (setup inhibit)
(2) When $\overline{S}$ is low:
(LM) $\overline{EM}$ is latch control for MSB byte,
(LL) $\overline{EL}$ is latch control for LSB byte,
1 – data held in latch,
0 – latch is transparent.
(3) (LA) $\overline{INH}$ is latch control for CT latch:
1 – latch is transparent,
0 – data held in latch.

FIGURE 14. CT MODE TIMING – TWO BYTE TRANSFER, DOUBLE BUFFERED

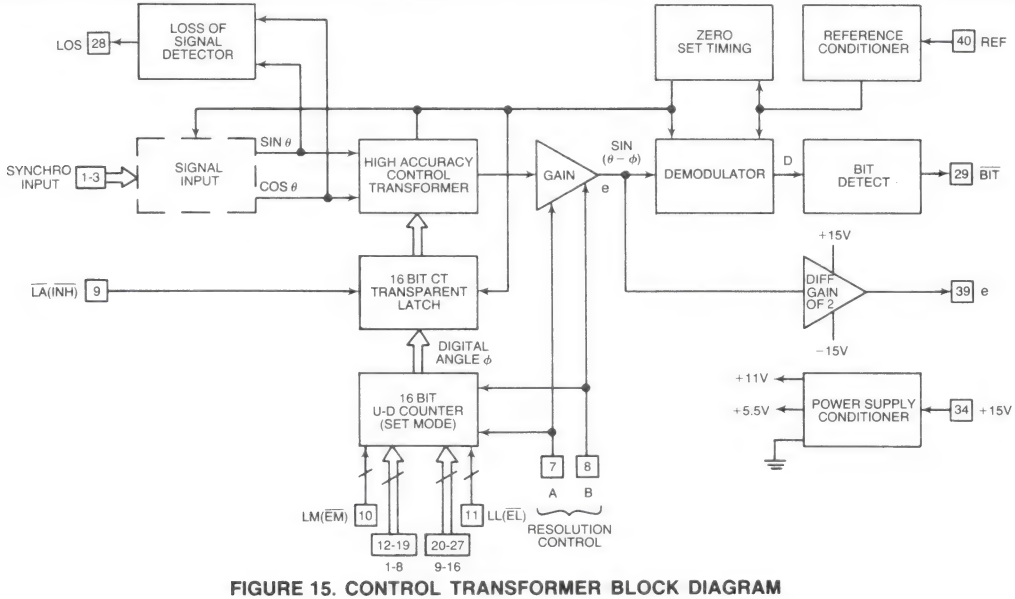


FIGURE 15. CONTROL TRANSFORMER BLOCK DIAGRAM

ANALOG OUTPUTS

The analog outputs are AC error (e) and velocity (VEL). If the analog outputs are not required, ground −15V (pin 36).

AC ERROR (e, PIN 39)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the resolver input angle θ and the digital input angle ϕ, $(\theta - \phi)$, with a scaling of:

50mVrms/LSB (10 bit mode)
25mVrms/LSB (12 bit mode)
12.5mVrms/LSB (14 bit mode)
6.3mVrms/LSB (16 bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10V peak min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level.

VELOCITY (VEL, PIN 38)

The velocity output (VEL, pin 38) is a DC voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The maximum VEL output can swing ±10V min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in table 5.

The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

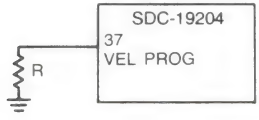
VELOCITY PROGRAMMING (VEL PROG, PIN 37)

The velocity output scale factor can be increased by connecting an external resistor (R) from VEL PROG, pin 37 to ground. By scaling up the output, the noise and offset will increase proportionally. The value of R can be determined by the following formula:

$$R = \frac{10 \times B/A}{1 - B/A}$$

Where:

R = external resistor in K Ohms
A = specified voltage scaling (RPS/VOLT)
B = desired voltage scaling (RPS/VOLT)



To determine A, refer to Table 6, Voltage Scaling.

TABLE 5. VELOCITY OUTPUT CHARACTERISTICS

PARAMETER	UNIT	SDC-19204/SDC-19206	
		TYP	MAX
Polarity		(positive for increasing angle)	
Voltage scaling	RPS/V	See Voltage Scaling Table 6	
Scale Factor	%	5	10
Scale Factor TC	PPM/°C	100	200
Reversal Error	%	1	2
Linearity	% output	1	2
Zero Offset	mV	15	40
Zero Offset TC	µV/°C	25	50
Load	KOhms	–	3
Output Voltage	V	±13	±10 min

TABLE 6. VELOCITY OUTPUT VOLTAGE SCALING (RPS/VOLT)

BW	10 BIT	12 BIT	14 BIT	16 BIT
HIGH	16	4	1	0.25
LOW	4	1	0.25	0.062

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-19204 superior dynamic performance as listed in table 1.

VELOCITY RESPONSE

A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. The VEL filter is shown in figure 16.

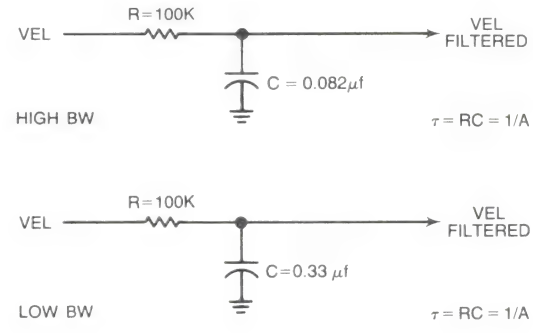
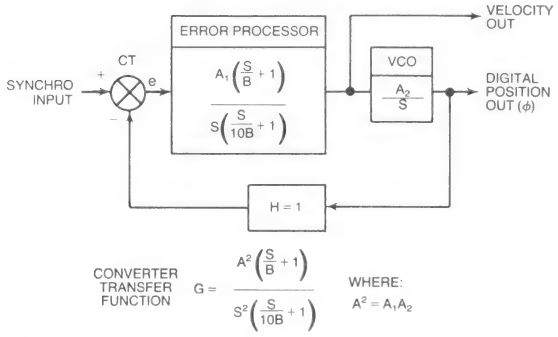


FIGURE 16. VEL OUTPUT FILTER

TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 17) and open and closed loop Bode plots (figures 18 and 19). Table 4 lists the parameters relating to the SDC-19204's dynamic characteristics for different resolution and bandwidth modes.



Note: See table 4 for values of A1, A2, and B.

FIGURE 17. TRANSFER FUNCTION BLOCK DIAGRAM

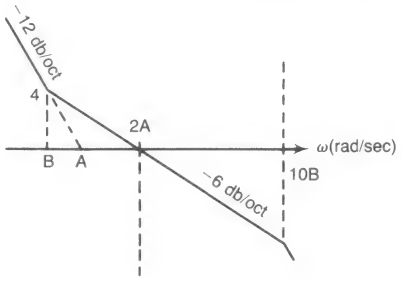


FIGURE 18. OPEN LOOP BODE PLOT

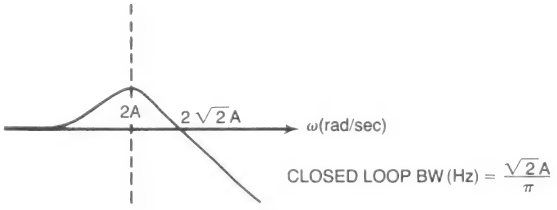


FIGURE 19. CLOSED LOOP BODE PLOT

ACCURACY AND RESOLUTION

Table 7 lists the total accuracy including quantization for the various resolution and accuracy grades.

TABLE 7. ACCURACY/RESOLUTION

SDC-1920X SERIES MODEL NO.	ACCURACY	10 BIT	12 BIT	14 BIT	16 BIT
SDC-1920X-304	2′ + 1 LSB	23.1	7.3	3.3	2.3
SDC-1920X-303	3′ + 1 LSB	24.1	8.3	4.3	3.3
SDC-1920X-302	4′ + 1 LSB	25.1	9.3	5.3	4.3
SDC-1920X-301	8′ + 1 LSB	29.1	13.3	9.3	8.3

SDC-19204 APPLICATIONS

USING THE SDC-19204 IN THE CT MODE

The CT mode can be applied in servo systems, as shown in figure 20. In this application, changes in position are commanded by the computer through signals fed to the CT. The CT then drives the motors through DC power amplifiers.

MULTI-TURN APPLICATIONS – USE OF MAJOR CARRY (MC, PIN 32)

Refer to Major Carry paragraph for details.

USING THE SDC-19204 AS AN S/D WITH VEL TO STABILIZE POSITION LOOP

Figure 21 illustrates a typical use of a SDC-19204 connected as an S/D using the VEL output to stabilize the position loop.

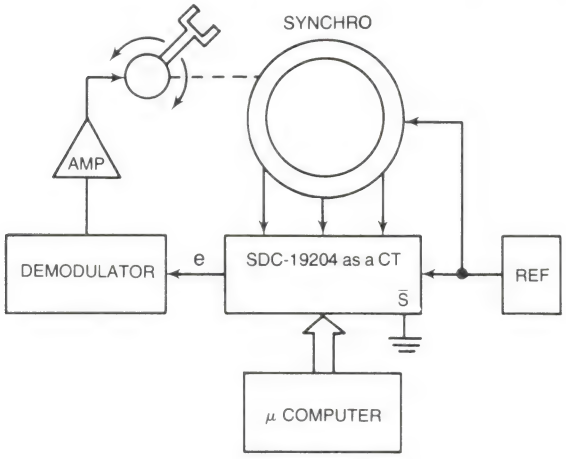


FIGURE 20. CT MODE APPLICATION

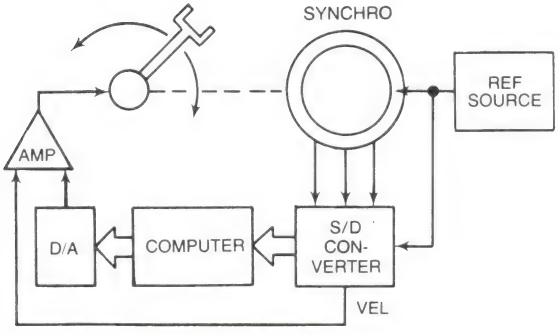


FIGURE 21. S/D WITH VEL TO STABILIZE POSITION

INTERFACING THE SDC-19204 WITH AN IBM PC/XT/AT®

The SDC-19204 can be connected to an IBM PC/XT/AT through the IBM PC Bus located at address HEX 300 through 303. This location is reserved by the PC for prototype cards. Figure 23 illustrates the connection to the IBM PC Bus; figure 22 illustrates the timing considerations for the interface.

SDC-19204 TO IBM PC/XT/AT THEORY OF OPERATION

1. The port address where the SDC-19204 is located is hard wired with jumpers into the 74LS688 address decoder. This address is HEX 300 through 303 and is reserved for prototype cards.

2. Address line A1 selects the upper or lower 8 bits of the SDC-19204 to be placed on the Bus. When A1 is high, bits 1-8 are selected.

3. Address line A0 sets and resets the SDC-19204 INHIBIT line. When A0 is low, the INHIBIT command ($\overline{\text{INH}}$) is invoked.

4. To read the output of the SDC-19204, perform the following:

   a. Send address HEX 302 to INHIBIT the SDC-19204 (hold data stable) and place bits 1-8 on the Bus. Read and store data on D0 to D7.

   b. Send address 300 HEX to keep the SDC-19204 in the INHIBIT mode and place bits 9-14 on the Bus. Read and store data on D0 to D7.

   c. Read address 301 HEX or 303 HEX to release the SDC-19204 from the INHIBIT mode and prepare for the next measurement. No valid data will be on the bus during this command.

5. Since the output data is not valid until 0.5μs after the INHIBIT command is invoked, the I/O READY line is held low for this period of time. When I/O READY returns to the high level, the data on the bus reads on the next negative clock edge.

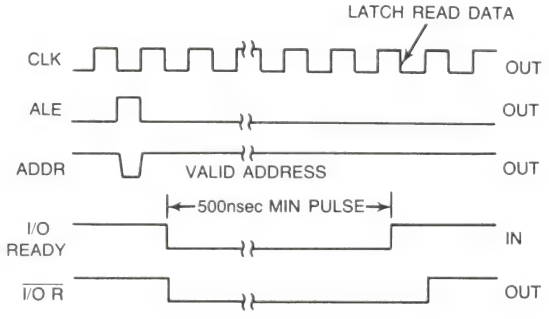


FIGURE 22. PC APPLICATION – I/O READ CYCLE TIMING

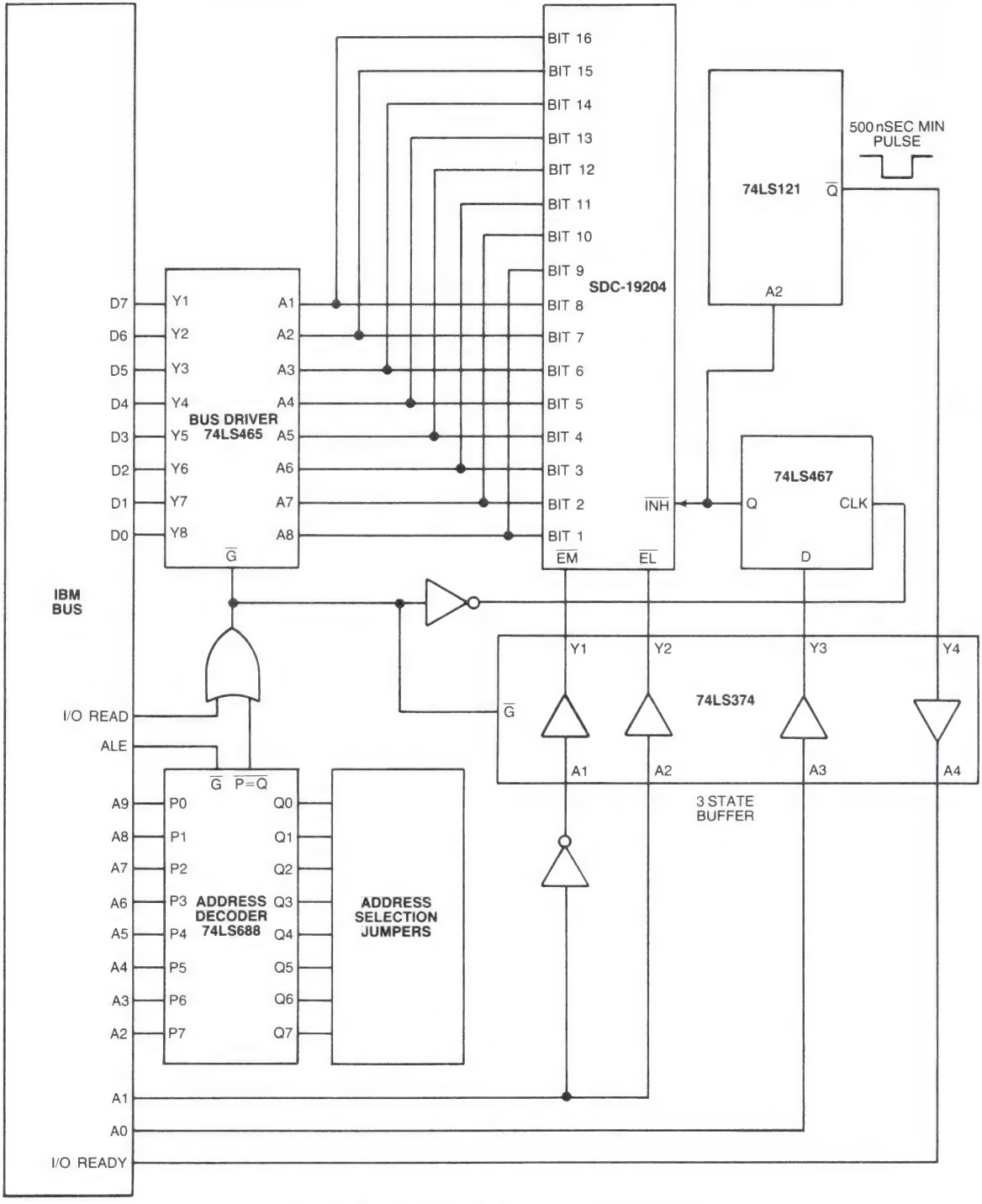


FIGURE 23. SDC-19204 TO PC CONNECTION DIAGRAM

TABLE 8. SDC-19204 PIN FUNCTIONS

PIN NO.	TITLE	I/O	FUNCTION
1	S1	I	Synchro Input.
2	S2	I	Synchro Input.
3	S3	I	Synchro Input.
4	NC	I	No connection
5	BW	I	Bandwidth. Logic 1 for high BW (530 Hz); logic 0 for low BW (130 Hz).
6	$\overline{S}$	I	Control Transformer Set. Logic 1 for normal tracking; logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input, and for presetting the converter to a specific angle to reduce the step response time.
7 8	A B	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bit, depending on logic level. B A Resolution 0 0 10 BIT 0 1 12 BIT 1 0 14 BIT 1 1 16 BIT
9	$\overline{INH}$	I	Inhibit. Logic 0 prevents digital output bits from changing.
10	$\overline{EM}$	I	Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits.
11	$\overline{EL}$	I	Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits.
12	1	O	Digital Output Bit 1 (MSB all modes)
13	2	O	Digital Output Bit 2
14	3	O	Digital Output Bit 3
15	4	O	Digital Output Bit 4
16	5	O	Digital Output Bit 5
17	6	O	Digital Output Bit 6
18	7	O	Digital Output Bit 7
19	8	O	Digital Output Bit 8
20	9	O	Digital Output Bit 9
21	10	O	Digital Output Bit 10 (LSB-10 BIT MODE)
22	11	O	Digital Output Bit 11
23	12	O	Digital Output Bit 12 (LSB-12 BIT MODE)
24	13	O	Digital Output Bit 13
25	14	O	Digital Output Bit 14 (LSB-14 BIT MODE)
26	15	O	Digital Output Bit 15
27	16	O	Digital Output Bit 16 (LSB-16 BIT MODE)
28	LOS	O	Loss of signal. Used for system safety, the LOS output changes from logic 0 to 1 if both resolver inputs are disconnected.
29	$\overline{BIT}$	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65 bits, approx. Also logic 0 for an over-velocity condition.
30	CB	O	Converter Busy. Indicates digital output update.
31	U	O	Direction. Logic 1 to count up; logic 0 to count down.
32	$\overline{MC}$	O	Major Carry. Used for turns counting applications; normally high, goes low for all 1's when counting up or all 0's when counting down.
33	+5V	I	Supply Voltage
34	+15V	I	Supply Voltage
35	GND	–	Ground
36	−15V	I	Supply Voltage.
37	VEL PROG	I	Velocity Programming. Increases output scale factor with external resistor (R) from VEL PROG, pin 37 to ground.
38	VEL	O	Velocity. DC voltage proportional to angular velocity
39	e	O	AC Error. Used in CT mode; e is proportional to the difference between the resolver input angle θ and the digital output angle ϕ ($\theta - \phi$).
40	REF	I	AC Reference Input. Used to drive internal demodulator.

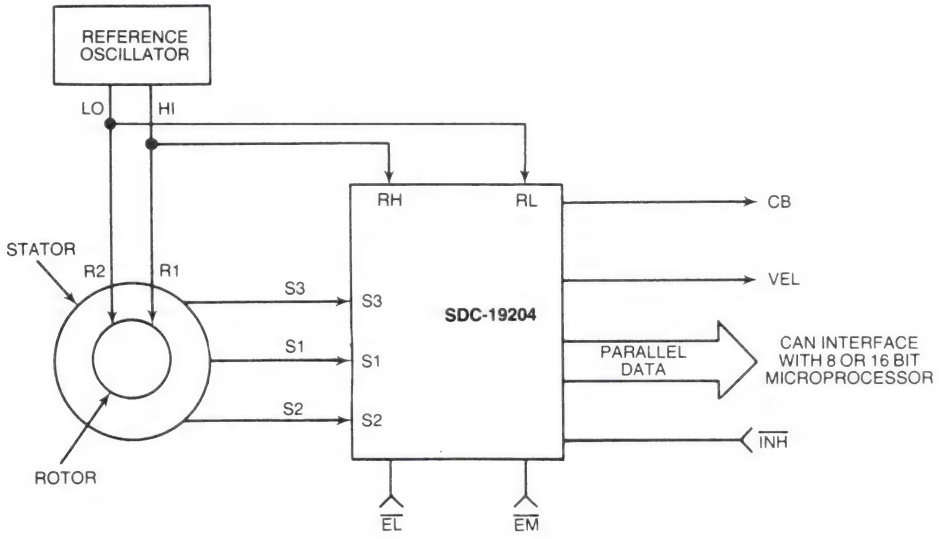


FIGURE 24. SYNCHRO CONNECTION

SOURCES OF SOCKETS FOR THE SDC-19204

The following companies are sources of sockets for use with the SDC-19204 Series. Consult them for more information.

Aries Electronics, Inc.
P.O. Box 130
Frenchtown, NJ 08825
Tel: 1-908-996-6841

Single In-Line Socket
Strip-Line Socket
Part No. 20-05511-11

Circuit Assembly Corp.
18 Thomas Street
Irvine, CA 92718
Tel: 714-855-7887

Part No. CA-20-STL-XX XX-X

CONNECTING THE SDC-19204

The SDC-19204 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

Do not use vapor phase soldering as this product contains SN60 or SN62 solder which melts at 180°C (356°F).

Since the SDC-19204 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

Dimensions are inches (mm).

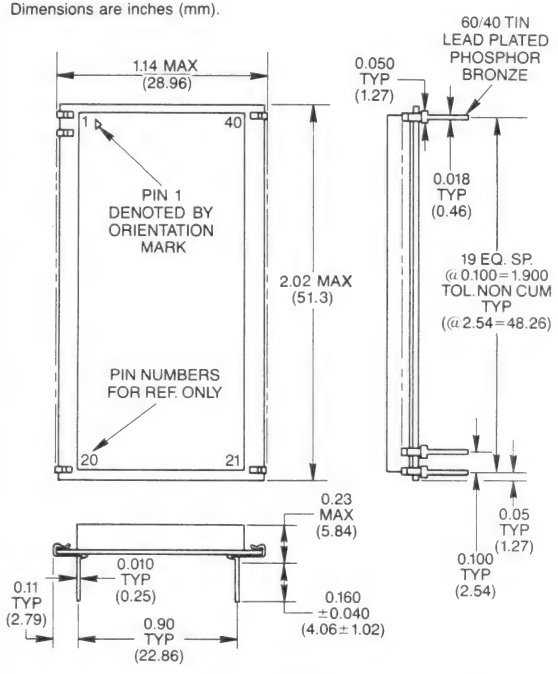
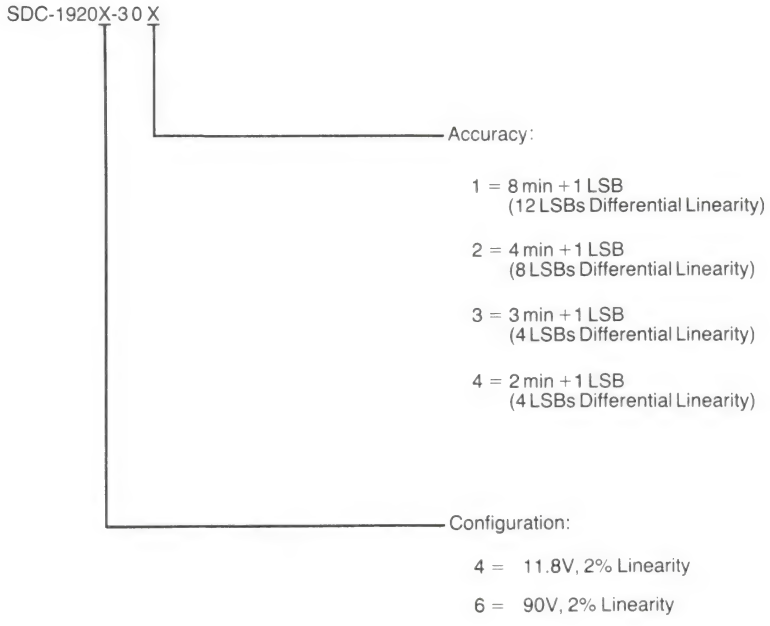


FIGURE 25. SDC-19204 MECHANICAL OUTLINE

ORDERING INFORMATION


SDC-1920X-30X
Accuracy:
1 = 8 min + 1 LSB
(12 LSBs Differential Linearity)
2 = 4 min + 1 LSB
(8 LSBs Differential Linearity)
3 = 3 min + 1 LSB
(4 LSBs Differential Linearity)
4 = 2 min + 1 LSB
(4 LSBs Differential Linearity)
Configuration:
4 = 11.8V, 2% Linearity
6 = 90V, 2% Linearity

Note:
Differential Linearity is x LSB in the 16th bit.

SECTION F
DIGITAL TO SYNCHRO AND RESOLVER (D/S, D/R) CONVERTERS

PRODUCT SUMMARY TABLE

MODEL	RESOLUTION	ACCURACY	OUTPUT DRIVE	PACKAGE	DESCRIPTION/FEATURES	PAGE
DRC-10520	16 Bit	to ± 1'	2 VA	32 Pin TDIP 1.14 x 1.74 x 0.18"	High power D/R converter. 8-bit, 2-byte, double buffered transparent input latch. BIT output and short circuit output protection. Ac or dc power amps. Replaces DRC-10500. Requires standard ±15V supply.	F-4
DRC-11522	16 Bit	± 1'	2mA-rms	36 Pin TDIP Hybrid 1.9 x 0.78 x 0.21"	2 channel D/R. Each channel is independent from the other with the exception of the 16 digital lines. Pin programmable gain control.	F-8
DSC-544	14 Bit	±4'	4.5 VA	2.6 x 3.1 x 0.8" Module	Powered from reference, metal heat sink, all internal transformers. Short circuit proof and transient protected. Thermal cutoff. Output is transformer isolated 90V synchro at 400Hz and 60Hz.	F-12
DSC-644	14 Bit	±4'	1.5 VA	2.6 x 3.1 x 0.5" Module	Low profile industry standard pin-out. Metal heat sink, current limited, and transient protected. Internal 400 Hz transformers. Low scale factor variation. CMOS and TTL digital input compatibility.	F-16
DSC-10510	16 Bit	to ±1'	7VA	40 Pin TDIP 2.0 x 1.1 x 0.2"	High power D/S converter. Microprocessor compatible. BIT output and short circuit protected. Ac or dc power supplies. 5VA drive available.	F-22
DSC-11520	16 Bit	to ±1'	2mA	36 Pin DDIP 1.9 x 0.78 x 0.21"	16-bit programmable D/S and D/R converter. 8-bit, 2-byte double buffered transparent latches. Output short circuit protection. 0.05% scale factor variation. Replaces HDSC-14.	F-25
* **DSC-11524**	16 Bit	to ±1'	15mA	36 Pin DDIP 1.9 x 0.78 x 0.21"	16-bit programmable D/S and D/R converter; 11.8V_{L-L} synchro or resolver; and 6.8V sin/cos. 90V synchro with optional external transformers.	F-28
TD-100	12 Bit	±10'	25 VA	5.4 x 5.3 x 0.7" PC Card	High power torque receiver synchro driver. Options to 115 VA with external booster amp. Short circuit protected, thermal cutout, sequenced turn on, input registers.	F-31
TD-101	12 Bit	±10'	—	5.4 x 5.3 x 0.7" PC Card	Same as above but designed for remote power stage.	

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

* New Product

BACKGROUND INFORMATION

INTRODUCTION

DDC's Digital-to-Synchro and Digital-to-Resolver converters are intended to satisfy a broad category of interface applications where digital angle data with binary bit weights must be converted accurately to either three-wire synchro or four-wire resolver signals.

From a systems engineer's standpoint, outstanding performance features have been incorporated into these units. They are designed for printed circuit board mounting by hand soldering and flow soldering techniques. Each unit is fully trimmed and tested before leaving the factory. DDC builds hundreds of converters each month, making shipments from stock a common occurence.

THEORY OF OPERATION

The input to a Digital-to-Synchro (D/S) or Digital-to-Resolver (D/R) converter is a set of binary weighted "logic levels", (ones & zeros), representing the shaft angle, θ, to some number of bits of resolution (Figure 1). The first two most significant bits (MSBs) of any pure binary coded word are the quadrant designating bits (the first three, by similar reasoning, are the octant designating bits). The remaining bits of the digital word determine the angle precisely by adding some value between 0 degrees and 90 degrees. Converting these bits into analog levels corresponding to the sin and cos of that angle (between 0 degrees and 90 degrees) will enable us to use the quadrant-designating bits to establish the appropriate polarity for these analog levels, in accordance with the following identities:

$$\begin{aligned}
\text{Sin } \theta \text{ (2nd quad.)} &= + \cos(\theta\text{-}90^\circ) \\
\text{Sin } \theta \text{ (3rd quad.)} &= - \sin(\theta\text{-}180^\circ) \\
\text{Sin } \theta \text{ (4th quad.)} &= - \cos(\theta\text{-}270^\circ) \\
\text{Cos } \theta \text{ (2nd quad.)} &= - \sin(\theta\text{-}90^\circ) \\
\text{Cos } \theta \text{ (3rd quad.)} &= - \cos(\theta\text{-}180^\circ) \\
\text{Cos } \theta \text{ (4th quad.)} &= + \sin(\theta\text{-}270^\circ)
\end{aligned}$$

Quadrant	1st 2 MSBs	Polarity Sin θ	Polarity Cos θ
4	11	Neg	Pos
3	10	Neg	Neg
2	01	Pos	Neg
1	00	Pos	Pos

By routing the first two MSBs to a set of polarity/signal selection logic circuits, we may reduce our problem to trigonometric D/A conversion in only one quadrant (see Figure 1). The first two MSBs are diverted to a quadrant selector circuit and the remaining bits are used to program 0 degrees to 90 degrees sin and cos function generators. These generators may be described as non-linear, bipolar, multiplying D/A converters in which the reference input signal is the reference (E ref), and the transfer function is either EA = E ref Sin θ or EB = E ref cos θ, where θ is the angle represented by the digital input.

The reference voltage supplied to the D/S converter is transformer or resistor isolated and converted (with the use of a centertap) into two equal reference frequency sin waves of

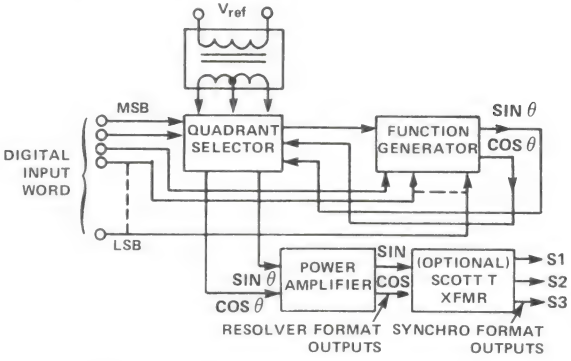


FIGURE 1 BASIC DIGITAL-TO-SYNCHRO RESOLVER CONVERTER

opposite phase. After quadrant selection, they are fed to the inputs of the function generators. The outputs of the function generators are now accurate resolver-format signals. For resolver to synchro conversion, the use of a "reversed" Scott-T transformer is required in order to convert from 4-wire resolver to 3-wire synchro. The outputs produced by these converters are low-energy, low-voltage signals and may require the use of an external high power buffer amplifier (DDC's HPB or SBA series of amplifiers).

The conventions for output phasing and for RH, RL for each of DDC's synchro or resolver to digital converters and torque receivers are described individually for each product. If the output of an S/D or R/D converter is used to provide input for a D/S or D/R converter, the relative phasing of RH, RL on both units should be compared.

APPLICATIONS

In all of DDC's D/S or D/R converters, careful attention must be given to making the proper electrical connections. Reversal or misapplication of power supplies can result in damage to the converter. When preparing the P.C. artwork, keep all AC signals apart from both the digital and power leads. This will make it less likely that meter or scope probes will induce potentially destructive shorts.

Care must be taken when handling units which have CMOS inputs since they are extremely sensitive to static. Avoid handling the units by their leads, keeping them plugged into the conductive foam supplied with the unit until they are ready for use in a circuit.

The synchro or resolver system reference must be connected to the REF HI and REF LO terminals. It is very important that extreme caution be used in handling the reference since sometimes it is a high AC voltage, usually from a low source impedance. If it makes contact with either a digital input or a power terminal, damage will result. The output AC signals are derived from (and proportional to) the applied reference. Any distortion present on the reference will appear in the output signals. The input power to the reference terminals is a negligible load for almost any reference source. The typical load for a D/S is a CT (control transformer) which is a highly inductive

load with a reasonable Q. It is possible to "tune" this load by placing three capacitors of the proper value across the synchro output in a delta configuration (Figure 2). The same holds true for the resolver output, except that only two capacitors are

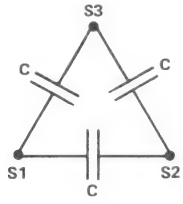


FIGURE 2 DELTA CONFIGURATION FOR TUNING LOADS

required. The formula for determining the size of the capacitor is given in Figure 3. Note that good grade capacitors are necessary and that they must be able to withstand the full AC output voltage. By tuning the load, you can raise the effective impedance and thereby drive many more loads simultaneously.

Do not exceed the converter's output load ratings since it will cause waveform distortion leading to inaccuracies. A false null may occur 180 degrees away from the true null due to the fact that the converter can alter the angle so fast that the servo (load) cannot respond. To avoid this problem, the software which determines how the digital data is generated should never allow 180 degrees changes to take place in one step.

Transients may occur when the data angle changes. This usually does not cause any error since the low bandwidth of the synchro filters out these transients. If your application includes a high speed S/D, be sure that you give the D/S enough time to settle before reading the output angle. To test these converters you will need the equipment shown in Figure 4. We suggest that DDC's new synchro angle indicator (the SR-103) be used to test the D/S. As an alternative, use the bit switches to program any angle, and adjust the synchro bridge for a null as read by the phase angle voltmeter. The error is equal to the angle read by the bridge subtracted from the theoretical angle. If it would seem beneficial to avoid the high cost of test equipment, we invite you to use DDC's facilities for "source inspection" at no extra charge.

$$C = \frac{X'_{LSO}}{6\pi f\,[(R'_{so})^2 + (X'_{LSO})^2]}$$

Where:

C = Tuning capacitor in farads in delta connection.

X'_{LSO} = Reactive component of impedance of one stator winding leg with rotor open circuit.

f = Frequency in Hz

R'_{so} = Resistive component of impedance of one stator winding leg with rotor open circuit.

Note: $Z'_{so} = \frac{2}{3}(Z_{so})$

Z_{so} = Stator winding impedance with rotor open circuit.

Z'_{so} = per leg winding impedance with rotor open circuit.

FIGURE 3 CAPACITOR FOR TUNING SYNCHRO STATOR WINDINGS

SOME COMMON CONTROL TRANSFORMERS AND THEIR LOAD IMPEDANCES

Military Type Number	Size	Z_{so}	Use DDC Converter Number	Transformer
26 V 08CT4c	08	100+j490	DSC-644-L	
26 V 11CT4d	11	21+j132	DSC-644-L	
11CT4e	11	838+j4955	DSC-644-H	
15CT4c	15	1600+j9300	DSC-644-H	
15CT6b	15	1170+j6780	DSC-644-6	60 Hz
18CT4c	18	1420+j3260	DSC-644-H	
18CT6b	18	1680+j5040	DSC-644-6	60 Hz
23CT4a	23	1460+j11050	DSC-644-H	
23CT6a	23	1250+j3980	DSC-644-6	60 Hz

Please obtain complete data from the synchro manufacturer or other sources to determine the impedances. There are many variations in synchros and you should not assume that a 15 CT 4 and a 15 CT 4d are the same. They are not.

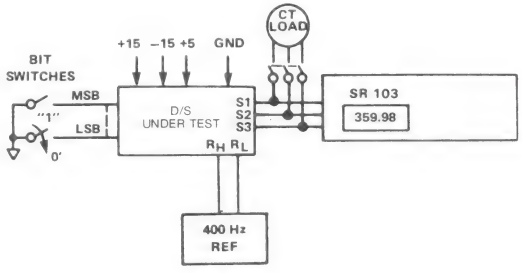
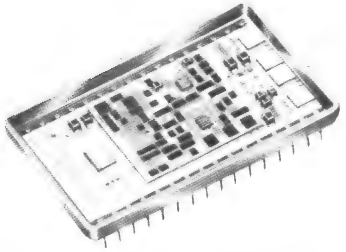


FIGURE 4 D/S TEST CONFIGURATION

See page N-19 for a list of Application Notes available from DDC.

DRC-10520©

HIGH POWER 16 BIT HYBRID D/R CONVERTER



FEATURES

- *HYBRID CONSTRUCTION*
- *2 VA DRIVE CAPABILITY*
- *8 BIT/2 BYTE DOUBLE BUFFERED TRANSPARENT INPUT LATCH*
- *RESOLUTION: 16 BITS ACCURACY: TO 1 MINUTE*
- *POWER AMPLIFIER USES AC REFERENCE OR DC SUPPLIES*
- *BIT OUTPUT*

DESCRIPTION

The DRC-10520 is a 16 bit, 32 pin triple DIP D/R Converter with 2 VA drive capability. Featuring a power amplifier that may be driven by a standard ±15V DC power supply, or by the reference source when used with the optional power transformer DDC/PN 29306, the DRC-10520 provides compatibility with microprocessors through its 8 bit 2 byte transparent input latch. Data input is natural binary angle in TTL compatible parallel positive logic format. The DRC-10520 is comprised of a high accuracy D/R converter and a dual power amplifier stage and has high accuracy and low scale factor variation. In addition, a standard BIT circuit provides a digital overcurrent signal output. A logic "0" is used for detection of overcurrent condition in the sine or cosine outputs. Reference inputs are scalable with external resistors. Loss of reference signal will not damage the converter.

APPLICATION

The DRC-10520 can be used where digitized shaft angle data must be converted to an analog format for driving control transformers. With its built-in input latches, the DRC-10520 is especially compatible with a microprocessor based system including flight simulators, flight instrumentation, fire control systems, radar and navigation systems, and air data computers.

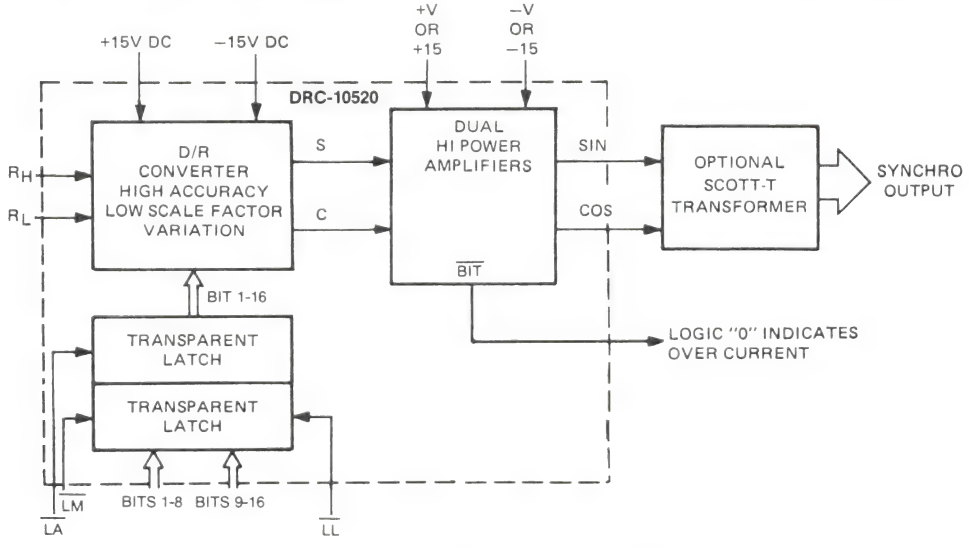


FIGURE 1. DRC-10520 BLOCK DIAGRAM

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SPECIFICATIONS
Apply over temperature range, power supply ranges, reference voltage and frequency range and 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 bits
ACCURACY AND DYNAMICS	
Output Accuracy	
Without Scott-T	±1, ±2 or ±4 minutes
With Scott-T P/N29305	±10 minutes (1.5 VA min for CT load) ±16 minutes (2VA min for CT load)
Differential Linearity	±1 LSB
Output Settling Time	Less than 40μsec for any digital input step change
DIGITAL INPUT	
Logic Type	Natural binary angle, parallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected.
Logic Voltage level	Logic 0 = 0 to +1.25V Logic 1 = 2V to 5V
Load Current	20μa max to GND (bit 1-16) 20μa max to V_L ($\overline{LL}$, $\overline{LM}$, $\overline{LA}$)
Timing	See Timing Diagram (Fig. 2).
REFERENCE INPUT	
Type	Differential 3.4V rms
Voltage	Higher voltages are scaled by adding series resistors
Frequency	DC to 1kHz
Input Impedance	
Single Ended	13kΩ ±0.5%
Differential	26kΩ ±0.5%
ANALOG OUTPUT	
Type	Resolver
Output Current	300mA rms, min (2VA, min)
Max Output Voltage (tracks reference input voltage)	6.8V rms max line-to-line ±1%
Scale Factor Variation	Simultaneous amplitude variation in all output lines as function of digital angle is ±0.1% max.
DC Offset (each line to ground)	±15mV max varies with input angle.
Protection	Output is protected from overcurrent, short circuits and voltage feedback transients.
POWER SUPPLIES	+15V / -15V / +V / -V
Voltage	
Voltage Limits	±5% / ±5% / 20V peak max 3V above output voltage min.
Max Voltage Without Damage	+18V / -18V / +25V / -25V
Current	20 mA max / 20 mA max / load dependent
Peak Current At Power Turn On or Short Circuit (when using Transformer)	700mA max
TEMPERATURE RANGES	
Operating (−3xx)	0°C to +70°C case
(−1xx)	−55°C to +125°C case
Storage	−55°C to +135°C
PHYSICAL CHARACTERISTICS	
Package Type	32 pin triple DIP
Size	1.14 x 1.74 x 0.18 inch (29 x 44 x 4.4mm)
Weight	1.15 oz (33g)

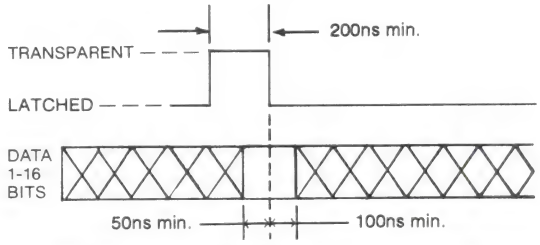

FIGURE 2. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

The DRC-10520 is a digital to resolver (D/R) converter which has an inherently high accuracy and low scale factor variation. The circuit is based on an algorithm whose theoretical math error is only ±3.5 arc-seconds and whose theoretical scale factor variation with angle is less than ±0.015%. Therefore accuracy and scale factor are limited only by the physical components, not by the algorithm.

The digital inputs are CMOS double buffered transparent latches (Figure 1). Angle is determined by adding bits in the logic 1 state.

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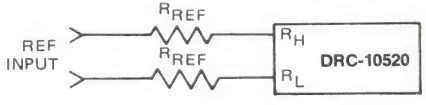
REFERENCE LEVEL ADJUSTMENT

The input is specified for operation at a reference level of 3.4V rms; however, reference levels other than 3.4V rms may be scaled by calculating the value of the scaling resistor with the following equation:

$$R_{REF} = \frac{(V_{REF} - 3.4)}{3.4} \times 13k$$

eg., if V_{REF} = 26V rms, then $R_{REF} = \frac{(26-3.4)}{3.4} \times 13k$

$= 86.4k\Omega$



The output is 6.8V rms line-to-line resolver format signal which may be converted into a synchro format of 11.8V line-to-line with the companion Scott-T transformer module available as DDC P/N29305.

DRIVING THE POWER AMPLIFIER WITH THE REFERENCE

The high power amplifier stage can be driven by a standard ±15V DC supply or with a high efficiency pulsating power supply derived from the reference voltage source. A companion power transformer DDC P/N29306, designed to implement the pulsating power source for the DRC-10520 is also available (Figure 3). The DRC-10520 will not be damaged by sequencing order in the ±15V, V_L supplies or the reference input.

OUTPUT PROTECTION AND BIT

The output is protected from overcurrent, short circuits and voltage feedback transients. The BIT circuit detects overcurrent conditions in the sine or cosine resolver output. A logic "0" is used for overcurrent detection. Normal operation is logic "1". The BIT line is normally at logic "1". An overload or short circuit will cause the BIT line to drop after 1 sec when the output current exceeds a peak level of approximately 450mA.

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

$$\sin = (R_H - R_L)\, A_O\, (1 + A\,(\theta))\, \sin\theta$$

$$\cos = (R_H - R_L)\, A_O\, (1 + A\,(\theta))\, \cos\theta$$

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The amplitude factor A_O is 2 for 6.8V rms L-L output. The maximum variation in A_O from all causes is 0.3%. The term $A(\theta)$ represents the variation of the amplitude with the digital input angle. $A\,(\theta)$, which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.1% for all values of θ. The total maximum variation in $A_O\,(1 + A\,(\theta))$ is therefore ±.4%.

Because the amplitude factor $(R_H - R_L)\, A_O\,(1 + A\,(\theta))$ varies simultaneously on all output lines, it will not be a source of error when the DRC-10520 is to drive a ratiometric system such as a resolver or synchro. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.

THERMAL CONSIDERATIONS

The power stage consists of two power amplifiers; one for the sine output and one for the cosine output. Maximum power stage junction temperature rise occurs at 0° and 180° for the sine output and 90° and 270° for the cosine output.

Maximum power dissipation for the hybrid occurs at the interquadrant points: 45°, 135°, 225°, and 315°. At these points the total power dissipation of each amplifier is 0.707 max. Therefore, the total power dissipation is 1.41 times the max for any one amplifier.

The thermal resistance junction to the outside of the case is 10.6°C/W. For a 2 VA purely inductive load and ±15VDC power supplies, the junction temperature rise is 42°C. For a real inductive load (one that has some power dissipation) and using pulsating supplies, the power dissipated is cut in half. The temperature rise is also halved to 21°C.

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	NC	12	5	23	14
2	NC	13	6	24	R_L
3	16 (LSB)	14	7	25	R_H
4	COS	15	8	26	15
5	SIN	16	$\overline{LM}$	27	−15V
6	+V	17	$\overline{LL}$	28	GND
7	−V	18	9	29	$\overline{LA}$
8	1 (MSB)	19	10	30	+15V
9	2	20	11	31	$\overline{BIT}$
10	3	21	12	32	NC
11	4	22	13		

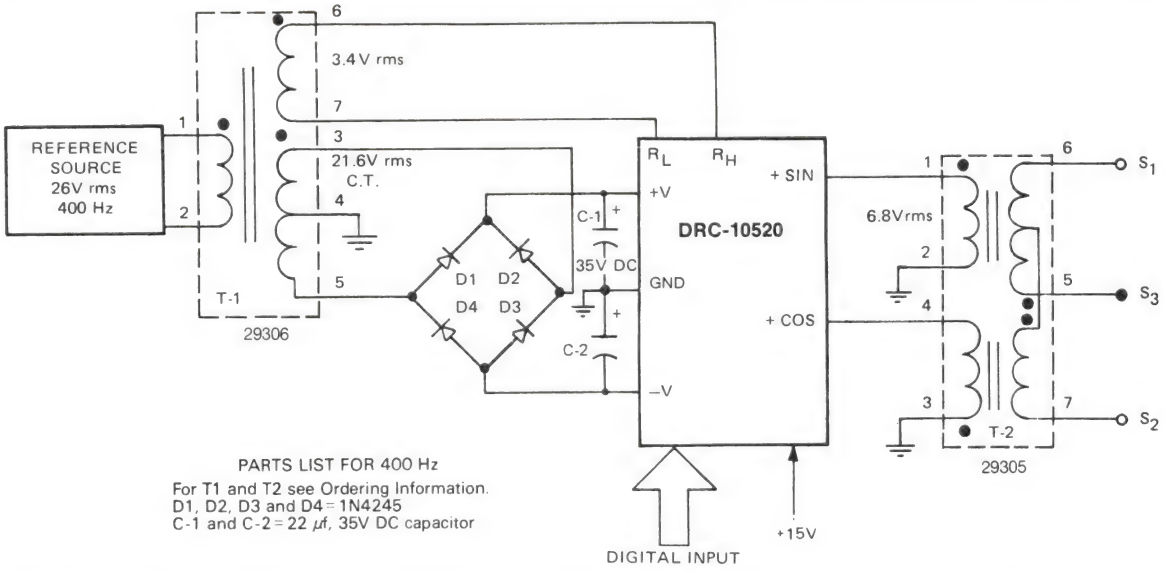
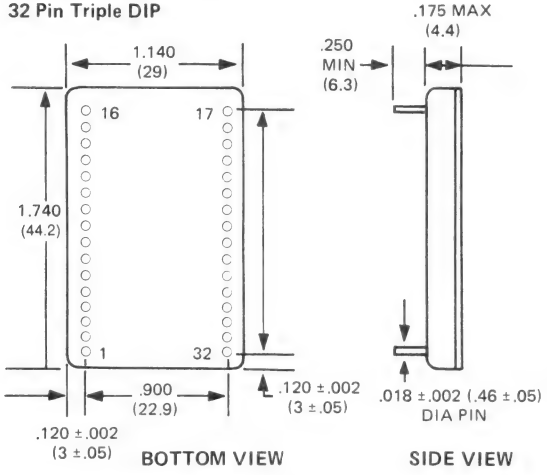


FIGURE 3. TYPICAL CONNECTION DIAGRAM UTILIZING PULSATING POWER SOURCE FOR SYNCHRO OUTPUT

MECHANICAL OUTLINE
32 Pin Triple DIP



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.010 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-883, Method 2003.
5. Tol ±.005 unless otherwise noted.

ORDERING INFORMATION

DRC-10520-X X X

- Accuracy: 3 = ±4 minutes; 4 = ±2 minutes; 5 = ±1 minute
- Reliability Grade: 0 = Standard DDC procedures. 1 = Fully compliant with MIL-STD-883. 2 = Screened to MIL-STD-883 but without QCI testing
- Operating Temperature Range: 1 = −55°C to +125°C (case); 3 = 0°C to +70°C (case)

TRANSFORMERS

FOR T1 USE:

P/N 29306 Power Transformer used for driving amplifier stage with reference source.

P/N 33920 Power Transformer for 115V input.

FOR T2 USE:

P/N 29305 Scott-T Transformer for 11.8V Synchro output.

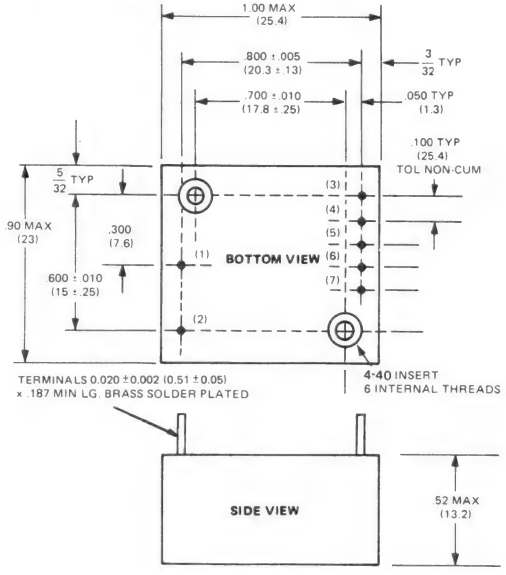
P/N 29947 Scott-T Transformer for 11.8V Resolver output.

P/N 32976 Scott-T Transformer for 90V Synchro output.

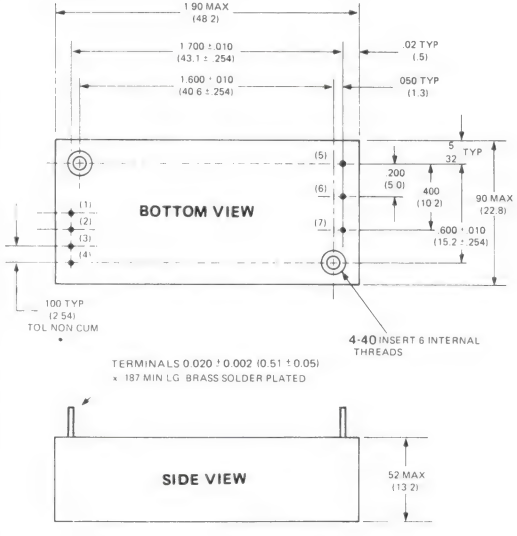
NOTE: The transformers listed above are representative of many available models. For alternative size and line to line levels contact the factory.

MECHANICAL OUTLINE
POWER TRANSFORMER (29306)

Dimensions in inches (millimeters)



MECHANICAL OUTLINE
OUTPUT SCOTT-T TRANSFORMER(29305)



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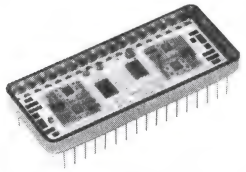
DDC
ILC DATA DEVICE CORPORATION

DRC-11522

2 CHANNEL D/R CONVERTER



DESCRIPTION

The DRC-11522 is a Dual 16 Bit Digital to Resolver Converter. Each channel is independent from the other with the exception of the 16 digital lines. The DRC-11522 allows the user to program the Gain of the Resolver Output

Packaged in a 36 pin double DIP, the DRC-11522 is 2 DSC-11520 D/R converters in one hybrid module.

With a synchro or resolver reference input, the DRC-11522 is a digital-to-resolver converter.

With a DC reference input, the unit can be used as a hybrid digital-to-sin/cos dc converter.

With the reference input proportional to the radius vector, the DRC-11522 converts polar to rectangular coordinates.

Hybrid technology results in low weight, low power consumption, very high reliability and a wide operating temperature range. A new, improved circuit design allows higher accuracy and reduces the output scale factor variation so that the output can drive displays directly. The output line-to-line voltage can be scaled by pin programming. Other features include buffered reference input and output short circuit protection.

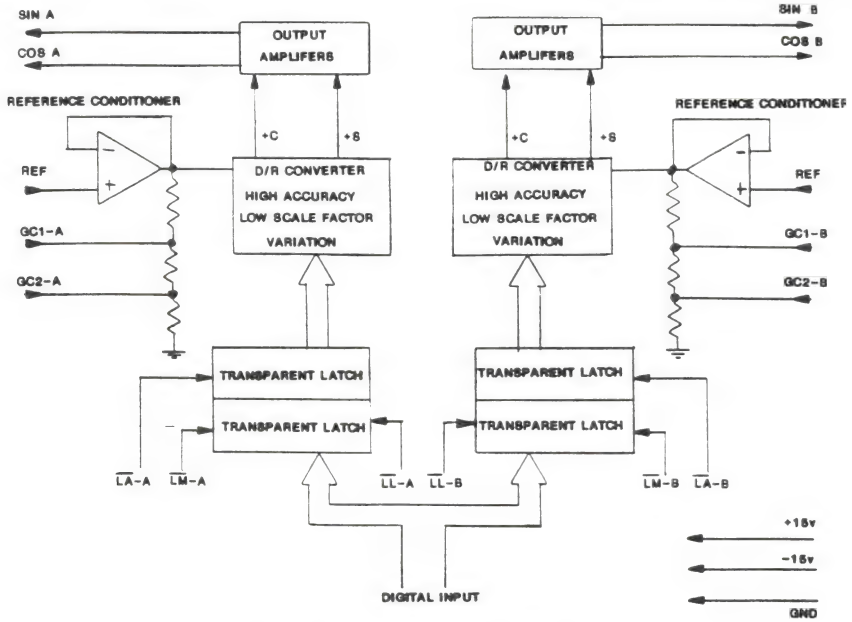
APPLICATIONS

Because of its high reliability, small size and low power consumption, the hybrid DRC-11522 is ideal for the most stringent and severe industrial and military ground or avionics applications. All units are available with MIL-STD-883B processing .

Among the many possible applications are computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, fire control systems, radar and navigation systems.

FEATURES

- *16 Bit Resolution*
- *Pin Programmable Gain Control*
- *2 Channels in One 36 Pin DDIP*
- *Accuracy: to ±1 Min.*
- *0.05% Scale Factor Variation with Angle*
- *DC Coupled Reference*
- *High Rel CMOS D/R Chip*
- *8 Bit/2 Byte Double Buffered Transparent Latches*



DRC-11522 BLOCK DIAGRAM

TABLE 1. SPECIFICATIONS (for each channel)
Apply over temperature range, power supply ranges. reference voltage and frequency range, and 10% harmonic distortion in the reference.

PARAMETER	VALUE	DESCRIPTION/REMARKS
RESOLUTION	16 bits (0.33 arc minutes)	MSB = 180° LSB = 0.0055°
ACCURACY		
Output Accuracy	±8 minutes to ±1 minute (see ordering info)	Accuracy applies over operating temp. range
Differential Linearity	±1 LSB max	
Radius accuracy	±0.03%	Simultaneous amplitude variation in both outputs as a function of digital angle
DYNAMICS		
Output Settling Time	Less than 20 µsec for any digital step change.	For any analog or digital step change
DIGITAL INPUT		
Logic Type		Natural binary angle, parallel positive logic CMOS and TTl compatible. Inputs are CMOS transient protected. Each input has a 20µa max pull down to GND.
Logic "0"	-0.3V-dc to 1.25V-dc	External logic voltage not needed. TTL compatible
Logic "1"	+2.0V-dc to +5.5V-dc	
Load Current	20µa max to GND	bits 1-16
	20µa to V_L	$\overline{LL}$, $\overline{LM}$, $\overline{LA}$ (See timing Diagram, Fig. 2)
REFERENCE INPUT		
Type		Programmable (See table 2.)
Frequency Range	DC to 1000Hz	DC to 10kHz with reduced accuracy.
Voltage	3.5V ±10%	0 to ±10 peak AC or DC
Input Impedance	10 M Ohm min	Operational Amplifier Buffer
ANALOG OUTPUT		
Type		Resolver
Output Current	2mA rms max	
Max Output Voltage (Tracks Reference Input Voltage)	$K \cdot V_{in} \cdot \sin\theta$ also $K \cdot V_{in} \cdot \cos\theta$	±10V peak AC or DC
Converter Gain (K)	0.5, 1.0, 2.0 ±1%	See table 2.
Transformation Ratio Tol.	±0.2% max	
Scale Factor Variation	±0.05% max	
DC Offset	±10mV typical, ±25mV max	Each Line to GND
Short Circuit Protection		Fully protected
POWER SUPPLIES		
Voltage	±15V-dc ±10%	For ±10V peak output
Max Voltage Without Damage	±18V	
Current or Impedance	±40 mA max	
TEMPERATURE RANGES (CASE)		
Operating		
-1 Option	-55°C to +125°C	
-3 Option	0°C to +70°C	
Storage	-60°C to +135°C	
PHYSICAL CHARACTERISTICS		
Type	36 pin double DIP	
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)	
Weight	0.6oz (17g) max	

F

TECHNICAL INFORMATION

DIGITAL INPUTS

For each channel the 16 bit digital angle is double buffered with transparent latches (see figure 1). The latch controls have internal pull-up current sources to +5V, this puts the latches in the transparent mode when they are not connected.

Angle is determined by adding the logic bits. The enable inputs are $\overline{LL}$ (1st Latch LSBs), $\overline{LM}$ (1st Latch MSBs), and $\overline{LA}$ (2nd Latch All); see figure 2 for timing.

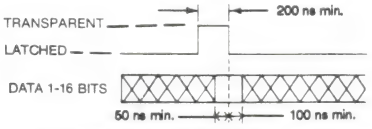


FIGURE 2. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAM

OUTPUT SCALING AND REF. LEVEL ADJUSTMENT

The DRC-11522 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage.
The maximum line-to-line levels are determined by the output amplifiers and are programmable for a gain of 0.5, 1.0, and 2.0 (see table below).

TABLE 2. PROGRAMMABLE GAIN

GC1-A (PIN 7)	GC2-A (PIN 8)	GAIN (K)
GND	OPEN	0.5
OPEN	GND	1.0
OPEN	OPEN	2.0

GC1-B (PIN 4)	GC2-B (PIN 5)	GAIN (K)

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:
$\sin = (REF \cdot K)A_0(1 + A(\theta)) \sin \theta$
$\cos = (REF \cdot K)A_0(1 + A(\theta)) \cos \theta$

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (REF · K). The transformation ratio A_0 is determined by the programmable gain inputs (0.5, 1.0, or 2.0). The maximum variation in A_0 from all causes is 0.1%. The term $A(\theta)$ represents the variation of the amplitude with the digital signal input angle. $A(\theta)$, which is called the scale factor variation, is a smooth function of (θ) without discontinuities and is less than ± 0.05% for all values of (θ). The total maximum variation in $A_0(1 + A((\theta)))$ is therefore ± 0.15%

Because the amplitude factor $(REF \cdot K)A_0(1 + A((\theta)))$ varies simultaneously on all output lines, it will not be a source of error when the DRC-11522 is to drive a ratiometric system. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.

TABLE 3. PIN OUTS

Pin	Function	Pin	Function
1	$\overline{LL}$-B	19	Bit 16 (LSB)
2	COS A	20	Bit 15
3	SIN A	21	Bit 14
4	GC1-B	22	Bit 13
5	GC2-B	23	Bit 12
6	Ref B	24	Bit 11
7	GC1-A	25	Bit 10
8	GC2-A	26	Bit 9
9	Ref A	27	Bit 8
10	COS B	28	Bit 7
11	SIN B	29	Bit 6
12	NC	30	Bit 5
13	+15V	31	Bit 4
14	-15V	32	Bit 3
15	$\overline{LA}$-B	33	Bit 2
16	$\overline{LA}$-A	34	Bit 1 (MSB)
17	$\overline{LL}$-A	35	$\overline{LM}$-A
18	GND	36	$\overline{LM}$-B

NOTE:
Functions $\overline{LL}$,$\overline{LM}$,$\overline{LA}$ both A and B may be left unconnected when not used.

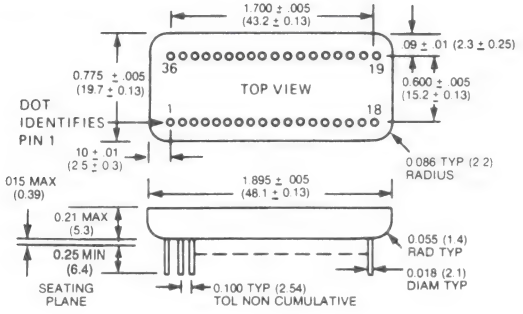
TABLE 4. PIN DEFINITIONS:

PIN	DEFINITION
GND	Power Supply Ground Digital Ground Analog Signal Ground
B1-B16	Digital input bits, B1 = MSB = 180 degrees
$\overline{LM}$-A	High Byte Enable (B1-B8) for MSB's 8 bit input register of channel A. Logic high enables, low holds.
$\overline{LM}$-B	High Byte Enable (B1-B8) for MSB's 8 bit input register channel B. Logic high enables, low holds.
$\overline{LL}$-A	Low Byte Enable (B9-B16) for LSB's 8 bit input register of channel A. Logic high enables, low holds
$\overline{LL}$-B	Low Byte Enable (B9-B16) for LSB's 8 bit input register of channel B. Logic high enables, low holds.
$\overline{LA}$-A	Channel A Load Converter. Logic high transfers Channel A input registers data into 16 bit holding register. When low Channel A is in hold mode.
$\overline{LA}$-B	Channel B Load Converter. Logic high transfers Channel B input registers data into 16 bit holding register. When low Channel B is in hold mode.
+15V	Power Supply Voltage.
-15V	Power Supply Voltage. **CAUTION:** **REVERSAL OF POWER SUPPLIES WILL DAMAGE THE CONVERTER.**
Ref-A	Channel A reference voltage input
Ref-B	Channel B reference voltage input
GC1-A	Channel A gain programming pin
GC2-A	Channel A gain programming pin
GC1-B	Channel B gain programming pin
GC2-B	Channel B gain programming pin
Sin A	Analog output of Channel A
Cos A	Analog output of Channel A
Sin B	Analog output of Channel B
Cos B	Analog output of Channel B

DRC-11522

MECHANICAL OUTLINE

36 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

ORDERING INFORMATION

DRC-11522 — 3 0 2

Accuracy
- 2 = ±8 minutes
- 3 = ±4 minutes
- 4 = ±2 minutes
- 5 = ±1 minute

Reliability Grade:
- 0 = Standard DDC procedures.
- 1 = 883B processing available.
- 2 = 883B processing available but without QCI testing.

Operating Temperature Range:
- 1 = -55°C to 125°C (Case)
- 3 = 0°C to +70°C (Case)

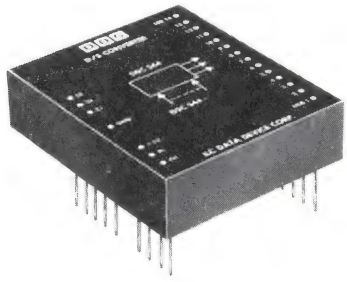
F

D

DDC
ILC DATA DEVICE CORPORATION

DSC-544*

14 BIT D/S CONVERTER 4.5VA; Powered From Ref Input



DESCRIPTION

The DSC-544 digital to synchro (D/S) converter complements the low profile DSC-644 industry standard by providing additional features. The DSC-544 has a 0.82" high profile and standard pinouts except that the need for +15V and -15V power supplies has been eliminated. Because the unit is powered from the reference input with an internal pulsating power supply it is much more efficient. The reduced heat dissipation has made it possible to increase the load at 400 Hz by a factor of three, and the power output at 60 Hz is limited only by the size of the internal power transformer.

The DSC-544 also retains the many improved features of the DSC-644. The output is fully protected against overloads, transients from load kickbacks, short circuits and overheating. An aluminum top plate in the module improves thermal dissipation. And a new circuit design provides a smoother, more accurate output with improved transient response and a negligible scale factor variation.

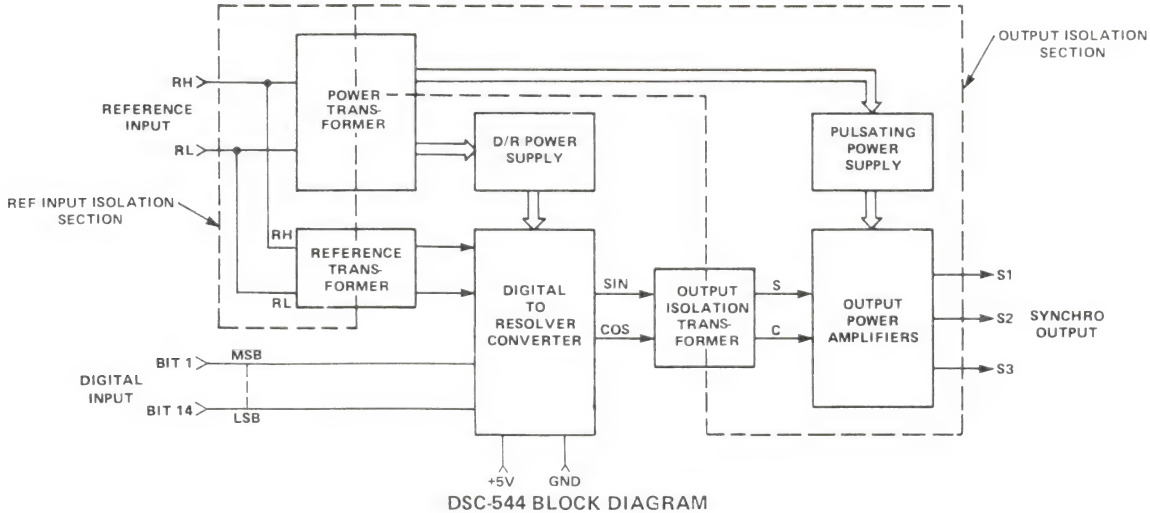
APPLICATIONS

The DSC-544 may be preferred when its special features are required: elimination of the ±15V power supplies, elimination of an external transformer at 60 Hz, greater drive capability at 400 Hz, and less heat dissipation. The converter is used in many applications where digitized shaft angle data must be converted to synchro form to drive control transformers, control differential transmitters, and angle indicators. Because these converters are very rugged, and meet the requirements of MIL-STD-202, they are suitable for the most severe industrial and military applications, including military ground support and avionics. They are used especially in computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, and fire control systems.

FEATURES

- *POWER DISSIPATION CUT IN HALF:*
  AT 400 Hz, DRIVING 4.5 VA, DISSIPATES 6W
  AT 60 Hz, DRIVING 1.5 VA, DISSIPATES 3W
- *DOES NOT REQUIRE +15V OR –15V SUPPLIES*
- *NO EXTERNAL TRANSFORMER AT 60 Hz*
- *VIRTUALLY INDESTRUCTABLE:*
  RUGGED POWER AMPLIFIERS WITH CURRENT LIMITING
  COMPLETELY SHORT-CIRCUIT PROOF
  OVERVOLTAGE TRANSIENT PROTECTION
  THERMAL CUTOFF
- *OUTPUT*
  TRANSFORMER ISOLATED OUTPUT
  90V SYNCHRO OUTPUT AT 400 Hz AND 60 Hz
- *DIGITAL INPUT*
  CMOS AND TTL COMPATIBLE
  PARALLEL BINARY ANGLE INPUT
- *POWER SUPPLIES REQUIRED:*
  +5 V ONLY

*Patented



DSC-544 BLOCK DIAGRAM

DSC-544 SPECIFICATIONS

Apply over operating temperature and frequency ranges, ±5% variation of power supply, ±10% reference amplitude variation, up to 10% reference harmonic distortion, and for any load up to full load.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY (TO FULL LOAD)	
Output Accuracy	±4 minutes
Differential Linearity	±1 LSB max
ANALOG OUTPUT (TRANSFORMER ISOLATED)	
Drive Capability (L-L Balanced)	
Synchro Output	
90V rms L-L, 360 – 440 Hz (Option H)	1.33 KΩ min
90V rms L-L, 57 – 63 Hz (Option I)	4.0 KΩ min
Output Scale Factor	
Absolute (All Causes)	± 2%max simultaneous amplitude variation on all output lines, including variation with digital angle. Output amplitude tracks reference input amplitude.
Variation With Digital Angle	±0.1% max
Output Quadrature	±0.2% max
DIGITAL INPUT	
Logic Type	Natural binary angle; parallel positive logic TTL compatible Transient protected CMOS 33 KΩ pull-up to +5V
Loading	0.13 Std. TTL load

PARAMETER	VALUE
REFERENCE INPUT (TRANSFORMER ISOLATED)	
Ref Voltage Level	115V rms ±10%
Max Voltage Without Damage	138V rms
Current	
No Load	
Option H	40 mA max
Option I	50 mA max
Additional With Load	1 mA per mA of load
POWER SUPPLY	
Voltage	+5V
Max Voltage Without Damage	+7V
Current	20 mA max
TEMPERATURE RANGES	
Operating (Temperature of Metal Plate on Top of Case)	
–1 Option	–55°C to +85°C
–3 Option	0°C to +70°C
Storage	–55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 x 2.625 x 0.82 inch (7.94 x 6.67 x 2.08 cm)
Weight	8 oz. max (227 g)

*The output amplifiers will drive loads with any phase angle from –90° to +90°

TECHNICAL INFORMATION

INTRODUCTION

The DSC-544 circuit is divided into 3 parts which are transformer isolated from each other (see Block Diagram). The first part contains the reference input, the second part contains the digital input and an internal digital to resolver converter, and the third part contains output power amplifiers and an associated pulsating power supply.

Reference input isolation is provided both by the reference transformer and by the power transformer. The converter output signals are proportional to the applied reference, and any distortion in the reference input will appear in the output signals. The power transformer output has a voltage clamp which protects the power amplifiers against transients in the reference input.

The internal digital to resolver (D/R) converter in the DSC-544 operates from an internal power supply connected to the reference input. The circuit in the internal D/R converter is based on an alogorithm whose theoretical math error is only ±3.5 arc-seconds (less than 5% of 1 LSB), and whose theoretical scale factor variation with angle is less than ±0.015%. The output is well behaved, with negligible glitches at major transition points. The accuracy and scale factor error are limited by the physical components, not by the algorithm.

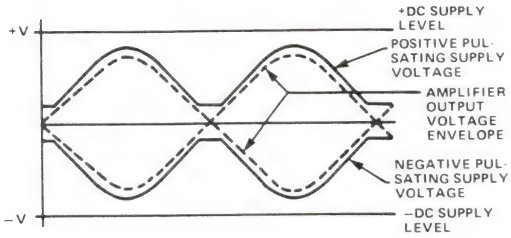
The digital inputs are transient protected CMOS switches with 33 KΩ pull-up resistors to the +5 V supply, and can be driven by all standard TTL gates. If the TTL gates drive other loads as well, the circuit must allow the 33 KΩ resistors to pull up the logic 1 level to within 1.0V of the +5V supply. Bit weights for the 14 binary inputs are given in the bit weight table. Angle is determined by adding bits in the logic 1 state.

Bit	Deg/Bit	Min/Bit	Bit	Deg/Bit	Min/Bit
1MSB	180	10,800	8	1.406	84.38
2	90	5,400	9	0.7031	42.19
3	45	2,700	10	0.3516	21.09
4	22.5	1,350	11	0.1758	10.55
5	11.25	675	12	0.0879	5.27
6	5.625	337.5	13	0.0439	2.64
7	2.813	168.75	14LSB	0.0220	1.32

BIT WEIGHT TABLE

The most novel features of the DSC-544 converter are in the output section. The pulsating power supply produces two unfiltered, full-wave-rectified positive and negative voltages as shown in the diagram. These voltages are in the phase with the amplifier output voltage because the power is derived from the reference input. The amplitude of the two voltages need only be a few volts greater than the power amplifier output voltage, since both will change together if the reference level changes. As indicated in the diagram, the positive and negative pulsating power supply voltage levels will be consistently lower than the constant DC levels of any DC supplies. Because the voltage levels are lower, the power consumed will be much less. The power dissipated as heat is equal to the amplifier current times the difference in voltage between the power supply and the output. For the DSC-544, the power dissipated is reduced by approximately 50% for reactive loads.

Another advantage of deriving power from the reference input is that the amplifier section power is easily transformer isolated from the D/R converter. The converter output isolation transformer can therefore be located in front of the power amplifiers. Because it does not transfer power it can be made smaller, and an internal transformer can be used at 60 Hz.



PULSATING POWER SUPPLY VOLTAGE WAVEFORMS

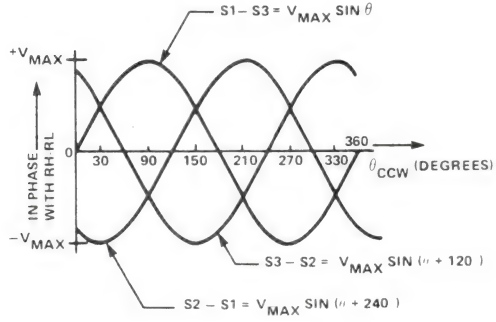
Minimum load impedances are listed in the Specifications Table under Drive Capability. The DSC-544 can drive these impedances under the worst case conditions stated in the table. The minimum load impedances correspond to 4.5 VA at 400 Hz and 1.5 VA at 60 Hz when the frequencies and voltage levels are at their nominal values. The metal top of the converter module should be provided with sufficient air circulation.

The thermal cutout disables the output power amplifiers when the internal temperature reaches 125° C. The output is automatically restored when the temperature drops again.

OUTPUT PHASING AND SCALE FACTOR

The analog output signals have the following phasing as shown in the synchro output signal diagram:

$S1 - S3 = (RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \sin\theta$
$S3 - S2 = (RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \sin(\theta + 120°)$
$S2 - S1 = (RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \sin(\theta + 240°)$

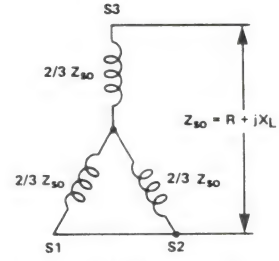


SYNCHRO OUTPUT SIGNALS

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RHRL). The amplitude factor A_0 is 90/115 for 90 V rms L-L output. The maximum variation is A_0 from all causes is ±1.9%. The term A term $A(\theta)$ represents the variation of the amplitude with the digital input angle. $A(\theta)$, which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.001 for all values of θ. The total maximum variation in $A_0\ (1 + A(\theta))$ is therefore ±2%. Because $A(\theta)$ is so small, the DSC-544 can be used to drive systems such as X-Y plotters or CRT displays in which the sin and cos outputs are used independently (not ratiometrically as in control transformer).

DRIVING CT AND CDX LOADS

When driving CT and CDX loads the DSC-544 must have enough steady state power capability to drive the Z_{SO} of the load. Z_{SO} (stator impedance with rotor open-circuited) is measured as shown in the diagram:



Z_{SO} MEASUREMENT

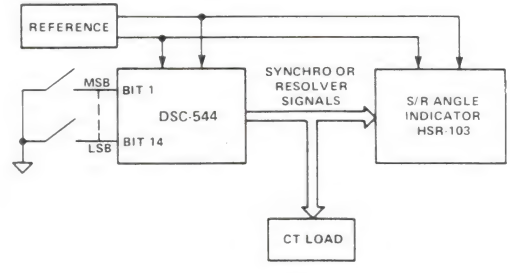
The following table shows the load impedance of some typical control transformers.

SOME COMMON CONTROL TRANSFORMERS AND THEIR LOAD IMPEDANCES

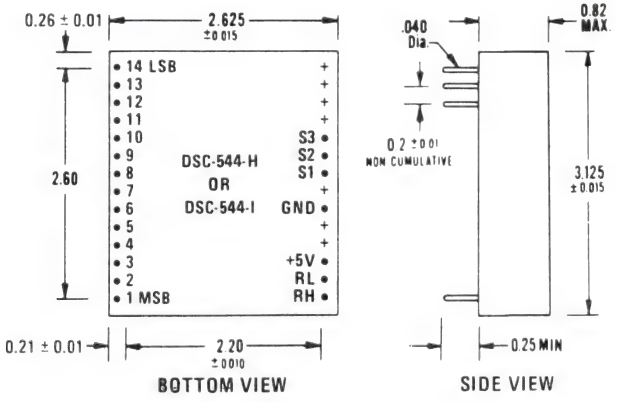
Military Type Number	Size	Z_{SO}
26V 08CT4c	08	100 + j490
26V 11CT4d	11	21 + j132
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1420 + j13260
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980

ACCURACY TESTS

The accuracy of the 544 may be tested with a high accuracy synchro/resolver angle indicator and a load such as a control transformer, as shown in the diagram. The bit switches are set to the desired test angles and the output angle is measured under load. The accuracy should conform to the specifications.



MECHANICAL OUTLINE



NOTES

1. Pin labels on bottom view are for reference only.
2. All dimensions shown are in inches.
3. Pin material meets solderability requirements of MIL-STD-202, Method 208C.
4. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F, except top surface is black anodized aluminum plate for heat transfer.
5. Any LSB pins not used should be grounded.

F

ORDERING INFORMATION

DSC 544 – H – 1 – R

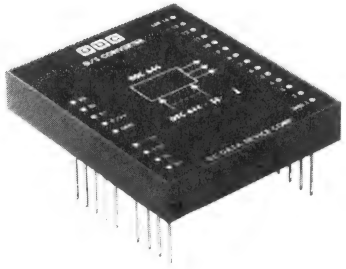
- R = Enhanced Reliability
- Operating Temperature Range of Case Metal Top
  - 1 = 55° to +85° C
  - 3 = 0° C to +70° C
- Synchro Output Voltage Level and Frequency
  - H = 90 V rms L-L, 360-440 Hz
  - I = 90 V rms L-L, 57-63 Hz

If a converter module socket is required, order socket number 9010.

C

DSC-644*

14 BIT D/S AND D/R CONVERTER
New Low-profile Industry Standard



DESCRIPTION

The DSC-644 is the first low-profile D/S and D/R converter. It is only 0.52 inches high, has standard pin configuration, and is designed to be a new industry standard. The DSC-644 accepts 14 bit digital input angle and a reference excitation, and produces a synchro or resolver output with moderate drive capability. The output is fully protected to prevent damage to the converter. The rugged, current-limited power output stage has overload and transient protection, and a thermal cut off to prevent overheating. The output is short-circuit proof and an aluminum top plate improves the thermal dissipation. The DSC-644 also has a new circuit design that provides a more accurate output with an improved transient response and a negligible scale factor variation. Reliability has also been increased, and cost is reduced.

The DSC-644 module contains an input reference isolation transformer. An internal output transformer is also included for all 400 Hz versions. The 60 Hz option requires a separate output transformer.

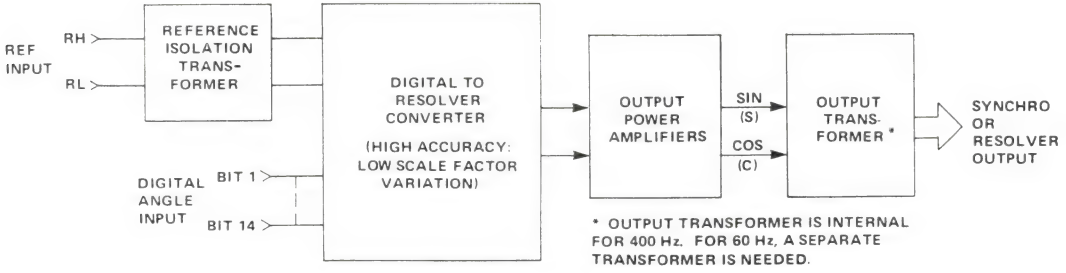
APPLICATIONS

The DSC-644 is used when digitized shaft angle data must be converted to synchro or resolver form to drive control transformers, control differential transmitters and angle indicators. Because these converters are very rugged, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial and military applications, including military ground support and avionics. They are used especially in computer based systems in which digital information is processed, such as simulators, flight trainers flight instrumentation, and fire control systems.

FEATURES

- *FULLY PROTECTED OUTPUT:*
  RUGGED OUTPUT AMPLIFIERS WITH CURRENT LIMITING
  COMPLETELY SHORT-CIRCUIT PROOF
  OVERVOLTAGE TRANSIENT PROTECTION
  THERMAL CUTOFF
- *METAL HEATSINK AT TOP OF CASE: CONSERVATIVE THERMAL DESIGN*
- *VERY LOW SCALE FACTOR VARIATION: 0.05% TYPICAL*
- *OUTPUT:*
  INTERNAL TRANSFORMER ISOLATION AT 400 Hz
  ALL COMMON SYNCHRO/RESOLVER VOLTAGE LEVELS AND FREQUENCIES
- *DIGITAL INPUT:*
  CMOS AND TTL COMPATIBLE
  PARALLEL BINARY ANGLE INPUT
- *POWER REQUIRED:*
  ±15V DC AND +5V DC

*Patented



DSC-644 BLOCK DIAGRAM

DSC-644 SPECIFICATIONS

Apply over operating temperature and frequency ranges, ±5% variation of power supplies, ±10% reference amplitude variation, up to 10% reference harmonic distortion, and for any balanced load up to full load.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY (To Full Load)	
Output Accuracy	±4 minutes
Differential Linearity	±1 LSB max
DIGITAL INPUT	
Logic Type	Natural binary angle; parallel positive logic TTL compatible; Transient protected CMOS 33 KΩ pull-up to +5V
Loading	0.13 Std. TTL load

REFERENCE INPUT (TRANSFORMER ISOLATED)

	Ref. Voltage Level*	Max. Ref. Current
Units with 90V rms L-L Output	115V rms	0.6 mA
Units with 11.8V rms L-L Output	26V rms	0.6 mA

*+20% absolute max to avoid damage

ANALOG OUTPUT (TRANSFORMER ISOLATED)	
Drive Capability (L-L Balanced*)	
Synchro Output	
90V rms L-L, 360 – 440 Hz (Option H)	4 KΩ min
90V rms L-L, 57 – 440 Hz (Option 6)	4 KΩ min
11.8V rms L-L, 360 – 440 Hz (Option L)	70 Ω min
Resolver Output	
11.8V rms L-L, 360 – 440 Hz (Option L)	93 Ω min
Output Scale Factor	
Absolute (All Causes)	±2% max simultaneous amplitude variation on all output lines, including variation with digital angle. Output amplitude tracks reference input amplitude.
Variation With Digital Angle	±0.1% max
Output Quadrature	±0.3% max

*The output amplifiers will drive loads with any phase angle from −90° to +90°

POWER SUPPLIES			
Voltage	+15V	−15V	+5V
Max Voltage Without Damage	+18V	−18V	+7V
Average Current	150 mA max	150 mA max	5 mA max
Peak Current With Normal Load	330 mA max	330 mA max	5 mA max
Peak Current at Power Turn-On or Short Circuit	600 mA max	600 mA max	5 mA max

TEMPERATURE RANGES	
Operating (Temperature of Metal Plate on Top of Case)	
−1 Option	−55°C to +85°C
−3 Option	0°C to +70°C
Storage	−55°C to +125°C
PHYSICAL CHARACTERISTICS	
Converter Module (encapsulated)	
Size	3.125 x 2.625 x 0.52 inch (7.94 x 6.67 x 1.32 cm)
Weight	5.1 oz max (145 g)
60 Hz Transformer Module (encapsulated)	
Size	2.25 x 2.25 x 0.81 inch (5.7 x 5.7 x 2.1 cm)
Weight	10.5 oz max (298 g)

TECHNICAL INFORMATION

INTRODUCTION

The DSC-644 contains an internal digital to resolver (D/R) converter (refer to the block diagram) which has an inherently high accuracy and low scale factor variation. The circuit in the internal D/R converter is based on an algorithm whose theoretical math error is only ±3.5 arc-seconds (less than 5% of 1 LSB), and whose theoretical scale factor variation with angle is less than ±0.015%. The output is well behaved, with negligible glitches at major transition points. The accuracy and scale factor error are now limited by the physical components, not by the algorithm.

The digital inputs are transient protected CMOS switches with 33 KΩ pull-up resistors to the +5V supply, and can be driven by all standard TTL gates. If the TTL gates drive other loads as well, the circuit must allow the 33 KΩ resistors to pull up the logic 1 level to within 1.0V of the +5V supply. Bit weights for the 14 binary inputs are given in the bit weight table. Angle is determined by adding bits in the logic 1 state.

Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14 LSB	0.0220	1.32

BIT WEIGHT TABLE

The internal reference input transformer provides isolation at both 60 Hz and 400 Hz, so a change of frequency will not cause damage. The input is specified for operation at a reference level of either 115V or 26V rms. The output signals are proportional to the applied reference, and any distortion in the reference input will appear in the output signals.

A thermal cutout disables the output power amplifiers when the internal temperature reaches 125°C. The output is automatically restored when the temperature drops again.

The DSC-644 will not be damaged by any sequencing order or interruptions in either the dc supplies or the reference input. However, if one of the 15V supplies is shut down or subsequently powered up, maximum turn on current (450 mA) will be drawn from the other 15V supply until the missing 15V supply is restored.

The 60 Hz synchro unit requires both a converter module (DSC-644-6) and a separate transformer because of the transformer size. The output power amplifiers on the −6 module provide a 7V rms nominal ±2% resolver signal for the external transformer when the reference input is 115V rms.

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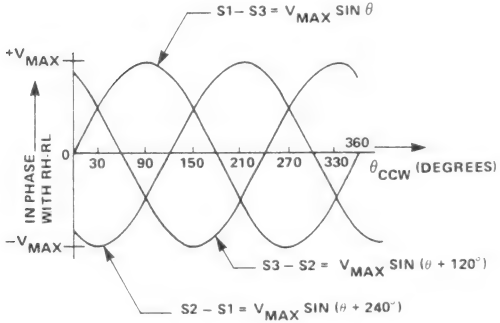
Minimum load impedances are listed in the Specifications Table under Drive Capability. The DSC-644 can drive these impedances under the worst case conditions stated in the table. The minimum load impedances correspond to a 1.5VA drive capability when the line voltages and frequencies are at their nominal values. The metal top of the converter module should be provided with sufficient air circulation.

DDC also manufactures the DSC-544, another D/S converter which provides 60 Hz and 400 Hz 90V L-L synchro output. The DSC-544 is a high efficiency, reference powered converter with a standard 0.82 inch high profile. It does not require ±15V power supplies. When driving the same load, the DSC-544 dissipates half as much power as the DSC-644. At 400 Hz the DSC-544 can drive 4.5VA compared to 1.5VA for the DSC-644. Both units can drive 1.5VA at 60 Hz, but the SDC-544 does not require an external transformer at this frequency.

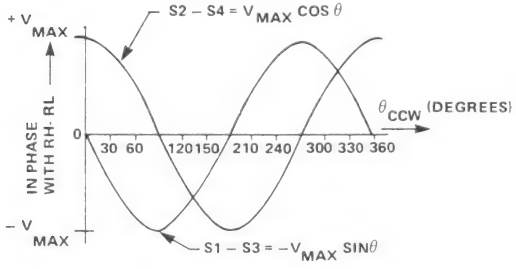
OUTPUT PHASING AND SCALE FACTOR

The analog output signals have phasing as shown in the following synchro and resolver output signal diagrams:



SYNCHRO OUTPUT SIGNALS

Synchro output
S1 – S3 = (RH-RL) A_0 (1 + A(θ)) sin θ
S3 – S2 = (RH-RL) A_0 (1 + A(θ)) sin (θ + 120°)
S2 – S1 = (RH-RL) A_0 (1 + A(θ)) sin (θ + 240°)



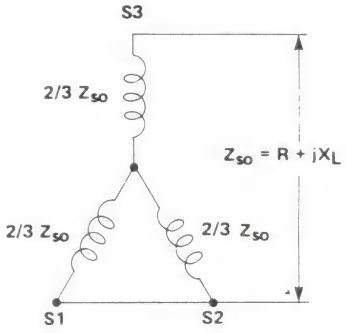
RESOLVER OUTPUT SIGNALS

Resolver output
S1 – S3 = –(RH-RL) A_0 (1 + A(θ)) sin θ
S2 – S4 = (RH-RL) A_0 (1 + A(θ)) cos θ

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The amplitude factor A_0 is 90/115 for 90V rms L-L output and 11.8/26 for 11.8V rms L-L output. The maximum variation in A_0 from all causes is ±1.9%. The term A(θ) represents the variation of the amplitude with the digital input angle. A(θ), which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.001 for all values of θ. The total maximum variation in A_0 (1 + A(θ)) is therefore ±2%. Because A(θ) is so small, the DSC-644 can be used to drive systems such as X-Y plotters or CRT displays in which the sin and cos outputs are used independently (not ratiometrically as in a control transformer).

DRIVING CT LOADS

When driving CT loads the DSC-644 must have enough power drive capability to drive the Z_{SO} of the load. Z_{SO} (stator impedance with rotor open-circuited) is measured as shown in the diagram:



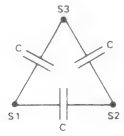
Z_{SO} MEASUREMENT

The following table shows the load impedance of some typical control transformers.

IMPEDANCES OF COMMON CONTROL TRANSFORMERS

Military Type Number	Size	Z_{SO}
26V 08CT4c	08	100 + j490
26V 11CT4d	11	21 + j132
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1420 + j13260
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Three capacitors may be placed across the legs of the synchro stator in a delta configuration:



DELTA TUNING CONFIGURATION

The correct value of the capacitance C in Farads is given by:

$$C = \frac{X_L}{4\pi f (R^2 + X_L^2)}$$

where f is the carrier frequency and R and X_L are the series real and reactive components of Z_{SO}. High grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel, because the load impedance Z is increased to:

$$Z = \frac{R^2 + X_L^2}{R}$$

ACCURACY TESTS

The accuracy of the 644 may be tested with a high accuracy synchro/resolver angle indicator and a load such as a control transformer, as shown in the diagram. The bit switches are set to the desired test angles and the output angle is measured under load. The accuracy should conform to the specifications.

TEST METHODS

DSC-644 converter modules are high quality products whose semiconductor components are hermetically sealed. These modules will meet the specific test methods and conditions of MIL-STD-202E shown unless alternative methods are specified by the customer in his procurement documentation.

METHOD	CONDITION	COMMENT
204C	C	10G, 2000 Hz vibration
213B	A	50G, 11ms shock
106D*	–	Moisture
107D	A	Thermal shock
101D	B	Salt spray
105C	B	50,000 ft. altitude

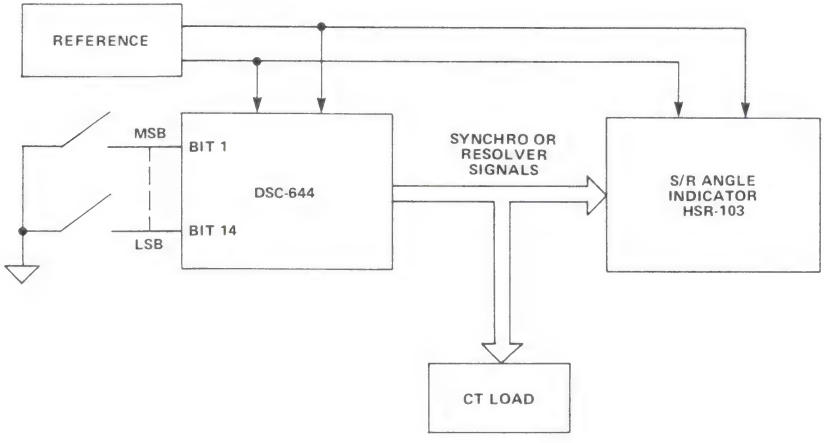
*when conformally coated on P.C. board

MIL-STD-202E TEST METHODS

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

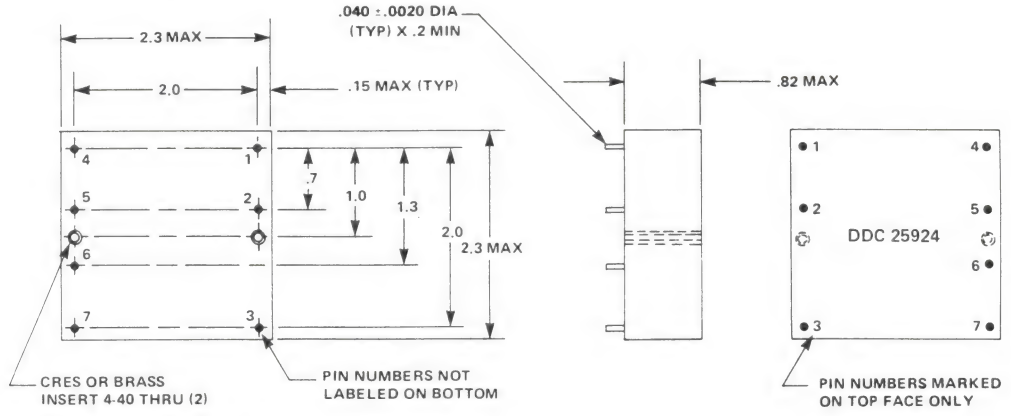
It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.



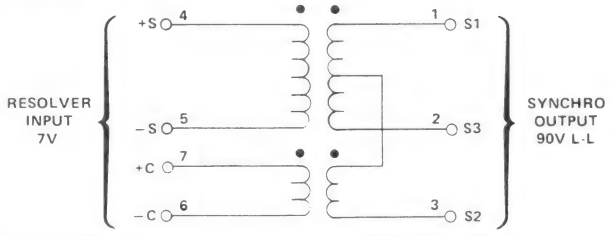
ACCURACY TEST CIRCUIT

60 Hz EXTERNAL SYNCHRO TRANSFORMER DDC-25924.

1. Mechanical Outline (Dimensions in inches, ±0.01 inch, unless otherwise indicated.)



2. Schematic Diagram

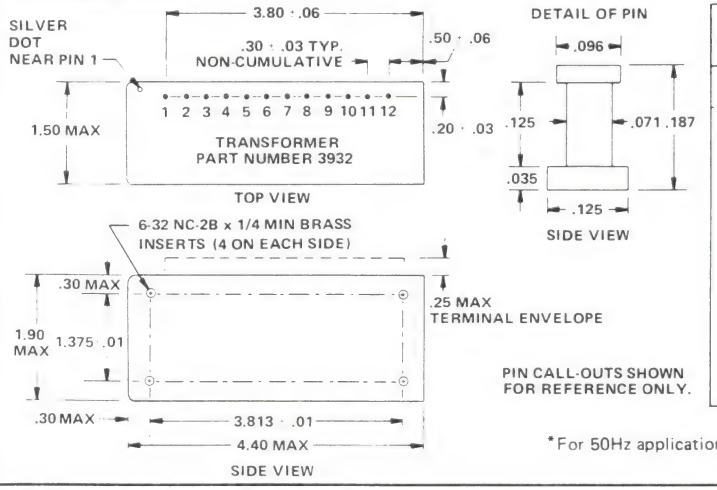


TRANSFORMER CONNECTIONS

Transformer Pin Number	Connect To	
1	S1	Synchro Output
2	S3	90V L-L
3	S2	57-440 Hz
4	SIN	To Converter Module
5	GND	
6	GND	
7	COS	

50 Hz EXTERNAL SYNCHRO TRANSFORMER DDC-3932*

1. Mechanical Outline

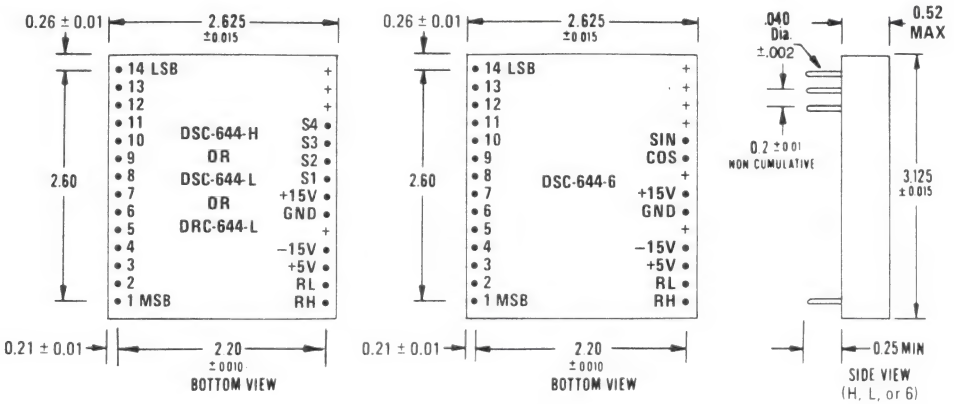


TRANSFORMER CONNECTIONS

Transformer Pin Number	Connect To	
1	S1	Synchro Output
2	S3	90V rms L-L
3	S2	47-440 Hz
4	SIN	To Converter Module
5	GND	
6	GND	
7	COS	
8	RH	Do Not Use
9	RL	
10	+R	Do Not Use
11	RC	
12	–R	

*For 50Hz applications P/N DDC-3932 must be ordered.

MECHANICAL OUTLINE FOR CONVERTER MODULE



NOTES
1. Pin labels on bottom view are for reference only.
2. All dimensions shown are in inches.
3. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
4. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F, except top surface is a black anodized aluminum plate for heat transfer.
5. Pin S4 is present on resolver units only.
6. Any LSB pins not used should be grounded.

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ORDERING INFORMATION

1. Order converter modules as follows. 400 Hz units (H and L) have an internal output transformer. 60 Hz units require an external transformer which must be ordered separately as desired below. If a converter socket is required, order socket number 9010.

DSC-644 – H – 1 – R

- R — High Reliability
- 1 — Operating Temperature Range of Metal Top
  - 1 = –55° C to + 85° C
  - 3 = 0° C to + 70° C
- H — Output Voltage Level and Frequency
  - H = 90 V rms L-L, 360-440 Hz (Synchro only)
  - L = 11.8 V rms, L-L, 360-440 Hz (Synchro or Resolver)
  - 6 = 90 V rms L-L, 47-440 Hz (synchro only) see No. 2 below
- DSC-644 — Output Type
  - DSC = Synchro
  - DRC = Resolver

2. For -6 Option:
   (a) For 57-440 Hz application, either the transformer P/N DDC-3932 or DDC-25924 may be used.
   (b) For 47-440 Hz applications, transformer P/N DDC-3932 must be used. Reference pins should not be connected.

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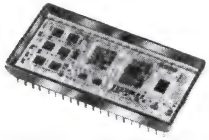
DSC-10510®

7VA D/S CONVERTER



FEATURES

- *7VA DRIVE CAPABILITY FOR CT, CDX, OR TR LOADS*
- *Z_{ss} = 2 OHMS FOR TR LOADS*
- *DOUBLE BUFFERED TRANSPARENT INPUT LATCH*
- *16 BIT RESOLUTION*
- *UP TO 1 MINUTE ACCURACY*
- *POWER AMPLIFIER USES PULSATING OR DC SUPPLIES*
- *BUILT-IN-TEST (BIT) OUTPUT*
- *S2 GROUNDED, 5VA DRIVE CONFIGURATION AVAILABLE*

DESCRIPTION

With 16 bit resolution and up to ±1 minute accuracy, the DSC-10510 is a high power digital to synchro converter capable of driving multiple Control Transformer (CT) and Control Differential Transmitter (CDX) loads up to 7VA and Torque Receiver (TR) loads up to Z_{ss} = 2 Ohms.

The DSC-10510 contains a high accuracy D/R converter, a triple power amplifier stage, a walk around circuit (to prevent torque receiver hangups), and thermal and over-current protection circuits. The hybrid is protected against short circuits, overloads, load transients, over-temperature, loss of reference, and power amplifier or DC power supply shutdown, making it virtually indestructible.

Microprocessor compatibility is provided through a 16 bit/2 byte double buffered input latch. Data input is natural binary angle in TTL compatible parallel positive logic format.

Packaged in a 40 pin TDIP, the DSC-10510 features a power stage that may be driven by either a standard ±15VDC supply or by a pulsating reference supply when used with an optional power transformer. When powered by the reference source, heat dissipation is reduced by 50%.

APPLICATIONS

The DSC-10510 can be used where digitized shaft angle data must be converted to an analog format for driving CTs, CDXs, and TRs loads. With its double buffered input latches, the DSC-10510 easily interfaces with microprocessor based systems such as flight simulators, flight instrumentation, fire control systems, and air data computers. For aircraft applications requiring S2 grounded, 5VA drive configurations, the DSC-10511 is available.

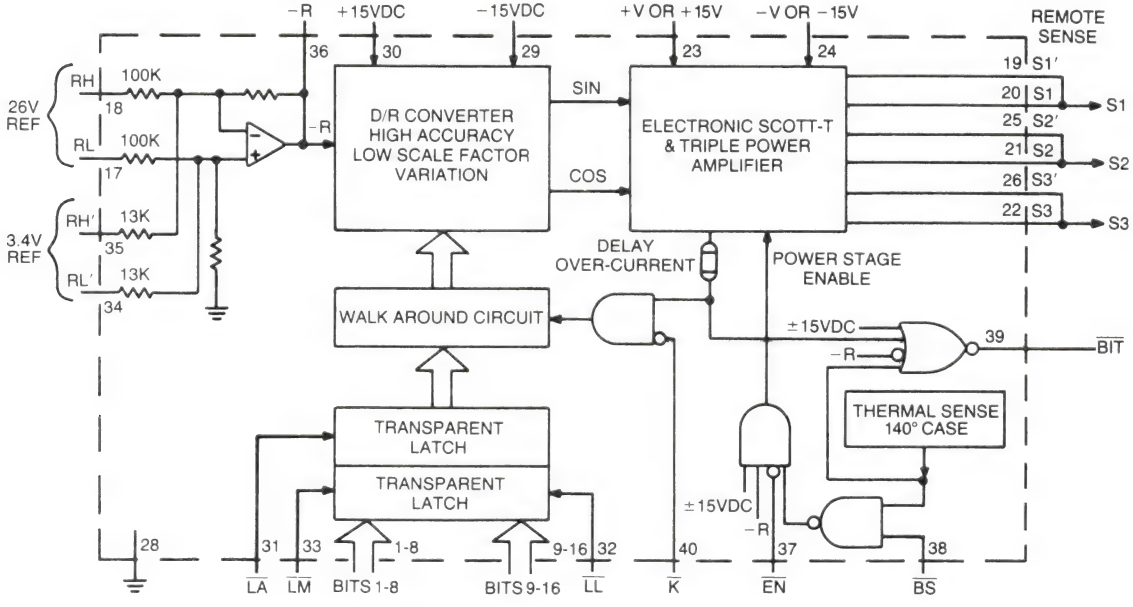


FIGURE 1. DSC-10510 BLOCK DIAGRAM

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TABLE 1. DSC-10510 SPECIFICATIONS

PARAMETER	VALUE	DESCRIPTION
RESOLUTION	16 bits	Bit 1 = MSB, Bit 16 = LSB
ACCURACY	±1, 2, or 4 minutes	
DIFFERENTIAL LINEARITY	1 LSB max in the 16th bit	
OUTPUT SETTLING TIME	40μs max	For any digital input step change (passive loads).
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Digital Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	All inputs except $\overline{K}$ (Kick, pin 40).
Loading	20 μA max to GND // 5pf max	Bits 1-16, $\overline{BS}$, and $\overline{EN}$.
	20 μA max to +5V // 5pf max	$\overline{LL}$, $\overline{LM}$, and $\overline{LA}$ (CMOS transient protected)
$\overline{K}$	20 μA max	Ground to enable Kick circuit, open to disable; pulls self up to +15V.
Digital Outputs		
$\overline{BIT}$		Logic 0 for BIT condition (see BIT pin function)
Drive Capability	Logic 0 = 1 TTL Load	1.6mA at 0.4V max
	Logic 1 = 10 TTL Loads	0.4mA at 2.8V min
REFERENCE INPUT		
Type	26Vrms differential	RH-RL
	3.4Vrms differential	RH'-RL'
Max Voltage w/o Damage	72.8Vrms for RH-RL	
	9.52Vrms for RH'-RL'	
Frequency	DC to 1 KHz	
Input Impedance		
Single Ended	100K Ohms ±0.5%	RH-RL
	13K Ohms ±0.5%	RH'-RL'
Differential	200K Ohms ±0.5%	RH-RL
	26K Ohms ±0.5%	RH'-RL'

TABLE 1. DSC-10510 SPECIFICATIONS (Continued)

PARAMETER	VALUE	DESCRIPTION
SYNCHRO OUTPUT		DSC-10510 DSC-10511 S2 Grounded
Voltage L-L	11.8Vrms ±0.5% for nom Ref V	
Scale Factor Variation	±0.1% max	Simultaneous amplitude variation on all output lines as a function of digital angle.
Current	700mA rms max	
CT or CDX Load	7VA max	5VA for DSC-10511
TR Load	Z_{ss} = 2 Ohm min	
DC Offset	±15mV max	Each line to ground. Varies with angle.
Protection	Yes	Output protected from overcurrent, short circuit, voltage feedback transient, and overtemperature, loss of reference, loss of power amplifier, and loss of ±DC supply voltage.

POWER SUPPLY CHARACTERISTICS		
Nominal Voltage	±15V	±V
Voltage Range	±5%,	20V peak max 3V above output min
Max Voltage w/o Damage	18V	25V
Current	25mA max	load dependent

TEMPERATURE RANGES	
Operating, Case	
−3XX	0°C to + 70°C
−1XX	−55°C to +125°C
Storage	−65°C to +150°C

PHYSICAL CHARACTERISTICS		
Size	2.0 x 1.1 x 0.2 inches (50.8 x 27.9 x 5.1 mm)	40 Pin Triple DIP
Weight	0.9 oz	

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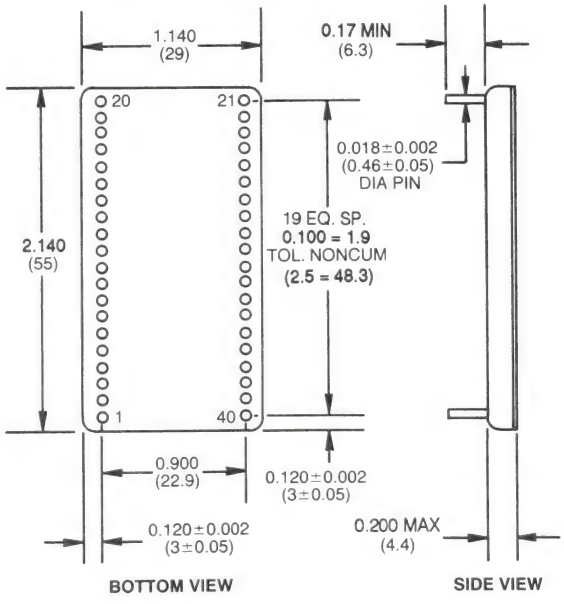
TABLE 2. DSC-10510 PIN FUNCTIONS

PIN	NAME	FUNCTION
1	D01	Digital Input 01 (MSB) Logic "1" enables.
2	D02	Digital Input 02
3	D03	Digital Input 03
4	D04	Digital Input 04
5	D05	Digital Input 05
6	D06	Digital Input 06
7	D07	Digital Input 07
8	D08	Digital Input 08
9	D09	Digital Input 09
10	D010	Digital Input 10
11	D011	Digital Input 11
12	D012	Digital Input 12
13	D013	Digital Input 13
14	D014	Digital Input 14
15	D015	Digital Input 15
16	D016	Digital Input 16 (LSB)
17	RL	26Vrms Reference Low Input
18	RH	26Vrms Reference High Input
19	S1′	Synchro S1 Remote Sense Output
20	S1	Synchro S1 Output
21	S2	Synchro S2 Output. Remotely grounded on DSC-10511
22	S3	Synchro S3 Output
23	+V	Power Stage +V
24	−V	Power Stage −V
25	S2′	Synchro S2 Remote Sense Output
26	S3′	Synchro S3 Remote Sense Output
27	NC	No connection.
28	GND	Ground
29	−15V	Power Supply
30	+15V	Power Supply
31	$\overline{LA}$	2nd Latch All Enable. Input enables dual latch.
32	$\overline{LL}$	1st Latch LSBs Enable. Enables bits 9-16.
33	$\overline{LM}$	1st Latch MSBs Enable. Enables bits 1-8.
34	RL′	3.4Vrms Reference Low Input
35	RH′	3.4Vrms Reference High Input
36	−R (TP)	No connection. Factory test point.
37	$\overline{EN}$	Enable. Power stage enable input allows for digital shutdown of power stage. Gives complete control of converter to digital system.
38	$\overline{BS}$	Battle Short Input. Logic "0" overrides over-temperature protection.
39	$\overline{BIT}$	Built-In-Test Output. Logic "0" when loss of reference, loss of ±15VDC supply, case temperature of +140°C, EN input signal, an output over-current or short circuit has been detected. Power output stage is turned off unless $\overline{BS}$ is at "0".
40	$\overline{K}$	Kick. Input used for reducing continual short-circuit current flow in torque receiver loads at false null.



Notes:

1. Dimensions are in inches (millimeters).
2. Lead identification numbers for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-883, Method 2003.

FIGURE 2. DSC-10510 AND DSC-10511 MECHANICAL OUTLINE 40 PIN (TDIP)

ORDERING INFORMATION

DSC-10510-30X

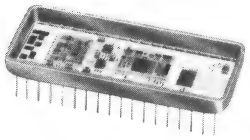
- Accuracy:
  - 3 = ±4 minutes
  - 4 = ±2 minutes
  - 5 = ±1 minutes
- Reliability Grade:
  - 0 = Standard DDC procedures.
  - 1 = Fully compliant with MIL-STD-883
  - 2 = Screened to MIL-STD-883 but without QCI testing
- Operating Case Temperature:
  - 3XX = 0° C to +70° C
  - 1XX = −55° C to +125° C
- Configuration:
  - 0 = Standard
  - 1 = S2 Grounded (Consult factory).

For DSC-10510 use optional Power Transformer, DDC P/N 42359.
For DSC-10511 use optional Power Transformer, DDC P/N 42360.

D

DSC-11520

16 BIT HYBRID D/S AND D/R CONVERTER
Pin Programmable For Synchro or Resolver Output



DESCRIPTION

The DSC-11520 is a versatile multiplying digital-to-analog converter. The digital input represents angle and the output is pin programmable either for resolver type sin/cos or for three-line synchro output. The reference input will accept any waveform, even a sawtooth for CRT drive. Because the reference is DC coupled to the output, the DSC-11520 can be used in many configurations:

With a synchro or resolver reference input, the DSC-11520 is a digital-to-synchro or digital-to-resolver converter.

With a DC reference input, the unit can be used as a hybrid digital-to-sin/cos DC converter.

With the reference input proportional to the radius vector, the DSC-11520 converts polar to rectangular coordinates.

With a sawtooth reference input and a rotating digital input, the module can generate a cartwheel rotating sweep for PPI displays.

Packaged in a 36 pin double DIP, the DSC-11520 is a complete D/S and D/R converter in one hybrid module.

Hybrid technology results in low weight, low power consumption, very high reliability, and a wider operating temperature range. A new, improved circuit design allows higher accuracy and reduces the output scale factor so that the output can drive displays directly. The output line-to-line voltage can be scaled by external resistors. Other features include high AC and DC common mode rejection at the reference input and output short circuit protection.

APPLICATIONS

Because of its high reliability, small size and low power consumption, the hybrid DSC-11520 is ideal for the most stringent and severe industrial and military ground or avionics applications. All units are available with MIL-STD-883 processing as a standard option.

Among the many possible applications are computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, fire control systems, radar and navigation systems, and PPI displays including moving target indicators.

FEATURES

- *COMPLETE D/S and D/R CONVERTER*
- *ACCURACY: TO ±1 MIN.*
- *0.05% SCALE FACTOR VARIATION WITH ANGLE*
- *DC COUPLED REFERENCE ACCEPTS ANY WAVEFORM*
- *GENERATES SIN/COS DC OR ROTATING PPI SWEEP*
- *HIGH REL CMOS D/R CHIP*
- *8 BIT/2 BYTE DOUBLE BUFFERED TRANSPARENT LATCHES*

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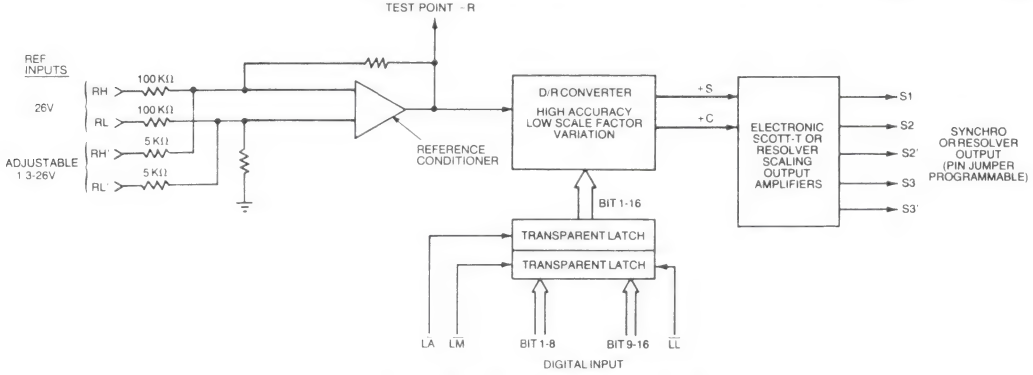


FIGURE 1. DSC-11520 BLOCK DIAGRAM

SPECIFICATIONS
Apply over temperature range, power supply ranges, reference voltage and frequency range and 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 bits
ACCURACY AND DYNAMICS	
Output Accuracy	±8 minutes, to ±1 min. (See Ordering Info).
Differential Linearity	±1 LSB max
Output Settling Time	Less than 20 μsec for any digital step change.
DIGITAL INPUT	
Logic Type	Natural binary angle, parallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected. Each input has a 20μa max pull down to GND.
Logic Voltage Level	Logic 0 = 0 to +1.25V Logic 1 = 2V to 5V
Load Current	20μa max to GND (bit 1-16) 20μa to V_L ($\overline{LL}$, $\overline{LM}$, $\overline{LA}$) See Timing Diagram (Fig. 2).
REFERENCE INPUT	
Type	Two differential solid state inputs, one for standard 26V input and one programmable.
Frequency Range	DC to 1000Hz (to 10 KHz with reduced accuracy)
Voltage	Standard Input: 26V ±10% Programmable Input: 1.3V min for full output; higher voltages are scaled by adding two series resistors
Input Impedance	
Single Ended	Standard Input: 100KΩ ±0.5% Programmable Input: 5KΩ ±0.5%
Differential	Standard Input: 200KΩ ±0.5% Programmable Input: 10KΩ ±0.5%
ANALOG OUTPUT	
Type	Pin programmable for synchro or resolver mode
Output Current	2mA rms max
Max Output Voltage (Tracks Reference Input Voltage)	11.8V rms L-L ±0.25% nominal in synchro mode 6.81V rms L-L ±0.25% nominal resolver mode
Transformation Ratio Tol.	±0.2% max
Scale Factor Variation	±0.05% max
DC Offset Each Line to Gnd	±15mV standard. Varies with input angle ±5mV available—Consult Factory
Short Circuit Protection	Fully protected
POWER SUPPLIES	
Voltage	+15V −15V
Voltage Limits	±5% ±5%
Max Voltage Without Damage	±18V −18V
Current or Impedance	20 mA max 20 mA max +5V logic levels are derived internally
TEMPERATURE RANGES (CASE)	
Operating	
−1 Option	−55°C to +125°C
−3 Option	0°C to +70°C
Storage	−55°C to +135°C
PHYSICAL CHARACTERISTICS	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)
Weight	0.85 oz (24g)

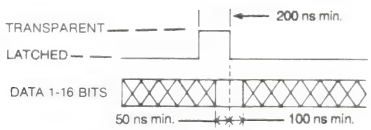


FIGURE 2. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

As shown in the block diagram, the signal conversion in the DSC-11520 is performed by a high accuracy digital to resolver converter whose sin and cos outputs have a low scale factor variation as a function of the digital input angle. This resolver output is either amplified by scaling amplifiers for resolver output, or is both amplified and converted to a synchro output by an electronic Scott-T. In both cases, the output line currents are limited to 2 mA rms max, which is sufficient for driving S/D converters, solid state control-transformers, and displays. Output power amplifiers will be required, however, for driving electro-mechanical devices such as synchros and resolvers.

The reference conditioner has a differential input with high AC and DC common mode rejection, so that a reference isolation transformer will seldom be required. There are two sets of reference inputs. The RH, RL input provides the maximum synchro or resolver output voltage for a standard 26V rms reference input. The RH', RL' input is used to scale the output for other reference voltage levels. Series resistors can be added to the reference input as described below either to accommodate lower reference levels for full output, or to reduce the output level.

The reference conditioner output -R is intended for test purposes. A signal between 6V and 7.5V at -R indicates that a reference input signal is present.

OUTPUT SCALING AND REF. LEVEL ADJUSTMENT

The DSC-11520 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage.

The maximum line-to line levels are determined by the output amplifiers and are nominally 11.8V for synchro output and 6.81V for resolver output. The RH, RL reference input is designed to provide this nominal output for the standard 26V reference level. The scaling adjustment is made by two internal 100 KΩ resistors in series with the reference conditioner input (see DSC-11520 Block Diagram). The maximum output levels without distortion are 10% greater than the nominal 11.8V and 6.81V levels.

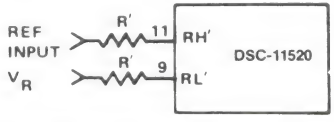


FIGURE 3. REF. LEVEL ADJUSTMENT

The RH', RL' reference input has only 5 KΩ internal resistors in series with the reference conditioner input, so that nominal line-to-line output is obtained for a reference input of 1.3V. For higher reference voltages, two resistors R' must be inserted in series with the inputs as shown in Figure 3. These resistors scale the DSC-11520 outputs

down to the nominal 11.8V and 6.81V levels stated above, or to lower voltages if desired. The magnitude of the resistors R′ in ohms is calculated as follows:

$$R' = \frac{5000}{1.3}(V_R - 1.3)\left(\frac{\text{NOMINAL L-L VOLTAGE LEVEL}}{\text{DESIRED L-L VOLTAGE LEVEL}}\right)$$

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

Synchro output

S1 — S3 = (RH-RL) A_o (1 + A(θ)) sin θ

S3 — S2 = (RH-RL) A_o (1 + A(θ)) sin (θ +120°)

S2 — S1 = (RH-RL) A_o (1 + A(θ)) sin (θ +240°)

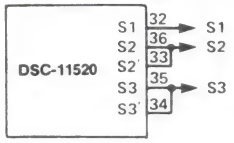
Resolver output

S1 — S3 = (RH-RL) A_o (1 + A(θ)) sin θ

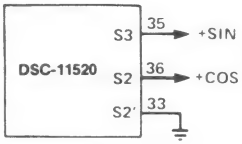
S2 — S4 = (RH-RL) A_o (1 + A(θ)) cos θ

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The transformation ratio A_o is 11.8/26 for 11.8V rms L-L output. The maximum variation in A_o from all causes is ±0.2%. The term A (θ) represents the variation of the amplitude with the digital input angle. A (θ), which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.05% for all values of θ. The total maximum variation in A_o (1 + A(θ)) is therefore ±0.25%.

Because the amplitude factor (RH-RL) A_o (1 + A(θ)) varies simultaneously on all output lines, it will not be a source of error when the DSC-11520 is to drive a ratiometric system such as a synchro or resolver. However, if the outputs are used independently, as in X-Y plotters, the amplitude variations must be taken into account.



11.8V SYNCHRO OUTPUT



6.81V RESOLVER OUTPUT

OUTPUT PIN PROGRAMMING

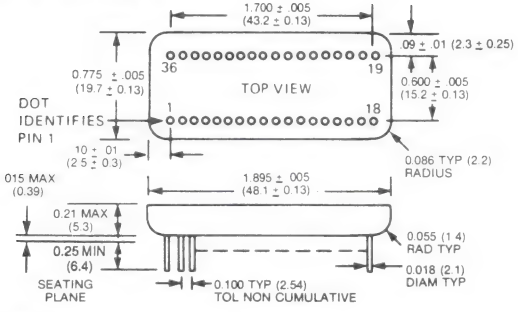
PIN CONNECTION TABLE

Pin	Name	Pin	Name	Pin	Name
1	NC	13	BIT 13	25	BIT 1 (MSB)
2	+15V	14	BIT 12	26	BIT 15
3	GND	15	BIT 11	27	BIT 16 (LSB)
4	−15V	16	BIT 10	28	$\overline{LM}$
5	NC	17	BIT 9	29	$\overline{LL}$
6	NC	18	BIT 8	30	$\overline{LA}$
7	-R	19	BIT 7	31	NC
8	RL	20	BIT 6	32	S1
9	RL′	21	BIT 5	33	S2′
10	RH	22	BIT 4	34	S3′
11	RH′	23	BIT 3	35	S3 (+SIN)
12	BIT 14	24	BIT 2	36	S2 (+COS)

NOTES:

1. -R (PIN 7) can be used for test purposes to detect whether a reference signal is present. See block diagram.
2. Functions $\overline{LL}$, $\overline{LA}$ and $\overline{LM}$ may be left unconnected when not used.
3. V_L (PIN 6) may be left unconnected where 5V logic levels are used.

MECHANICAL OUTLINE
36 PIN DOUBLE DIP



NOTES

1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.010 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

ORDERING INFORMATION

DSC-11520 — 3 0 2

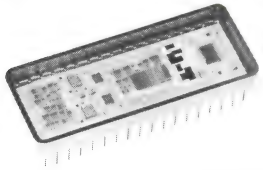
Accuracy
- 2 = ±8 minutes
- 3 = ±4 minutes
- 4 = ±2 minutes
- 5 = ±1 minute

Reliability Grade
- 0 = Standard DDC Processing
- 1 = Fully compliant with MIL-STD-883
- 2 = Screened to MIL-STD-883 but without QCI testing.

Operating Temperature Range:
- 1 = -55°C to 125°C (Case)
- 3 = 0°C to +70°C (Case)

DDC
ILC DATA DEVICE CORPORATION

DSC-11524



16 BIT HYBRID D/S and D/R CONVERTER Pin Programmable for Synchro or Resolver Output

PRELIMINARY

DESCRIPTION

The DRC-11524 is a versatile multiplying digital-to-analog converter. The digital input represents angle, and the output is pin programmable either for resolver type, sin/cos, or for three-line synchro output. The reference input will accept any waveform, even a sawtooth for CRT drive. Because the reference is dc coupled to the output the DSC-11524 can be used in many configurations; such as,

With a sinusoidal reference input, the DRC-11524 is a digital-to-synchro or resolver converter.

With a dc reference input, the unit can be used as a hybrid digital-to-sin/cos dc converter.

With the reference input proportional to the radius vector, the DRC-11524 converts polar to rectangular coordinates.

With a sawtooth reference input and a rotating digital input, the module can generate a cartwheel rotating sweep for PPI displays.

Packaged in a 36 pin DDIP, the DSC-11524 is a complete D/S and D/R converter in one hybrid module.

Hybrid technology results in low weight, low power consumption, very high reliability, and a wide operating temperature range. A new, improved circuit design allows higher accuracy and reduces the output scale factor variation so that the output can drive displays directly. The output line-to-line voltage can be scaled by external resistors. Other features include high ac and dc common mode rejection at the reference input, and output short circuit protection.

APPLICATIONS

Because of its high reliability, small size and low power consumption, the hybrid DSC-11524 is ideal for the most stringent and severe industrial and military ground or avionics applications. All units are available with 883B processing as a standard option.

Among the many possible applications are computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, fire control systems, radar and navigation systems, and PPI displays including moving target indicators

FEATURES

- *15mA RMS Output*
- *11.8$V_{L\text{-}L}$ Synchro, 11.8$V_{L\text{-}L}$ Resolver, or 6.81$V_{L\text{-}L}$ Resolver Output*
- *8 Bit/2 Byte Double Buffered Transparent Latches*
- *Pin Programmable for Synchro or Resolver Output*
- *16 Bit Resolution*
- *Complete D/S and D/R Converter*
- *Accuracy: To ±1 Min.*
- *0.05% Scale Factor Variation with Angle*
- *DC Coupled Reference Accepts Any Waveform*
- *Generates Sin/Cos DC or Rotating PPI Sweep*
- *High Rel CMOS D/R Chip*
- *No +5V supply*

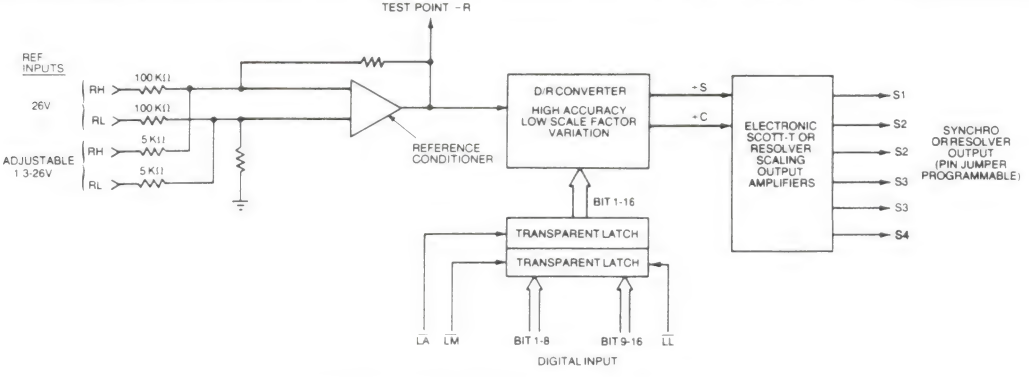


FIGURE 1. DSC-11524 BLOCK DIAGRAM

TABLE 1. DSC-11524 SPECIFICATIONS

Apply over temperature range, power supply range, reference voltage and frequency range, and 10% harmonic distortion in the reference.

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	16	
ACCURACY and DYNAMICS			
Output Accuracy	Minutes	± 8 to ±1 min. (See Ordering info.)	
Differential Linearity	LSB	±1 max	
Output Settling Time	µsec	Less than 20 for any digital step change.	
DIGITAL INPUT			
Logic Type		Natural binary angle, parrallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected. Logic 0 = 0 to +1.25V Logic 1 = +2V to +5V	
Load Current	µA	20 max to GND (bits 1-16) 20 max to +5V ($\overline{LL}$, $\overline{LM}$, $\overline{LA}$) See Timing Diagram (Figure 2.).	
REFERENCE INPUT			
Type		Two differential solid-state inputs: one for standard 26V, one programmable.	
Frequency Range	Hz	DC to 1k (to 10k with reduced accuracy)	
		Standard Input	**Programmable Input**
Voltage	V	26 ±10%	1.3 min for full output; higher voltages are scaled by adding two series resistors
Input Impedance			
■ Single Ended	k ohm	100 ± 0.5%	5 ± 0.5%
■ Differential	k ohm	200 ± 0.5%	10 ± 0.5%
ANALOG OUTPUT			
Type		Pin programmable for synchro or resolver	
Output Current	mA rms	15 max	
Output Voltage		(Tracks Reference Input Voltage)	
■ Synchro mode	$Vrms_{L-L}$	11.8 nominal	
■ Resolver mode	$Vrms_{L-L}$	6.81 or 11.8 nominal	
Transform. Ratio Tol.	%	± 0.2 max	
Scale Factor Variation	%	± 0.05 max	
DC Offset (Each Line to Gnd)	mV	± 15 max. Varies with input angle.	
Short-circuit Protection		Fully protected	
POWER SUPPLIES			
Voltage	V	+15 ± 5%	−15 ± 5%
Max voltage without damage		**+18V**	**− 18V**
Current or Impedance	mAmax	35+ load current	35+ load current
TEMPERATURE RANGES (CASE)			
Operating			
■ −1 Option	°C	−55 to +125	
■ −2 Option	°C	0 to +70	
Storage	°C	−55 to +135	
PHYSICAL CHARACTERISTICS			
Type		36 pin DDIP	
Size	in.(mm)	0.78 x 1.9 x 0.21 (19.7 x 48.1 x 5.3)	
Weight	oz (g)	0.85(24)	

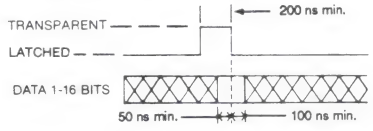


FIGURE 2. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

As shown in the block diagram, the signal conversion in the DSC-11524 is performed by a high-accuracy digital-to-resolver converter whose sin and cos outputs have a low scale factor variation as a function of the digital input angle. This resolver output is either amplified by scaling amplifiers for resolver output, or is both amplified and converted to a synchro output by an electronic Scott-T. In both cases the output line currents can be 15mA rms max, which is sufficient for driving S/D converters, solid-state control-transformers, and displays. Output power amplifiers will be required, however, for driving electromechanical devices such as synchros and resolvers.

The reference conditioner has a differential input with high ac and dc common mode rejection, so that a reference isolation transformer will seldom be required. There are two sets of reference inputs. The RH, RL input provides the maximum synchro or resolver output voltage for a standard 26V rms reference input. The RH', RL' input is used to scale the output for other reference voltage levels. Series resistors can be added to the reference input as described below, either to accommodate lower reference levels, or to reduce the output level.

The reference conditioner output –R is intended for test purposes. A signal between 6V and 7.5V at –R indicates that a reference input signal is present.

OUTPUT SCALING AND REF. LEVEL ADJUSTMENT

The DRC-11524 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage.

The maximum line-to-line levels are determined by the output amplifiers and are nominally 11.8V for synchro output and 6.81 V or 11.8V for resolver output. The RH, RL reference input is designed to provide this nominal output for the standard 26V reference level. The scaling adjustment is made by two internal 100k ohm resistors in series with the reference conditioner input (see DSC-11524 Block Diagram). The maximum output levels without distortion are greater than the nominal 11.8V and 6.81V levels.

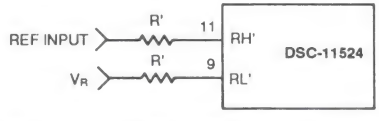


FIGURE 3. REF. LEVEL ADJUSTMENT

The RH', RL' reference input has only 5k ohm internal resistors in series with the reference conditioner input, so that nominal line-to-line output is obtained for a reference input of 1.3V. For higher reference voltages, two resistors, R', must be inserted in series with the inputs as shown in Figure 3. These resistors scale the DSC-11524 outputs down to the nominal 11.8V and 6.81V levels stated above, or to lower voltages if desired. The magnitude of the

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resistors, R', in ohms is calculated as follows:

$$R' = \frac{5000}{1.3}(V_R - 1.3)\left(\frac{\text{Nominal L–L Voltage Level}}{\text{Desired L–L Voltage Level}}\right)$$

OUTPUT PHASING AND OUTPUT SCALE FACTOR

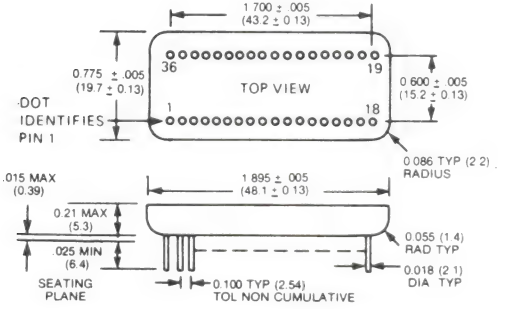
The analog output signals have the following phasing:

Synchro output:
S3 — S1 = (RH - RL)A_o(1 + A(θ)) sin θ
S2 — S3 = (RH - RL)A_o(1 + A(θ)) sin(θ + 120°)
S1 — S2 = (RH - RL)A_o(1 + A(θ)) sin(θ + 240°)

Resolver output:
S3 — S1 = (RH - RL)A_o(1 + A(θ)) sin θ
S2 — S4 = (RH - RL)A_o(1 + A(θ)) cos θ

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (RH - RL). The transformation ratio A_o is 11.8/26 for 11.8 Vrms L-L output. The maximum variation in A_o from all causes is ± 0.2%. The term A(θ) represents the variation of the amplitude with the digital signal input angle. A(θ), which is called the scale factor variation, is a smooth function of (θ) without discontinuities and is less than ± 0.05% for all values of (θ). The total maximum variation in A_o(1 + A(θ)) is therefore ± 0.25%

Because the amplitude factor (RH - RL)A_o(1 + A(θ)) varies simultaneously on all output lines, it will not be a source of error when the DRC-11524 is to drive a ratiometric system such as a synchro or resolver. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.



NOTES
1. dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

FIGURE 4. DSC-11524 MECHANICAL OUTLINE 36 PIN DDIP

A

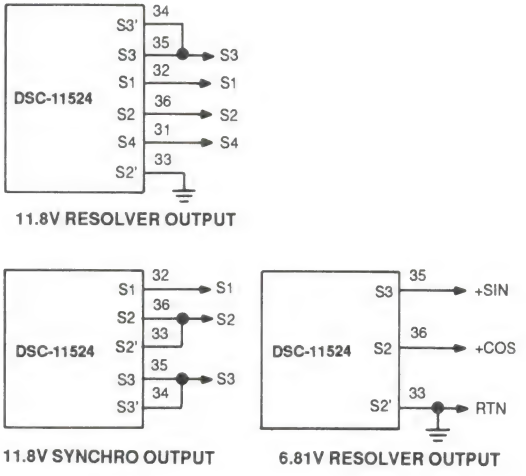


FIGURE 5. OUTPUT PIN PROGRAMMING

TABLE 2. PIN CONNECTION TABLE

PIN	NAME	PIN	NAME	PIN	NAME
1	NC	13	Bit 13	25	Bit 1 (MSB)
2	+15V	14	Bit 12	26	Bit 15
3	GND	15	Bit 11	27	Bit 16 (LSB)
4	– 15V	16	Bit 10	28	$\overline{LM}$
5	NC	17	Bit 9	29	$\overline{LL}$
6	NC	18	Bit 8	30	$\overline{LA}$
7	– R	19	Bit 7	31	S4
8	RL	20	Bit 6	32	S1
9	RL'	21	Bit 5	33	S2'
10	RH	22	Bit 4	34	S3'
11	RH'	23	Bit 3	35	S3 (+SIN)
12	Bit 14	24	Bit 2	36	S2 (+COS)

Notes:
1. – R (PIN 7) can be used for test purposes to detect whether a reference signal is present. See block diagram.
2. Functions $\overline{LL}$, $\overline{LA}$, and $\overline{LM}$ may be left unconnected when not used.
3. V_L (PIN 6) may be left unconnected where 5V logic levels are used.

ORDERING INFORMATION

DSC- 11524 - X X X

Accuracy:
2 = ±8 minutes
3 = ±4 minutes
4 = ±2 minutes
5 = ±1 minutes

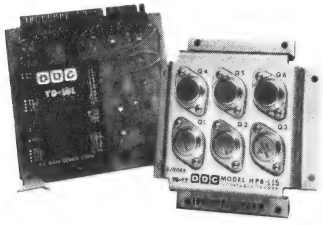
Reliability:
0 = Standard DDC procedures
1 = 883B Processing
2 = 883B Processing but without QCI testing

Operating Temperature Range:
1 = -55 to +125°C (Case)
3 = 0 to +70°C (Case)

DDC
ILC DATA DEVICE CORPORATION

TD-100 AND TD-101*

12 BIT HIGH POWER D/S TORQUE DRIVER
Fully Protected Output



DESCRIPTION

The TD-100 and TD-101 are torque drivers which accept digital angle input and produce a high power 3-line synchro output. This output can drive torque receivers or multiple CT or CDX loads. A complete unit has either of the following two configurations:

TD-100: A PC card containing both the D/S converter and an output power-buffer designed for convection cooling. Drive capability is 3 amps peak.

TD-101: A PC card containing the D/S converter and a separate output power-buffer which can be bolted to a chassis for conductive cooling. Drive capability is either 4 or 15 amps peak, depending on choice of buffer.

In addition, separate isolation transformers are available for both the synchro output and the reference input.

The TD-100 and TD-101 incorporate special features which protect them against overloading and which allow them to be computer-controlled in a sophisticated fashion to conserve power. A current sense, a thermal sense, and a voltage transient clamp protect the TD-100 and TD-101 against overloads, stalled rotor conditions, inductive kickback, and power supply loss. All units contain logic controls which can be used to switch the output off to conserve power, or to switch it on to continue operation in spite of thermal overload under battle short conditions. To warn when operating conditions are not normal, a fault indicator goes to logic 1 whenever the thermal or current sense indicates overload, or when the disable is applied.

APPLICATIONS

The TD-100 and TD-101 are rugged units, requiring no calibrations or adjustments. They are used in training simulators, remote indicators, gun fire control, and shipboard retransmission systems. Their power conserving features recommend them especially for installations requiring multiple units, and their control features are designed for computer supervision.

FEATURES

- *VIRTUALLY INDESTRUCTIBLE:*
  PROTECTED AGAINST SHORT CIRCUITS, OUTPUT OVERLOADING, THERMAL OVERLOAD, VOLTAGE TRANSIENTS, AND POWER SUPPLY SHUTDOWN
- *OUTPUT:*
  DESIGNED TO DRIVE BOTH CT OR CDX PASSIVE LOADS AND TORQUE RECEIVERS
  DIRECTLY COUPLED 11.8V L-L OUTPUT
  WITH OUTPUT ISOLATION TRANSFORMERS: 400 Hz AT 11.8V L-L, AND 60 Hz OR 400 Hz AT 90V L–L
  PEAK POWER UP TO 108 VA
- *ACCURACY:*
  ±21 MINUTES, FULL LOAD
  ±10 MINUTES, NO LOAD
- *LOGIC:*
  TTL COMPATIBLE
  PARALLEL BINARY ANGLE INPUT WITH STORAGE REGISTER
  OUTPUT CAN BE ENABLED OR DISABLED
  FAULT INDICATOR
- *POWER REQUIRED: ±15V DC AND +5V DC*

*Patented

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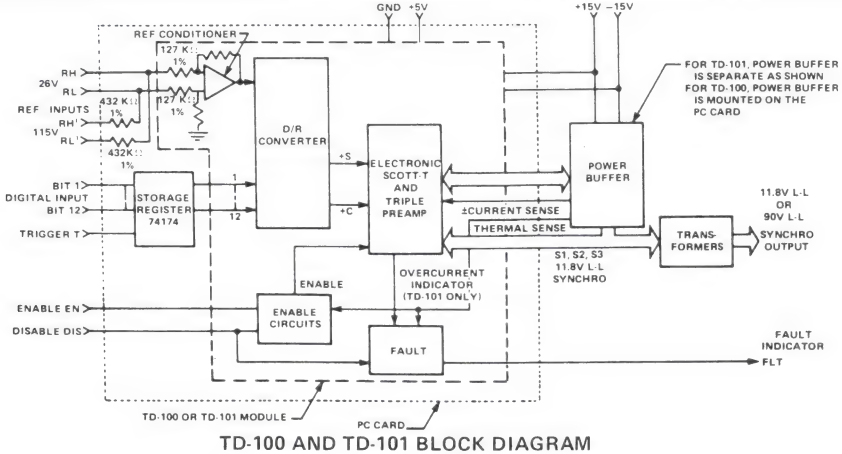

TD-100 AND TD-101 BLOCK DIAGRAM

SPECIAL FEATURES

Current Limiting. The card mounted power buffer and the HPB power buffer both contain a current sense which is used to limit the output current. The limiting value is the peak transient output power listed in the specifications.

Thermal Sense. If the thermal sense in the power buffer heat sink indicates a temperature exceeding 125°C, the enable circuits will shut off the triple amplifier output until the temperature drops below 125°C. The Fault Indicator will also be activated to indicate a fault.

Fault Indicator. The Fault Indicator signals when the output is off because of thermal overload or because the disable has been applied. In the TD-101, it also signals when the current has exceeded 2/3 of the peak transient current level.

Disable. The Disable shuts down the output. It can be used to conserve power when the output is not needed. When several torque drivers are used, the Disable lines can be used to sequence turn-on so that a smaller power supply is required.

Enable. This control line overrides the thermal sense so that operation can continue in spite of a thermal overload.

Voltage Transient Clamp. The buffer output stage is protected against voltage transients caused by inductive kickback from the load.

Power Supply Shutdown Protection. The power buffer will shut down if any of the power supplies is shut off or disconnected.

TECHNICAL INFORMATION

OUTPUT PHASING AND SCALE FACTOR

The AC amplitudes of the synchro output lines can be described as follows:

$$S1 - S3 = A_0\ (1 + A(\theta)(RH\text{-}RL)\sin\theta\sin\omega t$$
$$S3 - S2 = A_0\ (1 + A(\theta)(RH\text{-}RL)\sin(\theta + 120^\circ)\sin\omega t$$
$$S2 - S1 = A_0\ (1 + A(\theta)(RH\text{-}RL)\sin(\theta + 240^\circ)\sin\omega t$$

The scale factor, $A_0\ (1 + A(\theta)(RH\text{-}RL)$, is proportional to the reference voltage (RH-RL). The angular independent term A_0 is accurate to within ±2%. In addition, there is an angular dependence expressed by the scale factor variation $A(\theta)$. $A(\theta)$ is ±8% for the TD-100, but only ±1% for the TD-101 because the D/R converter within the TD-101 module has an inherently low scale factor variation. The scale factor variation will not cause errors in situations where the outputs are used ratiometrically as, for instance, to drive synchros.

SPECIFICATIONS

Apply over temperature range, power supply range, ±10% reference voltage and frequency variation, and ±10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	12 bit binary angle input
ACCURACY (All Causes, Balanced Load)	±21 minutes full load ±10 minutes no load

DIGITAL INPUT/OUTPUT (TTL Compatible)

Digital Inputs	
12 Parallel Data Bits	Natural binary angle; positive logic
Trigger (T)	Trigger for card-mounted storage register for input data bits Triggers on positive edge
Disable (DIS)	Logic 1 or open: Shuts down the output Logic 0 or GND: Normal operation
Enable (EN)	Logic 1 or open: Overrides thermal cutout Logic 0 or GND: Allows thermal cutout to operate normally
Fault Indicator Output (FLT)	Logic 0: normal operation Logic 1: indicates any of the following three conditions: (1) Thermal overload (trip point = 125°C) (2) Disable (DIS) is at logic 1 so that the output is shut down (3) Current overload for TD-101 (not for TD-100). Trip point is at approximately 2/3 of peak current setting. For the HPB-14, the trip point is about 2.7A, which corresponds to 20 VA output. For the HPB-115, the trip point is about 10A, corresponding to 75 VA output.

Loading or Drive Capability	Logic Type	Loading (STD TTL)	Pullup To +5V (Nominal)	Voltage Levels or Logic 0 Current
12 Parallel Data Bits				
TD-100 Module or Card	TTL	1		
TD-101 Module	CMOS		33 KΩ	logic 0 ≤ 1V logic 1 ≥ 1V less than +5V supply
TD-101 Card Mounted	TTL	1		
Trigger (Card Mtd Units Only)	TTL	2		
Disable and Enable				
TD-100	TTL	1		
TD-101	LS	0.2		
Fault Indicator				
TD-100			6 KΩ	6.4 mA
TD-101			4.7 KΩ	3.2 mA

REFERENCE INPUT

Frequency Range	47–440 Hz, solid state differential input
Voltage Levels	26V rms or 115V rms, separate inputs

Minimum Input Impedance (Balanced, Resistive)

	Differential	Single Ended
26V Input	260 KΩ	130 KΩ
115V Input	1100 KΩ	550 KΩ

Common Mode Range (DC level plus recurrent AC peak)	
26V Input	50V rms
115V Input	250V rms

TD-100 AND TD-101*

PARAMETER	VALUE		
SYNCHRO OUTPUT			
Voltage Level			
L-L Voltage	11.8V direct output		
	11.8V or 90V transformer output		
	Output voltage level tracks reference level		
Scale Factor	±2% max compared to nominal 11.8V or 90V		
Scale Factor Variation			
TD-100	±8% max variation with angle		
TD-101	±1% max variation with angle		
Output Power	CMA and CMB	HPB-14	HPB-115
Peak Transient	25W	32W	125W
Steady State	8 VA	20 VA	30 VA
Transformer Parameters	Transformer Number	Input Imped. Z_{SO} Min	Output Imped. Z_{SS} Max
For CMA and HPB-14 Options			
360–440 Hz, 90V rms L-L	18884	50Ω	40Ω
360–440 Hz, 11.8V rms L-L	18883	100Ω	1.0Ω
57–63 Hz, 90V rms L-L	18885	100Ω	110Ω
For HPB-115 Options			
360–440 Hz, 90V rms L-L	24748	60Ω	20Ω
57–63 Hz, 90V rms L-L	22638	12Ω	15Ω
Input Voltage, All Transformers	11.8V rms L-L		
POWER SUPPLIES			
Voltage	+15V±5%	−15V±5%	+5V±5%
Max Voltage Without Damage	+18V	−18V	+7V
Current	65 mA + load	40 mA + load	150 mA
Max Continuous Current			
CM and CMA Options	1A	1A	
HPB-14	2.5A	2.5A	
HPB-115	3.6A	3.6A	
Current Limiting			
CM and CMA Options	3A peak	3A	
HPB-14	4A	4A	
HPB-115	15A	15A	
THERMAL CHARACTERISTICS			
Temperature Ranges			
Operating (PC Card and Transformer Ambient; HPB Chassis Temperature)			
−1	−55°C to +85°C		
−3	0°C to +70°C		
Storage	−55°C to +125°C		
Heat to be Dissipated	2.5 Watts per VA delivered		
Thermal Resistance at Junction of Power Transistor and Heat Sink			
CM and CMA Options	7°C/Watt, with natural convection		
HPB-14	2°C/Watt, conduction cooling		
HPB-115	1.7°C/Watt, conduction cooling		
PHYSICAL CHARACTERISTICS			
PC Card, Options 100CM and 100CMA			
Size	5.38 x 5.26 x 0.73 high inch (13.7 x 13.4 x 1.9 cm)		
Weight	8 oz (227 g)		
PC Card Option 101CMB			
Size	5.38 x 5.26 x 0.65 high inch (13.7 x 13.4 x 1.7 cm)		
Weight	12.5 oz (355 g)		
HPB-14 and HPB-115 Buffer			
Size	5 x 5 x 1.35 inch (12.7 x 12.7 x 3.4 cm)		
Weight	11 oz (312 g)		
Transformers	See Mechanical Outline drawings		

DRIVING TORQUE RECEIVERS

A torque driver must have a peak transient output power capacity sufficient to drive a torque receiver to null, as well as enough steady state power capability to maintain the torque receiver at null. The various TD-100 and TD-101 models can drive the following torque receiver loads:

MAXIMUM TORQUE RECEIVER LOAD CAPABILITIES

Model	Output		Max Load (Z_{SS})
TD-100CM	Direct Output	11.8V, 400 Hz	1Ω
TD-100CMA or TD-101CMB with HPB-14	Transformer	11.8V, 400 Hz	1Ω
		90V, 400 Hz	50Ω
		90V, 60 Hz	100Ω
TD-101CMB With HPB-115	Transformer	90V, 400 Hz	6.5Ω
		90V, 60 Hz	15Ω

Some common torque receivers and their Z_{SS} (stator input impedance with rotor shorted) are listed in the following table.

SOME COMMON TORQUE RECEIVERS AND THEIR LOAD IMPEDANCES

Synchro	V_{L-L}/freq. (Hz)	Z_{SS}(Ω)
26V – 11TR4c	11.8V/400	3.3 to 4.2
11TR4c	90V/400	180 to 250
15TRx4a	90V/400	50 to 82
15TRx6a	90V/60	920
18TRx4a	90V/400	16 to 21
18TRx6b	90V/60	350 to 430
23TR6	90V/60	110 to 145
23TR6a	90V/60	110 to 145
23TRx4a	90V/400	6.5 to 8.1
23TRx6b	90V/60	110 to 145

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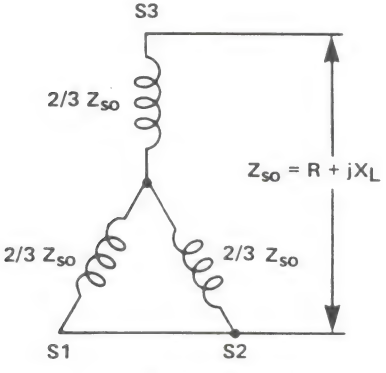
DRIVING CT AND CDX LOADS

When driving CT and CDX loads the torque driver must have enough steady state power capability to drive the Z_{SO} of the load. Z_{SO} (stator impedance with rotor open-circuited) is measured as shown in the diagram:



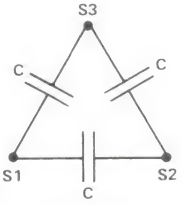
Z_{SO} MEASUREMENT

The following table shows the load impedance of some typical control transformers.

SOME COMMON CONTROL TRANSFORMERS AND THEIR LOAD IMPEDANCES

Military Type Number	Size	Z_{SO}
26V 08CT4c	08	100 + j490
26V 11CT4d	11	21 + j132
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1670 + j11883
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Three capacitors may be placed across the legs of the synchro stator in a delta configuration:

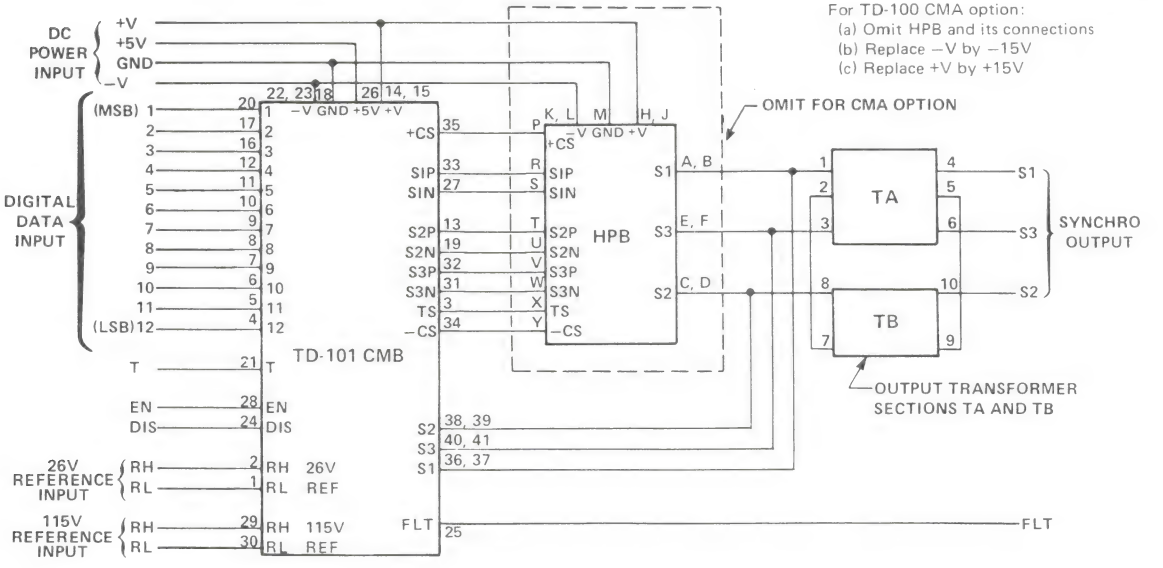


DELTA TUNING CONFIGURATION

INTERCONNECTION DIAGRAM FOR CMA AND CMB OPTIONS

Note:
Connect as shown for TD-101 CMB option.

For TD-100 CMA option:
(a) Omit HPB and its connections
(b) Replace −V by −15V
(c) Replace +V by +15V



The correct value of the capacitance C in Farads is given by:

$$C = \frac{X_L}{4\pi f Z_{SO}} = \frac{X_L}{4\pi f\,(R^2 + X_L{}^2)}$$

where f is the carrier frequency and R and X_L are the real and reactive components of Z_{SO}. Good grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel, because the load impedance Z is increased to:

$$Z = \frac{Z_{SO}}{R} = \frac{R^2 + X_L{}^2}{R}$$

FALSE NULL

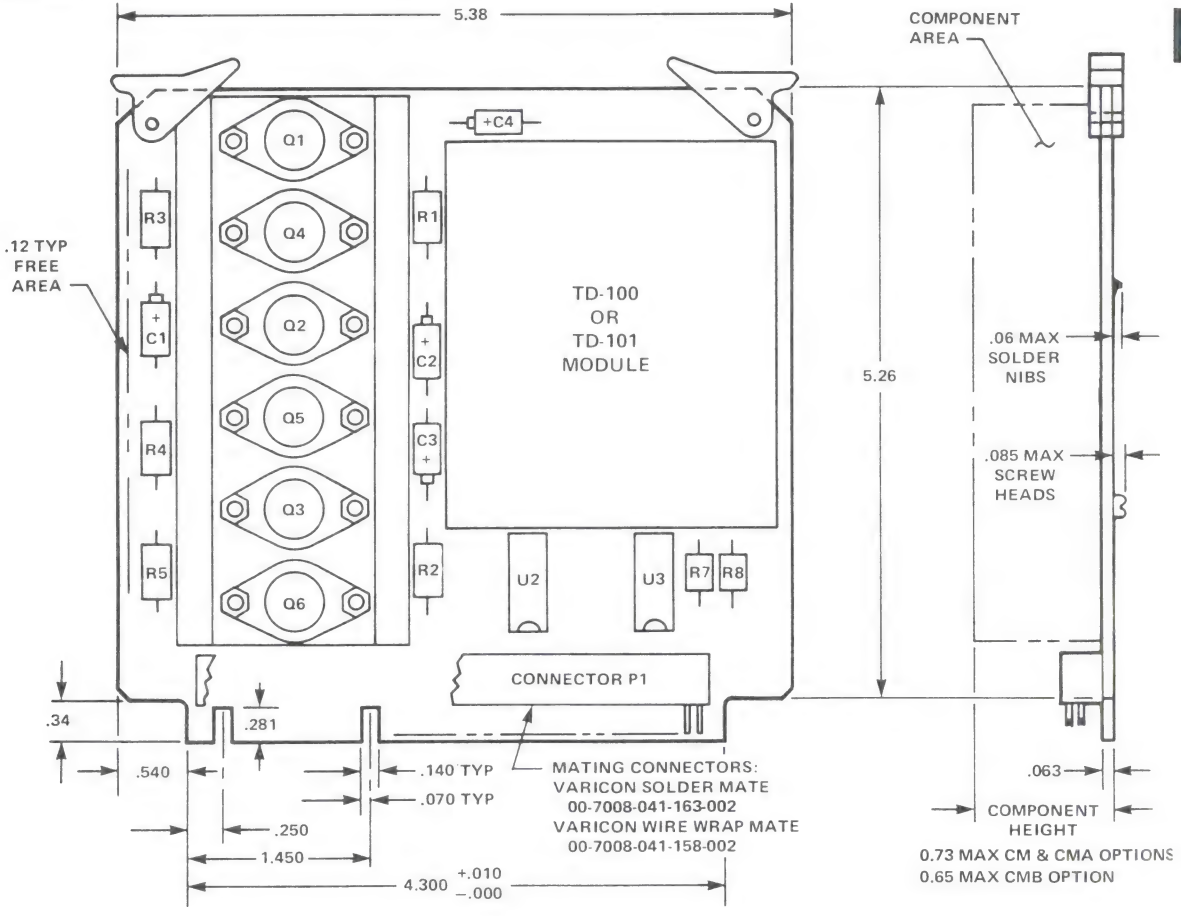
A hang-up condition can occur in a torque receiver or a servo if the rotor is exactly 180° away from the true null. The restoring torque is a sinusoidal function of angle and goes to zero 180° away from the true angle. This is a false null and if there were a finitie error signal the rotor would be driven back toward the true null. The TD-100/101 output angle can change 180° in less than 100 μsec, which is much faster than the electromechanical rotor response. Therefore the digital angle should never be changed 180° in a single step.

TRANSIENTS

Minor transients occur each time the data angle changes. They last for approximately 100 μsecs and usually do not cause any error, since the bandwidth of the driven servo filters them out.

PC CARD MECHANICAL OUTLINE

The diagram below shows the location of all components as on the CM option.
For option CMA the output resistors R3, R4, R5 are omitted.
For option CMB resistors R1, R2, R3, R4, R5 and the heat sink with Q1 to Q6 are omitted.



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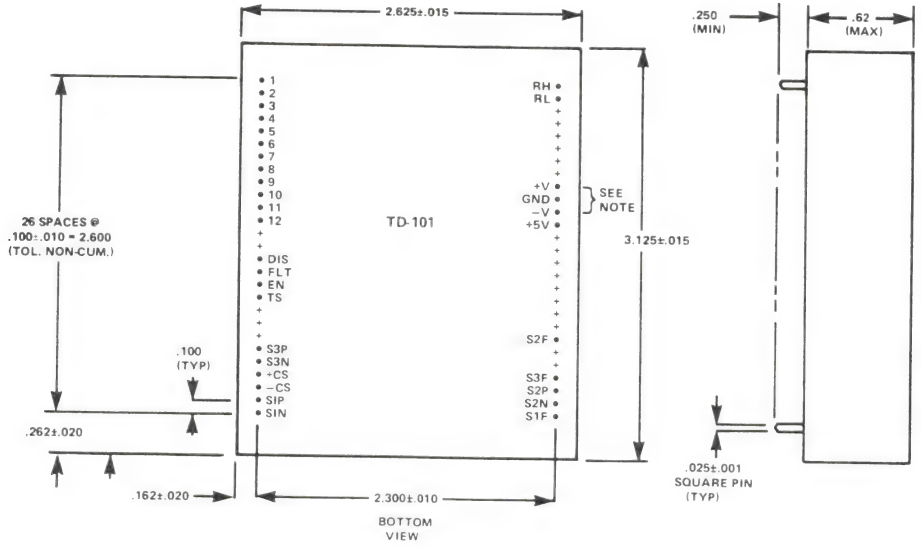
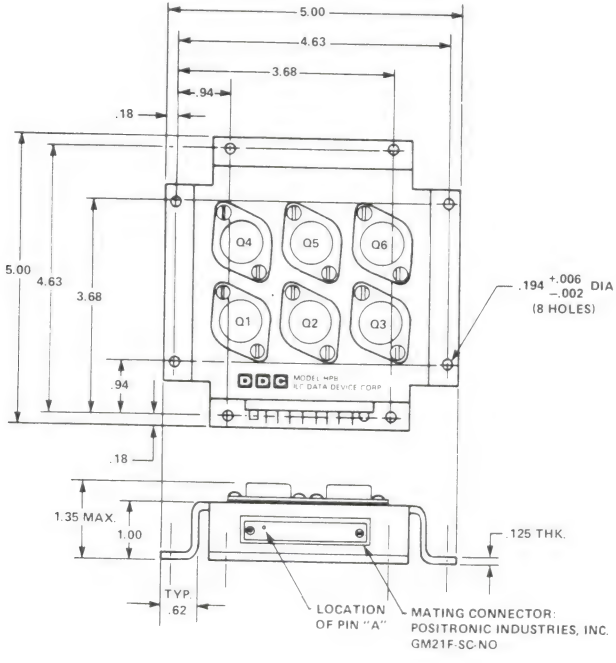
MECHANICAL OUTLINE, TD-100 AND TD-101 MODULES



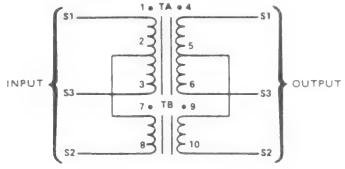
NOTES:
1. The TD-100 module has the same mechanical outline except that pin +V is +15V and pin −V is −15V.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
3. Pins meet solderability requirements of MIL-STD-202E, Method 208C.

MECHANICAL OUTLINE, HIGH POWER BUFFER, HPB-14 OR HPB-115



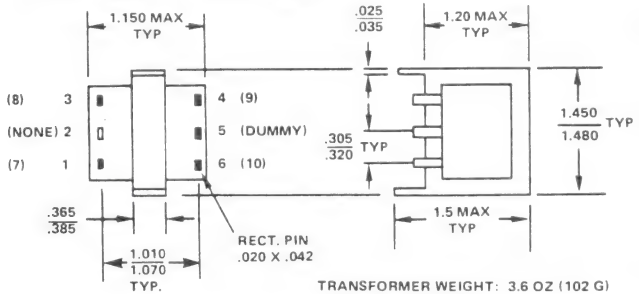
OUTPUT TRANSFORMERS DIAGRAMS

1. Schematic Diagram For all Output Transformers 18883, 18884, 18885, 24748 and 22638



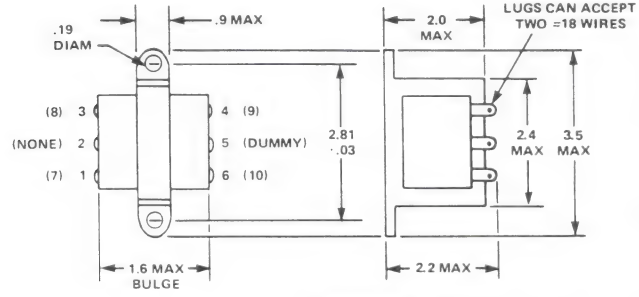
2. Mechanical Outlines
   Each output transformer has two sections, TA and TB. Both sections have the same physical dimensions, but pin designations are different. In the following diagrams, pin designations without parenthesis refer to section TA (pins 1 through 6) and pin designations with parenthesis refer to section TB (pins 7 through 10.)

TRANSFORMERS 18883 AND 18884



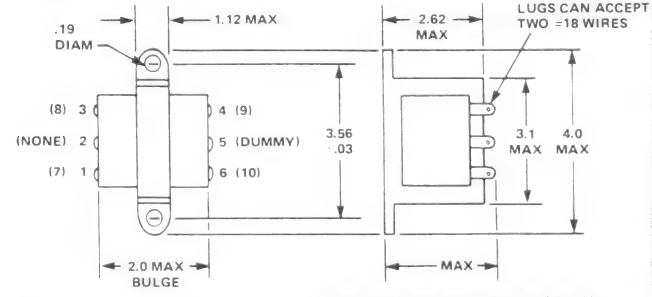
TRANSFORMER WEIGHT: 3.6 OZ (102 G)

TRANSFORMERS 18885 AND 24748



TRANSFORMER WEIGHT: 15.1 OZ (428 G)

TRANSFORMER 22638



TRANSFORMER WEIGHT: 33.2 OZ (942 G)

C

ORDERING INFORMATION

1. Order the basic torque driver or replacement modules as follows. Transformers and remote high power buffers must be ordered separately as described below in parts 2 and 3. All card mounted units are supplied with a mating connector.

TD – 101CMB – 1

Operating Temperature Ranges (Ambient):
1 = –55°C to +85°C
3 = 0°C to +70°C

Type:

100	=	TD-100 replacement module only
101	=	TD-101 replacement module only
100CM	=	Card mounted TD-100 module with card mounted medium power buffer. Includes three 1Ω output resistors. Unit is not intended for output transformers.
100CMA	=	Card mounted TD-100 module with card mounted medium power buffer. Output resistors are not included. Unit is intended for output transformers, which must be ordered separately below.
101CMB	=	Card mounted TD-101 module intended for separate remote medium or high power buffer. Order buffer and transformers separately below.

2. The high power buffer for the CMB option must be ordered separately as follows. These buffers are supplied with a mating connector. (See below for output transformers.)

HPB – 14 – 1

Temperature Range (chassis):
1 = –55°C to +85°C
3 = 0°C to +70°C

Output current:
14 = 4 amperes current limiting
115 = 15 amperes current limiting

3. Output transformer pairs for CMA and CMB options must be ordered separately as follows. A pair of transformers is supplied for each part number.

L-L Voltage	Frequency	Part Number	
		CMA or HPB-14	HPB-115
11.8V	360–440 Hz	18883	–
90V	360–440 Hz	18884	24748
90V	57–63 Hz	18885	22638

Reference isolation transformers are also available. Consult factory for information.

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SECTION G
SYNCHRO AND RESOLVER INSTRUMENTS

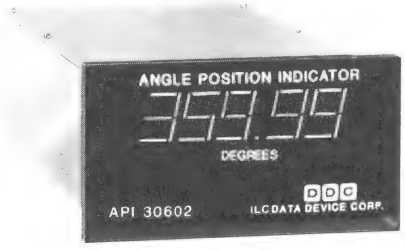
PRODUCT SUMMARY TABLE

	MODEL	FUNCTION	RESOLUTION	ACCURACY	PACKAGE	DESCRIPTION/FEATURES	PAGE
	API-30602	Synchro Indicator	0.001°	to ±0.03°	3.8 x 2 x 7.5" Panel Meter	Low cost, pin programmable for all common inputs, bright 0.43" display, tri-state output, offset adjust for system zeroing. 47-1200Hz.	G-2
*	**API-36005**	Synchro/ Resolver Angle Indicator	20/16 bits Programable	18 arc sec	Full Size IBM PC ® Card	Reference signal of either 26 or 115 Vrms. Synchro/ Resolver Signals of 11.8, 26, or 90 Volts L-L. Fully transformer isolated. Input frequency range of 360 Hz to 5000 Hz. Built-in single angle self-test feature for confidence testing.	G-6
	HSR-103/203	Synchro Indicator	0.001°	±0.005°	1.7" High (103) 3.5" High (203) 1/2 Rack	Wideband 47-1000 Hz, automatic gain ranging, bit fault Monitor, synthesized reference, programmable 0-360° or ± 180°, IEEE-488 option.	G-35/39
*	**IAC-37001**	Synchro Simulator & Indicator	20/16 bits Programable	18 arc sec	VXI 'C' size card 9.2 x 13.4 x 1.2"	Instrument on **A C**ard. Combines the capabilities of both the HSR-203 and SIM-31200 on one card.	G-12
	MSR-236	2 Speed Synchro indicator	0.01°	±0.01°	12 x 9.6 x 4.8" Combination Case	Converts single or dual (1:36 or 2:36) speed synchro or resolver signals to BCD angle. Transformer isolation. MIL-T-21200 case.	G-20
	SIM-31200	Angle Simulator	0.001°	to ±0.003°	14.5 x 8.12 x 3.47" Instrument	Synchro or resolver angle simulator with high accuracy, wide band operation (47Hz to 11kHz). Front panel keyboard programmable (local mode), standard parrallel I/O, or optional IEEE-488 I/O (remote mode).	G-23
*	**SIM-36010**	Synchro/ Resolver Angle Simulator	16 bits	25 arc sec	Full Size IBM PC ® Card	26 or 115 Vrms Reference signal.Synchro or Re- solver output signals at 11.8, 26, or 90 Volts L-L. Drive capability of 1.5 VA. Programmable Dynamic Rotation feature CW or CCW from 0.17°/sec up to 30.5 rps. External Rate Clock and Direction signals provisions for nonlinear motion. Has demo software.	G-28
	SR-103/203	Synchro Indicator	0.01°	±0.03°	1.7" High (103) 3.5" High (203) 1/2 Rack	0.01° version of HSR-103/203.	G-35/39

NOTES: Most hybrid products are available with Military Processing (Contact Factory).
® IBM PC is a registered trademark of International Business Machines.
* New Product

API-30602*

0.01° LOW COST TRACKING SYNCHRO AND RESOLVER PANEL METER



DESCRIPTION**

The API-30602 is a small, low cost 5 decade (.01° resolution) synchro/resolver angle indicator. It can be pin programmed to accept synchro or resolver signals at 2, 11.8, 26 or 90V line-to-line. Its broadband (47-1200 Hz) frequency capability and three-state BCD output, for use with a microprocessor data bus, makes the API-30602 a versatile instrument. The unit is available in two accuracy grades: ±0.05° (standard unit) and ±0.03° (high accuracy).

The synchro/resolver to digital tracking converter (Figure 1) is the heart of the panel meter. Using a type II servo loop for continuous tracking, the API-30602 has no velocity lag up to ±180°/sec.

Standard features include ±2° offset adjust, which is convenient for system alignment and lamp test capability for display testing. An optional dimmer control is available for applications requiring varying display intensities. The API-30602 requires no field adjustment or calibration.

APPLICATIONS

The API-30602 can be used wherever accurate angle information is required for display, control, testing purposes or computation. Applications include production testing of synchros and resolvers, information translators in quality control systems, machine tool control, ship and aircraft navigation systems, and antenna positioning.

**API-30604/05/08/09 units are usable only in resolver mode with the 6V reference input provided by the panel meter.

FEATURES

- *VERSATILE: ACCEPTS ALL STANDARD SYNCHRO AND RESOLVERS*
- *±2° ZERO ADJUST FOR SYSTEM ALIGNMENT*
- *RESOLUTION: 0.01° ACCURACY: ±0.05° OR ±0.03°*
- *TYPE II SERVO TRACKING LOOP*
- *3-STATE OUTPUT FOR MICRO-PROCESSOR DATA BUS*
- *OPTIONAL DIMMER CONTROL*
- *SHAFT ANGLE TRANSDUCER OPTION*

*Patented

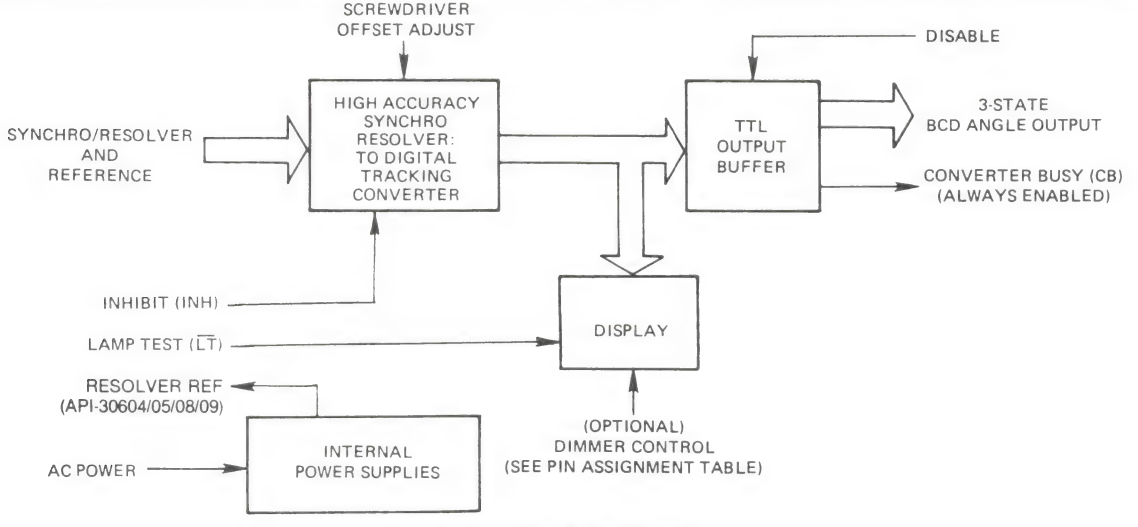


FIGURE 1. BLOCK DIAGRAM

API-30602*

SPECIFICATIONS

PARAMETER	VALUE			
MODEL	API-30602 and API-30603	API-30604 and API-30605	API-30606 and API-30607	API-30608 and API-30609
RESOLUTION	0.01° (5 BCD Digits)	0.01° (5 BCD Digits)	0.01° (5 BCD Digits)	0.01° (5 BCD Digits)
ACCURACY				
Standard	±0.05°	±0.05°	±0.05°	±0.05°
Hi Accuracy	±0.03°	±0.03°	±0.03°	±0.03°
REPEATABILITY	Within 0.01°	Within 0.01°	Within 0.01°	Within 0.01°
ANGLE RANGE (Continuous Rotation)	0° to 359.99°	0° to 359.99°	0° to 359.99°	0° to 359.99°
DISPLAY 7 Segments 0.43 inch LED	5 Digits	5 Digits	5 Digits	5 Digits
REFERENCE INPUT (Solid State)				
Voltage	10 to 126V rms	6V rms	10 to 126V rms	6V rms
Frequency	47 to 1200Hz	47 to 63Hz	47 to 1200Hz	47 to 63Hz
Impedance	148KΩ min, Single Ended 296KΩ min, Differential	148KΩ min, Single Ended 296KΩ min, Differential	148KΩ min, Single Ended 296KΩ min, Differential	148KΩ min, Single Ended 296KΩ min, Differential
Harmonic Content	±10% max	±10% max	±10% max	±10% max
SIGNAL INPUT				
Input Type	Synchro or Resolver, Transformer Isolated	Resolver, Direct/Single Ended	Synchro or Resolver, Transformer Isolated	Resolver, Direct/Single Ended
Voltage Level (L-L)	11.8, 26 or 90V rms ±10%	2V rms ±10%	11.8, 26 or 90V rms ±10%	2V rms ±10%
Frequency	47 to 1200Hz	47 to 63Hz	47 to 1200Hz	47 to 63Hz
Allowable Phase Shift	±10° Relative to Ref	NA	±10° Relative to Ref	NA
Input Impedance	Resistive Balanced, Transformer Isolated 170KΩ min (Resolver) 148KΩ min (Synchro)	10M Ω min	Resistive Balanced, Transformer Isolated 170KΩ min (Resolver) 148KΩ min (Synchro)	10M Ω min
Breakdown Voltage	500V min to logic ground	NA	500V min to logic ground	NA
DYNAMIC CHARACTERISTICS				
Tracking Rate	180°/sec min			
Settling Time (To 1 LSB) for 179° Step	3 sec			
Open Loop Transfer Function	$G = \frac{18.6^2\left(\frac{S}{9}\right)+1}{S^2\left(\frac{S}{90}\right)+1}$			
DIGITAL INPUTS (TTL Compatible)				
Loading	0.5 std TTL loads max (0.8 mA)			
Inhibit (1NH)	"1" or open = track "0" or GND = inhibit			
Lamp Test (LT)	"1" or open = normal operation "0" or GND = all LED segments on			
Disables	"1" or open = three state outputs high impedance "0" or GND = enable			
DIGITAL OUTPUTS (TTL COMPATIBLE)				
Drive Capability	Three state, 10 TTL loads (16 mA)			
Synchro or Resolver Angle	Parallel data bits; BCD angle; positive logic, 5 decades 18 lines and one common ground line.			
Converter Busy (CB)	4 to 10 usec positive pulse; counts on leading edge			
POWER INPUT				
Voltage	115V / 26V	115V	220V / 100V	220V / 100V
Frequency	47 to 440Hz / 360 to 440Hz	47 to 63 Hz	47 to 440 Hz / 47 to 440Hz	47 to 63Hz / 47 to 63Hz
Current	70 mA / 0.3 A	70 mA	35 mA / 80 mA	37 mA / 80 mA
Isolation	Transformer Isolated	Transformer Isolated	Transformer Isolated	Transformer Isolated
Power	9VA max, 6.5VA typ	9VA max, 6.5VA typ	9VA max, 6.5VA typ	9VA max, 6.5VA typ
Breakdown Voltage	1000VDC min to logic ground	1000VDC min to logic ground	1000VDC min to logic ground	1000VDC min to logic ground
TEMPERATURE RANGE				
Operating	0°C to +70°C			
Storage	−65°C to +125°C			
PHYSICAL CHARACTERISTICS				
Size (see mechanical outline)	2.03 X 3.84 X 7.50 inch (52 X 98 X 191 mm)			

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PIN ASSIGNMENTS

PIN	API-30602	API-30603	API-30604	API-30605	API-30606	API-30607	API-30608	API-30609
1	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd
2	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd
3	Connect to 27 for 26V L-L		NC	NC	Connect to 27 for 26V L-L		NC	NC
4	Converter Busy		Converter Busy		Converter Busy		Converter Busy	
5	Connect to 27 for 11.8V L-L		NC	NC	Connect to 27 for 11.8V L-L		NC	NC
6	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo
7[1]	6V AC Ref Hi Out		6V AC Ref Hi Out		6V AC Ref Hi Out		6V AC Ref Hi Out	
8	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi
9	NC	NC	NC	NC	NC	NC	NC	NC
10	.1	.1	.1	.1	.1	.1	.1	.1
11	.01	.01	.01	.01	.01	.01	.01	.01
12	.2	.2	.2	.2	.2	.2	.2	.2
13	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
14	.4	.4	.4	.4	.4	.4	.4	.4
15	.02	.02	.02	.02	.02	.02	.02	.02
16	.8	.8	.8	.8	.8	.8	.8	.8
17	100	100	100	100	100	100	100	100
18	.04	.04	.04	.04	.04	.04	.04	.04
19	S3'	S3'	NC	NC	S3'	S3'	NC	NC
20	Disable .1° Decade		Disable .1° Decade		Disable .1° Decade		Disable .1° Decade	
21	NC	NC	NC	NC	NC	NC	NC	NC
22	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd
23	200	200	200	200	200	200	200	200
24	8	8	8	8	8	8	8	8
25	Disable 100° Decade		Disable 100° Decade		Disable 100° Decade		Disable 100° Decade	
26	20	20	20	20	20	20	20	20
27	L-L Programming		S1, S4 (Resolver Input) (-Sin, -Cos)		L-L Programming		S1, S4 (Resolver Input) (-Sin, -Cos)	
28	4	4	4	4	4	4	4	4
29	.08	.08	.08	.08	.08	.08	.08	.08
30	40	40	40	40	40	40	40	40
31	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option
32	2	2	2	2	2	2	2	2
33	Disable .01° Decade		Disable .01° Decade		Disable .01° Decade		Disable .01° Decade	
34	80	80	80	80	80	80	80	80
35	+5V Dimmer Option		+5V Dimmer Option		+5V Dimmer Option		+5V Dimmer Option	
36	1	1	1	1	1	1	1	1
37	$\overline{LT}$ (Lamp Test)		$\overline{LT}$ (Lamp Test)		$\overline{LT}$ (Lamp Test)		$\overline{LT}$ (Lamp Test)	
38	10	10	10	10	10	10	10	10
39	S	S	NC	NC	S	S	NC	NC
40	Disable 1° Decade		Disable 1° Decade		Disable 1° Decade		Disable 1° Decade	
41	S1 (Synchro/Resolver Input)		NC	NC	S1 (Synchro/Resolver Input)		NC	NC
42	Disable 10° Decade		Disable 10° Decade		Disable 10° Decade		Disable 10° Decade	
43[2]	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo
44	S3 (Synchro/Resolver Input)		S3 (+Sin/Resolver Input)		S3 (Synchro/Resolver Input)		S3 (+Sin/Resolver Input)	
45	26V Power Hi	26V Power Hi	26V Power Hi	26V Power Hi	100V Power Hi	100V Power Hi	100V Power Hi	100V Power Hi
46	S4 (Resolver Only)		NC	NC	S4 (Resolver Only)		NC	NC
47	115V Power Hi	115V Power Hi	115V Power Hi	115V Power Hi	220V Power Hi	220V Power Hi	220V Power Hi	220V Power Hi
48	S2 (Synchro/Resolver Input)		S2 (Resolver Input: +Cos)		S2 (Synchro/Resolver Input)		S2 (Resolver Input: +Cos)	
49	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd
50	SS	SS	NC	NC	SS	SS	NC	NC

Notes:

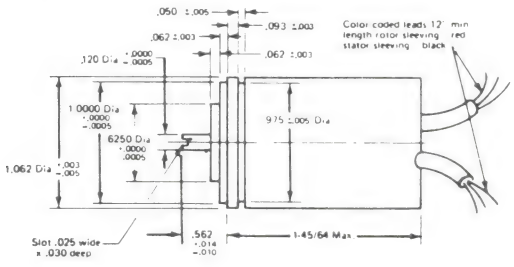
(1) Used only for API-30604/8 and -30605/9.

(2) Chassis Gnd (Pin 1,2 or 49) should be connected to Digital Gnd (pin 22) and then to Earth Ground.

(3) Connections required for optional operating configurations are described in our API-30602 Series Instruction Manual

SHAFT ANGLE TRANSDUCER OPTION

API-30604/05/08/09 are dedicated units to be operated at 2V line-line resolver signal. The reference input of 6V to the resolver is provided by the panel meter. Any standard 400 Hz, 26V/12.6V or 26V/11.8 resolver can be used. A standard 6 minute resolver is available from DDC: Order P/N 521000140000



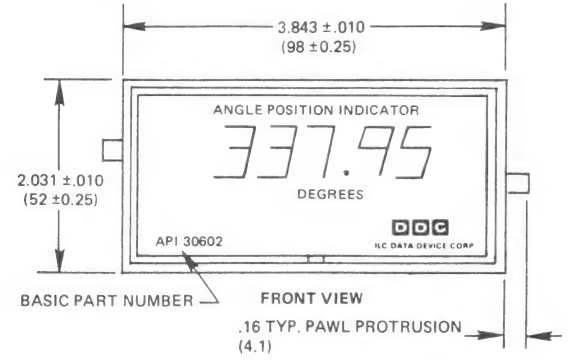
RESOLVER CONNECTION TABLE FOR API-30604/05/08/09

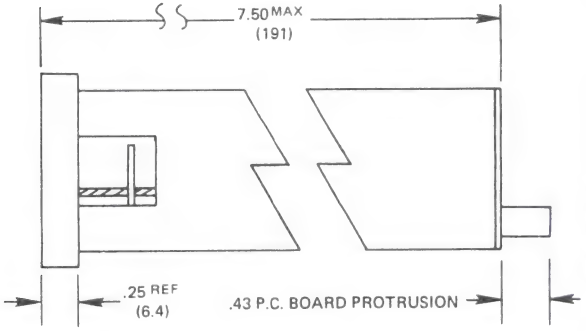
RESOLVER LEADS		PANEL METER CONNECTOR	
SYMBOL	COLOR	CONNECT TO PIN NO.	FUNCTION
R1	RED/WHITE	JUMPER 7	6V HI
R3	BLACK/WHITE	JUMPER 8	REF HI
R2	YELLOW/WHITE	JUMPER 43	POWER LO
		JUMPER 6	REF LO
S1	RED	27	-SIN
S2	YELLOW	48	+COS
S3	BLACK	44	+SIN
S4	BLUE	27	-COS

NOTE: This connection is for CCW rotation of the resolver for increasing angle sense. For CW rotation, representing increasing angle, interchange S1 and S3.

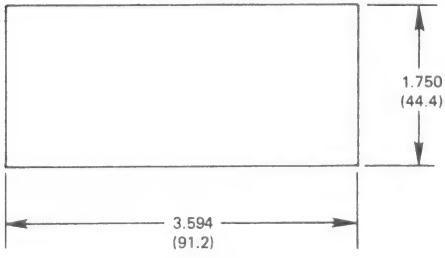
MECHANICAL OUTLINE

NOTE: Dimensions are in inches (millimeters)





SIDE VIEW

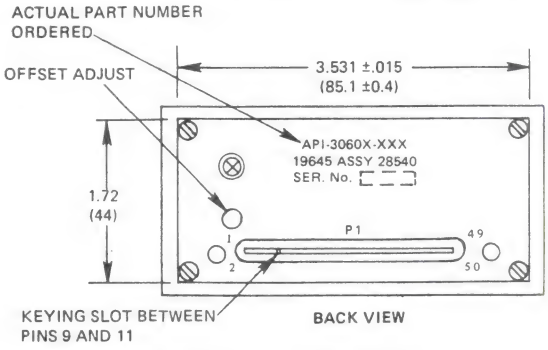


MOUNTING CUTOUT

MOUNTING PROCEDURE

1. Cut out mounting hole.
2. Removing lens: insert screwdriver into notch at the bottom of the bezel and gently pry out lens.
3. Insert Panel Meter into cutout.
4. Retract pawls to rear position by turning screws counter clockwise.
5. Lock Panel Meter into position by turning screws clockwise.
6. Replacing lens: Slightly bend lens and snap into side channels of bezel.

D



ORDERING INFORMATION

API – 3060X – 3 0 X

- Accuracy:
  - 1 = ±0.05°
  - 2 = ±0.03°
- Input:
  - 0 = Standard
- Temperature Range (operating):
  - 3 = 0°C to +70°C
- Options:
  - 2 = 115V Standard
  - 3 = 115V Dimmer option
  - 4 = 115V Transducer option (note 3)
  - 5 = 115V Dimmer and transducer options
  - 6 = 220V Standard
  - 7 = 220V Dimmer option
  - 8 = 220V Transducer option (note 3)
  - 9 = 220V Dimmer and transducer option
- Family Code

NOTES:

1. All instruments are supplied with mating connector, keying plug, and connector locking hardware.
2. Additional connectors and keying plugs may be ordered as P/N 28841.
3. Standard 6 minute resolver for use with API-30604/05 /08/09 may be ordered separately as P/N 15760.

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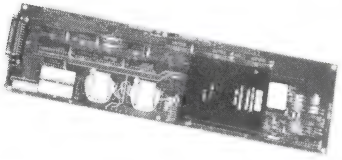
SYNCHRO/RESOLVER ANGLE INDICATOR IBM PC® CARD INSTRUMENT



PRELIMINARY

DESCRIPTION

The API-36005 is a full size IBM PC card containing a broadband, high-accuracy instrumentation grade Synchro/Resolver Angle Position Indicator. The indicator accepts a Reference signal of either 26 Vrms or 115 Vrms, along with Synchro/Resolver Signals of 11.8, 26, or 90 Volts Line-to-Line, and converts these signals into 16 or 20 bits of binary angular information. The Reference and Synchro/Resolver input signals are fully transformer isolated and can accept signals over the frequency range of 360 Hz to 5000 Hz. The API-36005 contains a built-in single angle self-test feature for confidence testing.

Demonstration software, which shows the API-36005 capabilities is available with the card.

APPLICATIONS

The API-36005 is a versatile high-accuracy Synchro/Resolver Angle Position Indicator instrument for IBM PC based test systems. Data to-and-from the instrument is more than an order-of-magnitude faster than conventional IEEE bus test systems, because the card plugs directly into the PC bus structure. It is ideal for use as a stand-alone angle indicator in the engineering lab or as part of the PC based automatic test equipment (ATE).

FEATURES

- ***Accuracy of ±18 ARC Seconds in 20-Bit Mode***
- ***Programmable Resolution of 16 or 20 Bits***
- ***Broadband Operating frequency 360 Hz to 5000 Hz***
- ***Fully Transformer Isolated***
- ***Tracking Rate of 1040 Deg/Sec in 16-Bit Mode, 65 Deg/Sec in 20-Bit Mode***
- ***Loss-Of-Reference and Tracking Status Bits***

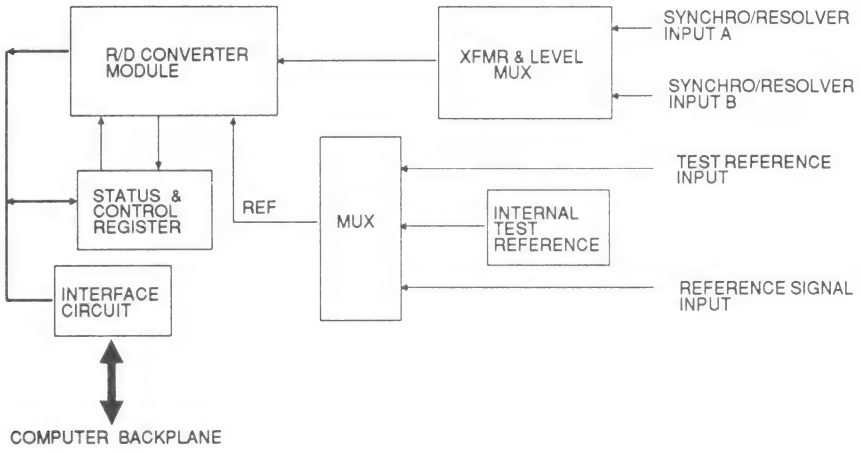


FIGURE 1. API-36005 BLOCK DIAGRAM

TABLE 1. API-36005 SPECIFICATIONS		
PARAMETER	**UNIT**	**VALUE**
RESOLUTION	Bits	20/16 programmable
ACCURACY	Arc Sec.	18 in 20-Bit Mode 36 in 16-Bit Mode
ANGULAR RANGE	Degrees	0 to 360
REFERENCE INPUT		
Type		transformer isolated
Voltage Range	Vrms	26 or 115 -40/+20%
Frequency	Hz	360 - 5,000
Input Impedance	Ohm	100k min
Breakdown Voltage	V	500 min.
Harmonic Content	%	10
SIGNAL INPUT		
Type		transformer isolated
Format		synchro or resolver
Voltages L-L	V L-L	11.8, 26, or 90 ±10%
Frequency	Hz	360 to 5,000
Phase Shift	Deg	± 50 max Rel to Ref
Input Impedance	Ohm	150k min.
Breakdown Voltage	V	500 min.
DYNAMIC CHARACTERISTICS		
Tracking Rate		
16-Bit Mode	Deg/Sec	1,040 min.
20-Bit Mode	Deg/Sec	65 min.
Settling Time	sec	0.5 max
PROGRAMMABLE FEATURES		
L-L Voltage Input	V_{L-L}	11.8, 26, or 90
Ref Level ()	Vrms	115 or 26
Synchro/Resolver	—	—
Resolution	Bits	20 or16
Inhibit (Freeze Measurement)	—	—
Channel	—	A or B
POWER SUPPLIES	V	+5V, 550mA max +12V, 150mA max
TEMPERATURE RANGE		
Operating	°C	0 to +50
Storage	°C	-25 to +85

INTRODUCTION

The API-36005 is a full size IBM PC card which contains a broadband instrument grade Synchro/Resolver-to-Digital converter. The instrument accepts either a 26 Vrms or a 115 Vrms Reference along with 11.8, 26, or 90 Volt Line-to-Line Synchro or Resolver signals, and converts this information into a 16 bit or 20 bit binary word. The Indicator can track the Synchro/Resolver input signals at rates up to 1040 degrees/second in the 16-bit mode and 65 degrees/second in the 20-bit mode. Both the Reference and the Synchro/Resolver inputs are fully transformer isolated and can accept signals over the frequency range of 360Hz to 5000Hz.

A conversion Inhibit feature allows the computer to freeze the angular position during the time it takes to read out the digital angular position data. The Inhibit can also be used to time synchronize angular data with external events, or to synchronize several instruments together if they are in the same computer.

Two fault signals are generated within the Instrument. The $\overline{BIT}$ status signal indicates that the converter is no longer tracking the Synchro/Resolver input. This condition can occur if a step input is applied to the tracking converter, or if the Synchro/Resolver input is rotating faster than the maximum allowable tracking rate. The Loss-of-Reference ($\overline{LOR}$) status bit indicates that the input Reference signal is missing or too low.

The API-36005 generates an internal 45 Degree angle for use in self-test.

A block diagram for the API-36005 is shown in Figure 1.

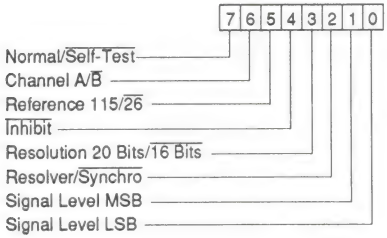
INTERNAL REGISTERS

REGISTER ADDRESSING

The API-36005 is I/O addressed in typical Base Address and Offset fashion and uses 8 contiguous bytes of memory in the I/O address space. To decode these 8 bytes requires the use of the three LSBs of the I/O address. The remaining 7 address lines are used for setting the Base Address via a DIP switch located on the circuit card assembly. The Base Address of the card is preset at the factory to HEX address 300. In this configuration the card will occupy the address space of 300h to 307h. Table 4 shows the DIP switch settings as the card leaves the factory. The base address can be changed to any address from 000h to 3F8h in increments of 8 using Table 4 as a reference. Table 2 contains a I/O Memory Map of the API-36005.

TABLE 2.				
A2	**A1**	**A0**	**I/O Write**	**I/O Read**
0	0	0	NOT USED	NOT USED
0	0	1	NOT USED	NOT USED
0	1	0	NOT USED	NOT USED
0	1	1	NOT USED	NOT USED
1	0	0	CONTROL WORD	CONTROL WORD
1	0	1	NOT USED	BITS 17-20 & FAULT
1	1	0	NOT USED	BITS 9-16
1	1	1	NOT USED	BITS 1-8 (MSBs)

CONTROL WORD BIT MAP

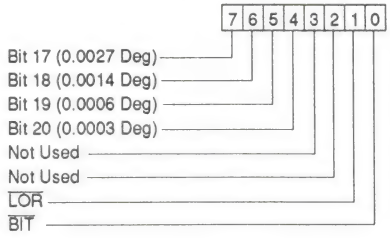


- Normal/Self-Test - A logic high for this bit connects the RH and RL reference input to the converter section of the instrument. A logic low for this bit selects the Test Reference input supplied externally.
- Channel A/B - The API-36005 can accept two independent Synchro/Resolver signal sources i.e., channel A and channel B. This bit is used to select the desired channel. A logic high selects channel A and a logic low selects channel B. Channel A contacts are normally open and channel B contacts are normally closed.
- Reference 115/26 - This bit is used to select the input Reference level. A logic high configures the converter to accept a 115 Vrms Reference signal and a logic low configures the converter to accept a 26 Vrms Reference signal.
- Inhibit - A logic high for this bit enables the converter to track the input synchro/resolver signal. A logic low causes the converter to freeze at the angular position present during the high to low transition of the Inhibit bit. When reading the angular position information from the API-36005 it is necessary set this bit low before reading the three bytes of angular data in order freeze the angular reading. The Inhibit bit should be set back to a logic high as soon as possible so that the converter can reacquire and track the synchro/resolver input signal. This bit can also be used to time synchronize the instrument to external events, or to synchronize several Synchro/Resolver Indicator cards in multichannel test systems.
- Resolution 20 Bits/16 Bits - There is a tradeoff between tracking rate and angular resolution i.e., for a constant angular rate each additional bit of resolution will have to track at twice the frequency of the previous bit. For this reason the API-36005 has two tracking ranges. A logic high for this bit will provide 20 binary bits of angular resolution at rates up to 65 degrees/second, and a logic low for this bit will provide 16 bits of angular resolution at rates up to 1040 degrees/second.
- Signal Level Select - These two signal select bits (MSB and LSB) select the Line-to-Line voltage level for the Synchro/Resolver input signals. Additionally an internal 45.000 degree self-test angle can also be selected. These bits are decoded as shown in Table 3.

TABLE 3.

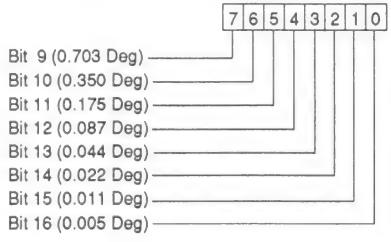
MSB	LSB	FUNCTION
0	0	45 Degree Self-Test Angle
0	1	11.8 Volt L-L input
1	0	26 Volt L-L input
1	1	90 Volt L-L input

BITS 17-20 & FAULT BIT MAP

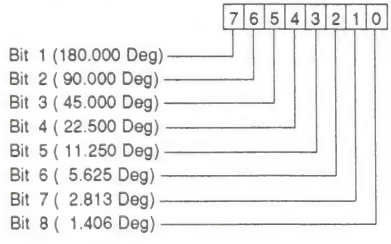


- Bits 17 thru 20 - These bits contain part of the binary angular information. This data must be combined with Bits 1 thru 16 as shown below under the heading of Binary Angular Data in order to calculate the angular position.
- LOR - During normal operation this bit will be in the logic high state. A logic low indication for this bit indicates that the Reference input to the converter is missing (Loss-Of-Reference).
- BIT - During normal operation this bit will be in the logic high state. A logic low indication for this bit indicates that the converter is not tracking the input Synchro/Resolver signal. This may occur momentarily if a step input is applied to the converter. The BIT signal will also be asserted if the converter is Inhibited while the input angle is changed or is rotating.

BITS 9-16 BIT MAP



BITS 1-8 BIT MAP



BINARY ANGULAR DATA

The composite Synchro/Resolver shaft angle is calculated from the data in bits 1 thru 20 using the following formula:

$$\text{Angle} = \frac{360 \times [(\text{Bits 1-8}) \times 4096 + (\text{Bits 9-16}) \times 16 + (\text{Bits 17-20})]}{1048576}$$

EXAMPLE:

Bits 1-8 = 0 1 1 0 1 0 1 0
Bits 9-16 = 0 1 0 1 0 0 0 1
Bits 17-20 = 0 1 1 0

The decimal equivalent of Bits 1-8 is 106
The decimal equivalent of Bits 9-16 is 81
The decimal equivalent of Bits 17-20 is 6

Inserting this data into the above equation yields the following:

$$\text{Angle} = \frac{360 \times [(106) \times 4096 + (81) \times 16 + (6)]}{1048576}$$

$$= 149.5095062 \text{ Degrees}$$

TIMING REQUIREMENTS

Data to and from the API-36005 card is controlled by the computer using standard I/O Read/Write cycles. However, the following precautions must be taken.

- Relays are used to switch the Synchro/Resolver input signals so enough time must be allocated for them to settle out (around 10ms).
- If the line-to-line voltage range of the synchro/resolver is changed, it could take up to 3 seconds for the converter to reacquire the input signals to the rated accuracy.
- If a step input is applied to the indicator, enough time must be allocated to allow the tracking converter to reacquire the input angular position. This could take up to 500 ms for a 180 degree step. During this time the $\overline{\text{BIT}}$ signal may be asserted.
- In order to guarantee that the three bytes of binary angular data are from the same instantaneous angular position the following sequence must be used:

  - 1.Set the $\overline{\text{Inhibit}}$ bit in the Control Word to logic low to freeze the converter.
  - 2.Read the three bytes of angular information in any sequence.
  - 3.Return the $\overline{\text{Inhibit}}$ bit to the logic high state to release the converter so that it can resume tracking the input signal.
  - 4.Process the retrieved data to calculate the angular position.

BASE ADDRESS SWITCH

The Base Address of the card is preset at the factory to HEX 300 as shown in Table 4. The Base Address can be changed to any address from 000h to 3F8h in increments of 8 using the Table 4 as a reference.

TABLE 4.

Address	Switch	OFF(OPEN)	ON	Function
A9	SW4	X		HEX 3
A8	SW5	X		
A7	SW6		X	HEX 0
A6	SW7		X	
A5	SW8		X	
A4	SW9		X	
A3	SW10		X	P/O HEX 0
A2		—	—	A0, A1, and A2 are
A1		—	—	not part of the
A0		—	—	base address.

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CONNECTORS

SIGNAL I/O CONNECTOR

The converter I/O signals are brought off the circuit card assembly via a 25 pin 'D' type connector. The signal connections to this connector are shown in Table 5.

TABLE 5.

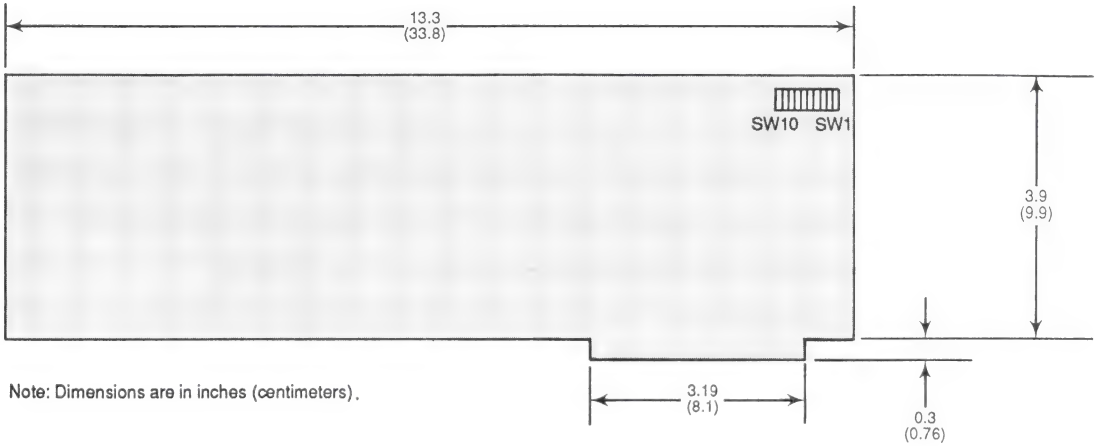
SIGNAL	PIN
S1 channel A	25
S1 channel B	13
S2 channel A	22
S2 channel B	10
S3 channel A	24
S3 channel B	12
S4 channel A	23
S4 channel B	11
RH	7
RL	8
Test Reference (externally supplied)	14
Circuit ground	9, 16, 1

COMPUTER INTERFACE CONNECTOR

The API-36005 inputs place one LS-TTL load on each of the IBM data bus lines and uses one standard TTL signal level to drive the data bus. The pin number and function of the computer interface signals are listed in Table 6.

TABLE 6. API-36005 PIN FUNCTIONS

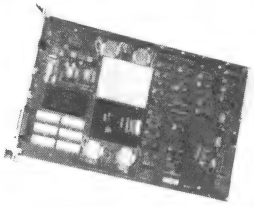
PIN NO.	SIGNAL NAME	FUNCTION
A1	$\overline{\text{I/O CHECK}}$	NOT USED
A2	D7	DATA BIT 7
A3	D6	DATA BIT 6
A4	D5	DATA BIT 5
A5	D4	DATA BIT 4
A6	D3	DATA BIT 3
A7	D2	DATA BIT 2
A8	D1	DATA BIT 1
A9	D0	DATA BIT 0
A10	I/O READY	NOT USED
A11	AEN	ADDRESS ENABLE
A12	A19	NOT USED
A13	A18	NOT USED
A14	A17	NOT USED
A15	A16	NOT USED
A16	A15	NOT USED
A17	A14	NOT USED
A18	A13	NOT USED
A19	A12	NOT USED
A20	A11	NOT USED
A21	A10	NOT USED
A22	A9	ADDRESS BIT 9
A23	A8	ADDRESS BIT 8
A24	A7	ADDRESS BIT 7
A25	A6	ADDRESS BIT 6
A26	A5	ADDRESS BIT 5
A27	A4	ADDRESS BIT 4
A28	A3	ADDRESS BIT 3
A29	A2	ADDRESS BIT 2
A30	A1	ADDRESS BIT 1
A31	A0	ADDRESS BIT 0
B1	GROUND	GROUND
B2	RESET	SYSTEM RESET
B3	+5V	POWER SUPPLY
B4	IRQ2	NOT USED
B5	-5V	NOT USED
B6	DRQ2	NOT USED
B7	$\overline{\text{-12V}}$	NOT USED
B8	$\overline{\text{0WS}}$	NOT USED
B9	+12V	POWER SUPPLY
B10	GROUND	GROUND
B11	$\overline{\text{MEMW}}$	NOT USED
B12	$\overline{\text{MEMR}}$	NOT USED
B13	$\overline{\text{IOW}}$	I/O WRITE
B14	$\overline{\text{IOR}}$	I/O READ
B15	$\overline{\text{DACK3}}$	NOT USED
B16	DRQ3	NOT USED
B17	$\overline{\text{DACK1}}$	NOT USED
B18	DRQ1	NOT USED
B19	$\overline{\text{DACK0}}$	NOT USED
B20	CLOCK	NOT USED
B21	IRQ7	NOT USED
B22	IRQ6	NOT USED
B23	IRQ5	NOT USED
B24	IRQ4	NOT USED
B25	IRQ3	NOT USED
B26	$\overline{\text{DACK2}}$	NOT USED
B27	T/C	NOT USED
B28	ALE	NOT USED
B29	+5V	POWER SUPPLY
B30	OSC	NOT USED
B31	GROUND	GROUND



Note: Dimensions are in inches (centimeters).

FIGURE 2. MECHANICAL OUTLINE
with DIP Switch location

ORDERING INFORMATION
API-36005



VXI REGISTER BASED SYNCHRO/RESOLVER SIMULATOR AND INDICATOR ON A CARD

PRELIMINARY

DESCRIPTION

The IAC-37001 is a Register Based "C" size VXI card containing separate Synchro/Resolver Angle Generation and Synchro/Resolver Angle Measurement instruments. Each instrument is totally independent from the other and can be programmed to operate in either the Synchro or Resolver mode at 11.8, 26, or 90 volts Line-to-Line over the frequency range of 360 to 5000 Hz.

The Measurement section allows selection of 20 or 16 Bit Binary resolution. The Generation section has a resolution of 16 Bits with an accuracy of ± 25 arc sec at no load and ± 36 arc sec with a 1.5 VA Synchro or Resolver load.

A Dynamic Rotation feature for the Generator provides the user with constant angular rotation either clockwise or counter clockwise via a programmed data rate, or by means of external speed and direction signals.

The two instruments can be connected together under program control to implement full wrap-around test capability.

APPLICATIONS

Applications for the IAC-37001 include production testing, quality control inspections, and laboratory instrumentation. Due to its flexibility, the IAC-37001 functions well for testing navigation equipment, antenna position, and calibration systems.

FEATURES

- *INDEPENDENT D/S AND S/D FUNCTIONS*
- *PROGRAMMABLE:*
  - *-Wrap-Around Self-Test*
  - *-Measurement/Generation Connect Relays*
  - *-L-L Voltage*
  - *-Synchro/Resolver*
  - *-Resolution*
  - *-Dynamic Rate and Direction*
  - *-Int/Ext Rate Signals*
- *FAULT REGISTER*
- *POWERED FROM THE ±12 AND +5 ON THE P1 CONNECTOR*
- *VXI:*
  - *-'C' Size Card (9.2 x 13.4 x 1.2")*
  - *-A16/D16 Format*
  - *-Register Based Device*

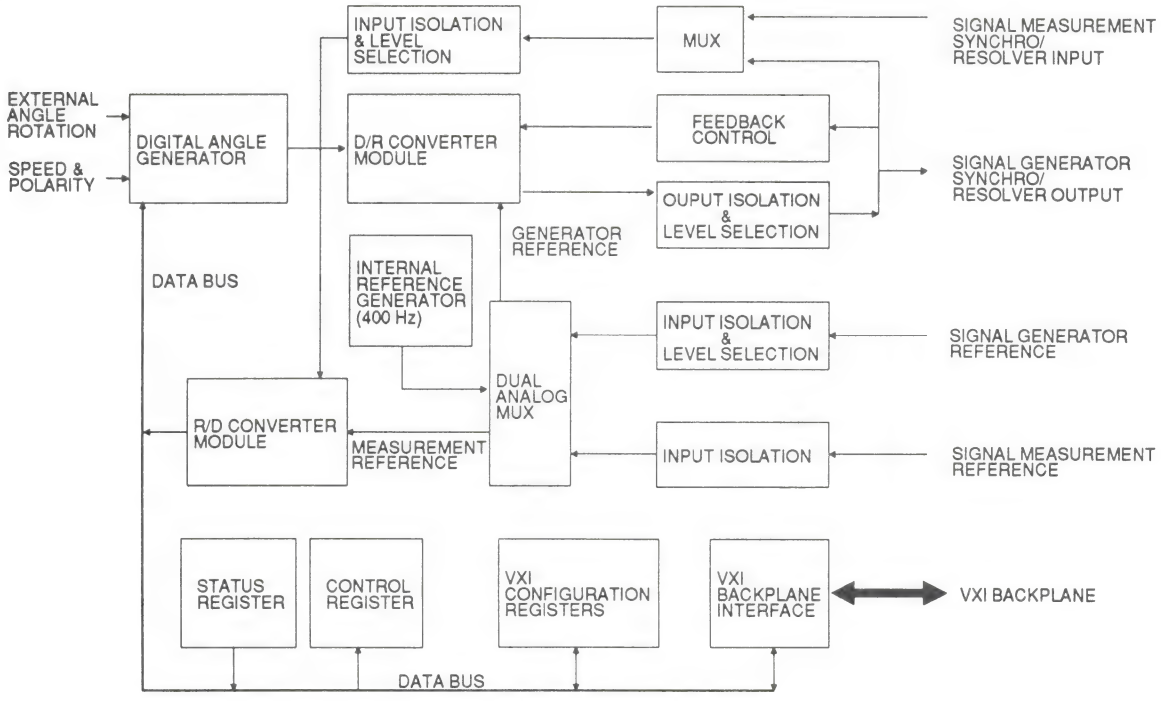


FIGURE 1. IAC-37001 BLOCK DIAGRAM

TABLE 1. IAC-37001 SPECIFICATIONS

PARAMETER	UNIT	VALUE
• *SIGNAL MEASUREMENT SECTION*		
RESOLUTION	Bits	20/16 programmable
ACCURACY	Arc Sec.	18(20-bit); 36(16-bit)
ANGULAR RANGE	Degrees	0 to 360
REFERENCE INPUT		
Type		transformer isolated
Voltage Range	Vrms	26 or 115 -40/+20%
Frequency	Hz	360 - 5,000
Input Impedance	Ohm	100k min
Breakdown Voltage	V	500 min.
Harmonic Content	%	10
SIGNAL INPUT		
Type		transformer isolated
Format		synchro or resolver
Voltages L-L	V L-L	11.8, 26, and 90
Frequency	Hz	360 to 5,000
Phase Shift	Deg	± 50 max Rel to Ref
Input Impedance	Ohm	150k min.
Breakdown Voltage	V	500 min.
DYNAMIC CHARACTERISTICS		
Tracking Rate		
16 Bit Mode	Deg/Sec	1,040 min.
20 Bit Mode	Deg/Sec	65 min.
Settling Time	sec	0.5 max
PROGRAMMABLE FEATURES		
L-L Voltage Input	—	—
Ref Level (115/26Vrms)	—	—
Synchro/Resolver	—	—
Resolution 20/16 Bits	—	—
Inhibit (Freeze Converter)	—	—
Hold (Freeze Data)	—	—
• *SIGNAL GENERATION SECTION*		
RESOLUTION	Bits	16
ACCURACY	Arc Sec.	25 No Load, 36 Full Load
ANGULAR RANGE	Degrees	0 to 360
REFERENCE INPUT		
Type		transformer isolated
Voltage	Vrms	26/115 programmable
Frequency	Hz	360 - 5,000
Breakdown Voltage	V	500 min.
Harmonic Content	%	10 max for full accuracy
SIGNAL OUTPUT		
Type		transformer isolated
Format		synchro or resolver
Voltages L-L	V L-L	11.8, 26, and 90
Drive Capability	VA	1.5
Scale Factor	%	± 3.5
Scale Factor Variation with angle	%	± 0.15
Protection		output & thermal overload
Breakdown Voltage	V	500 min.
DYNAMIC ROTATION (INT)		
Rotation		constant rate CW or CCW
Resolution		12 bits binary plus sign
Range 1 (Output Steps of 0.0055 Deg.)	Deg/Sec	0.17 min (LSB Weight) 686.48 (1.91 RPS) max
Range 2 (Output Steps of 0.088 Deg.)	Deg/Sec	2.68 min (LSB Weight) 10983.6 (30.5 RPS) max

TABLE 1. IAC-37001 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE
• *SIGNAL GENERATION SECTION - continued*		
DYNAMIC ROTATION (EXT)		
Range 1	Deg	0.0055 per clock tick
Range 2	Deg	0.088 per clock tick
Direction		CW or CCW
PROGRAMMABLE FEATURES		
L-L Voltage Output	—	—
Ref Level (115/26Vrms)	—	—
Synchro/Resolver	—	—
Dynamic Rate and Direction	—	—
Int/Ext Rate Signals	—	—
Disconnect	—	—
Converter Enable	—	—
• *GENERAL CARD INFORMATION*		
POWER SUPPLIES	V	Powered by ±12 and +5 on the P1 connector.
Current		
+5 I_{PM}	mA	900
+5 I_{DM}	mA	30
+12 I_{PM}	mA	590
+12 I_{DM}	mA	290
−12 I_{PM}	mA	520
−12 I_{DM}	mA	280
+5 average	mA	870
+12 average (no load)	mA	175
+12 average (full load)	mA	335
+12 average (short circuit)	mA	590
−12 average (no load)	mA	110
−12 average (full load)	mA	305
−12 average (short circuit)	mA	520
TEMPERATURE RANGE		
Operating	°C	0 to +50
Storage	°C	-25 to +85
PHYSICAL CHARACTERISTICS		
Size (VXI 'C')	in	9.2 x 13.4 x 1.2

INTRODUCTION

The Signal Measurement section can be programmed to provide either 16 or 20 bits of resolution with an accuracy of 18 arc seconds either in the Synchro or Resolver mode. Both the Reference and the Synchro/Resolver inputs are fully transformer isolated and can accept signals over the frequency range of 360 to 5000 Hz. The Measurement section can be programmed to accept Synchro/Resolver signals of 11.8, 26, or 90 volts Line-to-Line and Reference input levels of 26 or 115Vrms. A hold feature allows the computer to freeze the converter data at the current angle for data readout, synchronization to external events, or synchronization with other Synchro/Resolver Angle Indicator cards. Inhibit allows the computer to freeze the converter at the current angle.

The Signal Generation section can be programmed to provide either Synchro or Resolver output signals at 11.8, 26, or 90 volts Line to Line, and to accept Reference input levels of 26 or 115 Vrms. The Reference input and the Synchro/Resolver output

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signals are both transformer isolated and operate over the frequency range of 360 to 5000 Hz.

The Generator section also contains a Dynamic Rotation capability. This feature provides for a programmed constant angular velocity, either clockwise or counter clockwise, in two ranges (low and high). Using the internal clock the Low Range steps the converter in 0.0055 degree increments from 0.1676 degrees/second to 686.4776 degrees/second with a resolution of 0.1676 degrees/second. In the High Range, which is effectively the Low Range times 16, the converter steps in 0.088 degree increments and covers the rotational range of 2.6822 degrees/second to 10983.6418 degrees/second (30.5101 RPS). The card can also be programmed to accept external Rate and Direction signals for user programmable dynamic applications.

A block diagram of the IAC-37001 is shown in figure 1.

SELF-TEST

Three modes of wrap-around self-test are available under program control. A complete stand-alone self-test mode can be achieved by programming the IAC-37001 to connect the Measurement section input to the Generator section output, programming both sections for the same Synchro/Resolver mode and Line-to-Line level, and selecting the internal 400 Hz test Reference. No external signals are required to perform this wrap-around self-test.

When the IAC-37001 Instrument is being used primarily as a Generator, a real-time self-test mode can be programmed by simply programming the Measurement section for the same Synchro/Resolver mode and Line-to-Line level as the Generator (and supplying it with the same reference that the Generator is using), and connecting it to the Generator output. In this configuration the Generator output can be continuously monitored in real-time.

When the IAC-37001 is being used primarily for angle Measurement the Generator can be programmed for the same Synchro/Resolver mode and Line-to-Line voltage as the Measurement section and supplied with the same reference. The Measurement section can then be switched back and forth between the Generator output and the external signal inputs for a quasi-real-time test i.e., the Measurement section can be verified before each reading. If the expected angular position of the external Synchro/Resolver signal is known beforehand (as in a predefined test procedure) this self-test mode is generally more useful.

INTERNAL REGISTERS

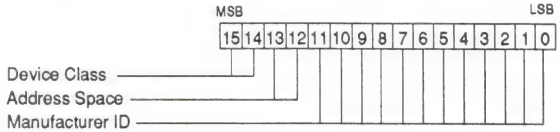
REGISTER ADDRESSING

The IAC-37001 is addressed in typical Logical Address and Offset fashion in accordance with the VXIbus System Specification, and utilizes 11 registers to communicate with the VXI system. A Memory Map of these eleven registers is shown in Table 2 and the registers are described in detail in the Register Bit Map section. The DIP switch for the Logical Address of the card is preset at the factory for a Logical Address of 2 as shown in Table 3. The Logical Address can be changed to any address from 00h to FFh using Table 3 as a reference.

TABLE 2.

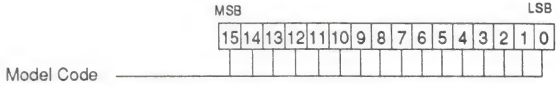
Hex Offset	Read	Write
00	ID Register	Not Used
02	Device Type	Not Used
04	Status Register	Control Register
06	Not Used	Not Used
08	Not Used	Control Word A
0A	Not Used	SG Angle
0C	SM Angle LSBs	Not Used
0E	SM Angle MSBs	Not Used
10	Extended Model Number	Not Used
12	Not Used	Not Used
14	Not Used	D/S Speed and Polarity

ID REGISTER BIT MAP



- Device Class - Both of these bits are set to logic 1 to define a Register Based VXI Device.
- Address Space - Both of these bits are set to logic 1 to define a A16 Only VXI Device.
- Manufacturer ID - These bits contain the DDC manufacturer ID number of 4072 (FE8h).

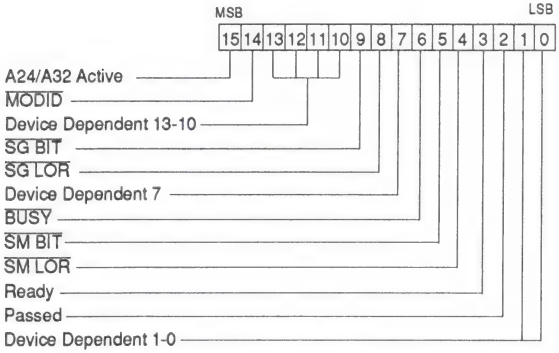
DEVICE TYPE BIT MAP



- Model Code - These 16 bits contain the DDC model number 310 (0136h).

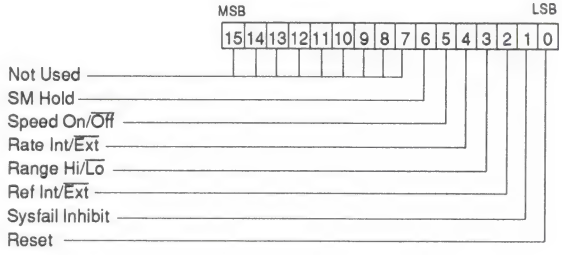
INTERNAL REGISTERS -continued

STATUS REGISTER BIT MAP



- A24/A32 Active - This is a device dependant bit for A16 devices and is permanently set to logic 1.
- MODID - The IAC-37001 does not support MODID capability so this bit is permanently set to logic 1.
- Device Dependent 13-10 - These device dependent bits are all permanently set to logic 1.
- SG BIT - This bit is normally at a logic 1 state. This bit will go to logic 0 if the Signal Generator is experiencing a thermal or electrical overload condition. This bit may go to logic 0 momentarily if a large angular step is programmed.
- SG LOR - This bit is normally at a logic 1 state. This bit will go to logic 0 if the Reference input to the Generator is missing (Loss-Of-Reference).
- Device Dependent 7 - This bit is permanently set to logic 1.
- BUSY - This bit is normally at a logic 1 state. This bit will go to logic 0 for approximately 3 seconds after making a write to the Control Word A register. During this time the Generator output and the Measurement data may not be within the specified accuracy limits.
- SM BIT - This bit is normally at a logic 1 state. This bit will go to logic 0 if the Signal Measurement is unable to track the input Synchro/Resolver signal. This can happen if the Synchro/Resolver input is rotating too fast, if the Synchro/Resolver input is missing altogether, or if the converter is inhibited and the input angle is changed. This bit may also go to logic 0 momentarily if a step input is applied to the converter.
- SM LOR - This bit is normally at a logic 1 state. This bit will go to logic 0 if the Signal Measurement input Reference is missing.
- Ready - This bit is permanently set to logic 1.
- Passed - This bit is permanently set to logic 1.
- Device Dependent 1-0 - These two device dependent bits are permanently set to logic 1.

CONTROL REGISTER BIT MAP



- SM Hold - This bit controls the transfer of the angular Measurement data into internal storage registers. Setting this bit to logic 0 will cause the continous transfer of angular Measurement data into these storage registers. Setting this bit to logic 1 will cause the Measurement section to continue to track the input signals; however, the storage registers will hold the angular data present at the time of the low-to-high transition of this bit (in worst case conditions there may be a 2 µs delay between the low-to-high transition and the storing of the angular data). To set up for the next read sequence, after the interface reads the angular data, this bit should be set back to logic 0 .
- Speed On/Off - A logic 1 on this bit enables the Signal Generator to rotate at the programmed direction and speed. A logic 0 disables the Dynamic Rotation feature causing the Generator to stop rotating.
- Rate Int/Ext - A logic 1 on this bit selects the internal programmed rate and polarity signals. A logic 0 selects the external rate and polarity inputs. In the external rate mode the rotational angular rate is related to the External Clock in the Low-Speed mode (see bit 03) as follows:
  - Rotational rate (Degrees/Second) = $\frac{360}{65536}$ * Ext clock
  - In the High-Speed mode the rate is 16 times faster.
- Range Hi/Lo - A logic 1 on this bit sets the Dynamic Rotation mode into the High-Speed (16X) mode. A logic 0 selects the Low-Speed range. See the D/S speed and polarity register for additional information.
- Ref Int/Ext - A logic 1 on this bit selects the internal 400 Hz Reference for both the Signal Measurement and Signal Generation sections. A logic 0 selects external Reference signals.
- Sysfail Inhibit - The Sysfail function is not implemented on the IAC-37001 so this bit is nonfunctional.
- Reset - A logic 1 on this bit will reset the IAC-37001 to the power on state i.e., the Control Word A register, the SG Angle register, and the D/S Speed and Polarity register are all cleared to logic 0.

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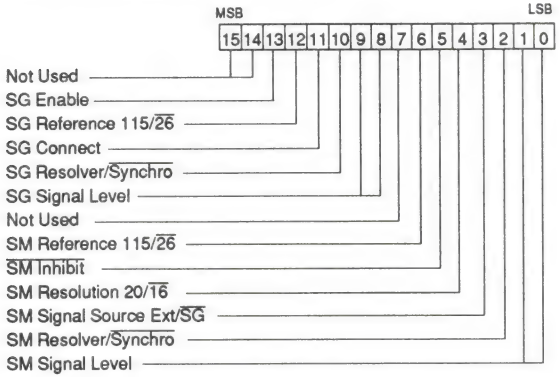
CONTROL WORD A REGISTER BIT MAP



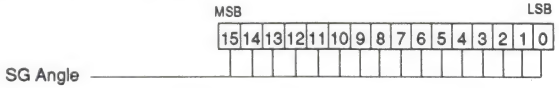
- SG Enable - A logic 1 on this bit enables the Signal Generator output power driver. A logic 0 disables the power driver.
- SG Reference 115/26 - A logic 1 on this bit configures the Signal Generator to accept a 115 Vrms Reference input signal. A logic 0 configures the Generator to accept a 26 Vrms Reference.
- SG Connect - A logic 1 on this bit closes the Connect relays placing the programmed Generator output signals on the front panel output connector pins. A logic 0 disconnects the Generator output signals from the front panel.
- SG Resolver/Synchro - A logic 1 on this bit configures the Generator to supply Resolver output signals. A logic 0 selects Synchro output signals.
- SG Signal Level - These two bits set the Generator Line-to-Line voltage level according to the following table:

Bit 9	Bit 8	L-L Level
0	0	11.8 V
0	1	26 V
1	0	INVALID
1	1	90 V

- SM Reference 115/26 - A logic 1 on this bit configures the Measurement section to accept a 115 Vrms Reference signal. A logic 0 selects a 26 Vrms reference signal.
- SM Inhibit - This bit should normally be set to the logic 1 state. A logic 0 on this bit freezes the converter at the angle present at the high to low transition of the bit. Be careful when using this function because it will stop the Measurement section from tracking the input signal. It could take up to 500ms for the system to recover after returning the SM Inhibit bit to logic 1.
- SM Resolution 20/16 - A logic 1 on this bit configures the Measurement section for a resolution of 20 bits. A logic 0 selects 16 bit resolution.
- SM Signal Source Ext/SG - A logic 1 on this bit configures the Measurement section to accept External Resolver/Synchro signals. A logic 0 connects the Measurement section inputs to the Generation section output for wrap-around testing.
- SM Resolver/Synchro - A logic 1 on this bit configures the Measurement section to accept Resolver input signals. A logic 0 selects Synchro input signals.
- SM Signal Level - These two bits control the input signal level selection for the Measurement section according to the following table:

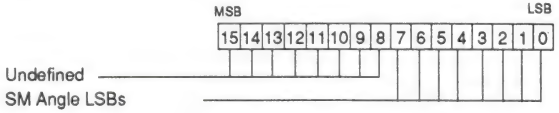
Bit 1	Bit 0	L-L Level
0	0	11.8 V
0	1	26 V
1	0	INVALID
1	1	90 V

SG ANGLE BIT MAP



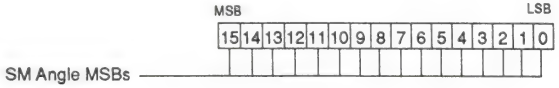
- SG Angle - The 16 bit word contained in this register programs the Generator output angle. Bit 15 has a angular bit weight of 180 degrees, bit 14 has a weight of 90 degrees, etc., down to bit 0 which has a weight of 0.0055 degrees (rounded to 4 decimal places).

SM ANGLE LSBs BIT MAP



- Undefined - A byte register for these bits is not implemented in the hardware. As it is most likely that logic 1s will be returned for this byte these bits should be ignored, stripped off, or set to logic 0 by the computer.
- SM Angle LSBs - Bits 07 thru 04 are preset to logic 0. Bits 03 thru 00 contain the LSBs of the Measurement angle when the Measurement section is programed for the 20 bit resolution mode of operation. Bit 03 has a angular bit weight of 0.0027 degrees and bit 00 has a weight of 0.0003 degrees (rounded to four decimal places).

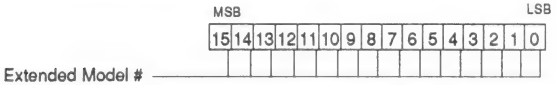
SM ANGLE MSBs BIT MAP



- SM Angle MSBs - This 16 bit word contains the 16 MSBs of the angle read by the Measurement section for both the 16 bit and 20 bit modes of operation. Bit 15 has an angular bit weight of 180 degrees, bit 14 has a weight of 90 degrees, etc., down to bit 00 which has a weight of 0.0055 (rounded to 4 decimal places).

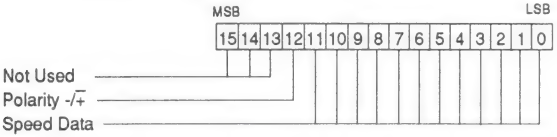
INTERNAL REGISTERS -continued

EXTENDED MODEL NUMBER REGISTER BIT MAP



- Extended Model # - This 16 bit word contains the DDC revision level of the instrument.

D/S SPEED AND POLARITY BIT MAP



- Polarity -/+ - A logic 1 for this bit (in conjunction with bits 3,4,and 5 in the Control Register) causes the Generator Output to rotate in the direction of decreasing angular values. A logic 0 causes the output to rotate in the direction of increasing angular values.
- Speed Data - This 12 bit word sets the speed of rotation of the Generator Output when the Int Rate mode is programed (see bit 04 of the Control register). This Speed Data value can range from 0 to thru 4095. The speed of rotation is related to this word in the Low-Speed range (see bit 04 of the control register) as follows:

  - Rotational speed (Deg/Sec) $= \frac{360 \times 125{,}000}{65536 \times 4096} \times$ Speed Data
    $= 0.167638063 \times$ Speed Data

  - For the High-Speed mode the rotational rate is 16 times faster.

BINARY ANGULAR DATA

Decimal Angle to Binary Angle conversion Algorithm

The Most Significant Bit (MSB) of the 16 bit word represents the Binary Angular value of 180 Degrees. The second MSB represents the angular value of 90 Degrees, and the third represents 45 Degrees, etc., down to the Least Significant Bit (LSB) which represents 0.005 Degrees (rounded to 3 decimal places).

Algorithms to convert Decimal angular data into Binary angular data consist of testing the magnitude of the Decimal value against the Binary values to see which Binary values can be added together in order to come closest to the Decimal value. This test generally starts with the most significant Binary bit weight of 180 Degrees and determines whether it is more or less than the Decimal value. If the Decimal value is larger than 180 degrees then obviously this Binary bit is part of the final Binary value, if the Decimal value is less than 180 degrees then this Bit is not part of the final Binary value. This same test is now performed using the second Binary Bit (90 degrees) and so on down to the LSB of 0.005 Degrees.

For example, to convert 135.703 Degrees to a Binary value the following steps are taken.

1. The Most Significant Binary bit is 180 Degrees and is obviously too large to be contained in the final Binary value so it is set to logic 0.
2. The Second Binary Bit has the value of 90 Degrees which is smaller than the Decimal value of 135.703 Degrees. It is obviously part of the final Binary value so it is set to logic 1 and 90 Degrees is subtracted from the Decimal value leaving 45.703 degrees.
3. The Third Binary bit has the value of 45 Degrees which again is smaller than the Decimal remainder of 45.703. It obviously is part of the final Binary value so it is set to logic 1 and 45 Degrees is subtracted from the Decimal remainder leaving 0.703 Degrees.
4. The Forth Binary Bit has a value of 22.5 Degrees which is too big to fit. It is set of logic 0 and the testing continues using the Decimal value of 0.703. So far we have tested the 4 MSBs of the Binary values and the Binary solution at this point is "0 1 1 0" with 12 more Binary Bits to test.
5. The 5th, 6th, 7th, and 8th Binary bits are all too large and are therefore set to logic 0. The Binary value at this point is "0 1 1 0 0 0 0 0" with 8 more Binary Bits to test.
6. The Binary Bit weight of the 9th bit is 0.703 Degrees and it fits exactly into the Decimal value of 0.703. The Binary Bit is therefore set to logic 1 and the Binary answer at this point is "0 1 1 0 0 0 0 0 1". The Binary value of 0.703 is subtracted from the Decimal Value and the remainder is 0.
7. As the Decimal remainder is now 0 obviously none of the remaining Binary Bits will Fit into the Decimal value so they can all be set to logic 0. The final 16 bit Binary answer is therefore "0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0"

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Binary Angle to Decimal Angle conversion Algorithm

Conversion of Binary Angular Data into Decimal Angular Data is simply a matter of adding all of the Decimal Angular weights for all of the binary bits which are set to logic 1. For example if the Measurement section is programmed for 16 bits of resolution and the Binary Angular measurement is

"0 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0"

The Decimal angle will be

(0 x 180)
+ (1 x 90)
+ (1 x 45)
+ (0 x 22.5)
+ (1 x 11.25)
+ (1 x 5.625)
+ (0 x all other bit weights)
Total 151.875 Degrees

If the 16 bit binary value is treated as an Binary Integer, which in this case has the hex value of FC00 or the decimal value of 27648, the binary angle can be calculated via the following formula:

$$\text{Decimal Angle} = \frac{360 \times \text{Binary Integer Value}}{65536}$$

which for this example is:

$$= \frac{360 \times 27648}{65536} = 151.875 \text{ degrees}$$

In the 20 Bit mode the equation expands to the following:

$$\text{Decimal Angle} = \frac{360 \times \text{MBSs Value}}{65536} + \frac{360 \times \text{LSBs Value}}{1048576}$$

TIMING REQUIREMENTS

All data to and from the IAC-37001 card is transferred via standard Read/Write cycles, however the following precautions must be taken.

- Relays are utilized to switch the Measurement section Synchro/Resolver input Line-to-Line levels so enough time must be allocated for them to settle out (around 10ms).
- If an angular step input is applied to the Measurement section, enough time must be allocated to allow the tracking converter to reacquire the input angular position. This could take up to 500 ms for a 180 degree step. During this time the $\overline{\text{SM BIT}}$ signal may be asserted.
- In order to guarantee that the Measured binary angular data is stable during the time it is being read by the computer the following sequence must be utilized:
  - 1.Set the SM Hold bit in Control Register (bit 06) to logic 1 to hold(freeze) the angular data.
  - 2.Wait at least 2 µs for the Measurement section to finish up any residual processing.
  - 3.Read the angular information of 16 or 20 bits.
  - 4.Return the SM Hold bit to the logic 0 to set up for the next read sequence.
  - 5.Process the retrieved data to calculate the angular position.
- Relays are utilized to switch the Synchro/Resolver Line-to-Line levels of the Generator, and to implement the Connect feature. Enough time must be allocated for the relays to settle out (around 10 ms) so that the Generator output is stable.
- If an angular step input is given to the Generator allow at least 50 ms for the output to stabilize.
- If the SG output amplifier is disabled (Control Word A, bit 13), it could take up to 3 seconds to stabilize after it is re-enabled.
- If the reference input to the SG or SM section is missing, the value of the $\overline{\text{BIT}}$ signal may not be valid.

LOGICAL ADDRESS SWITCH

The Logical Address switch is a 10 position dip switch located on the printed circuit card assembly. This switch is preset at the factory to the logical address of 2 as shown in Table 3. If desired the Logical Address can be changed to any other Logical Address from 00h to FFh using Table 3 as a reference.

TABLE 3

Switch Position	OFF/OPEN	ON	Function
10		X	User
9		X	Not Used
LSB 8		X	HEX 2
7	X		
6		X	
5		X	
4		X	HEX 0
3		X	
2		X	
MSB 1		X	

Note 1: The IAC-37001 is a static configuration, slave device and as such should not be assigned to Logical Addresses 0 or 255 (00h or FFh) to avoid conflicting with other VXI instrumentation. Setting the Logical Address to 1 may also cause a problem as some Slot 0 controllers utilize this address.

Note 2: Each VXI instrument is assigned a 64 byte memory area in the A16 address space, and to decode these 64 bytes requires the use of the lower 6 address bits (05 to 00). The Logical Address utilizes the next 8 address bits (13 to 06) and address bits 15 and 14 are defined by the VXIbus specification to be in the logic 1 state.

CONNECTORS

VXI INTERFACE CONNECTOR

The IAC-37001 utilizes only the P1 connector of the VXI backplane. The signal connections made on this connector are shown in Table 4.

SIGNAL I/O CONNECTOR

The converter I/O signals are brought off the circuit card assembly via a 25 pin 'D' type connector mounted on the front panel. The signal connections to this connector are shown in Table 5.

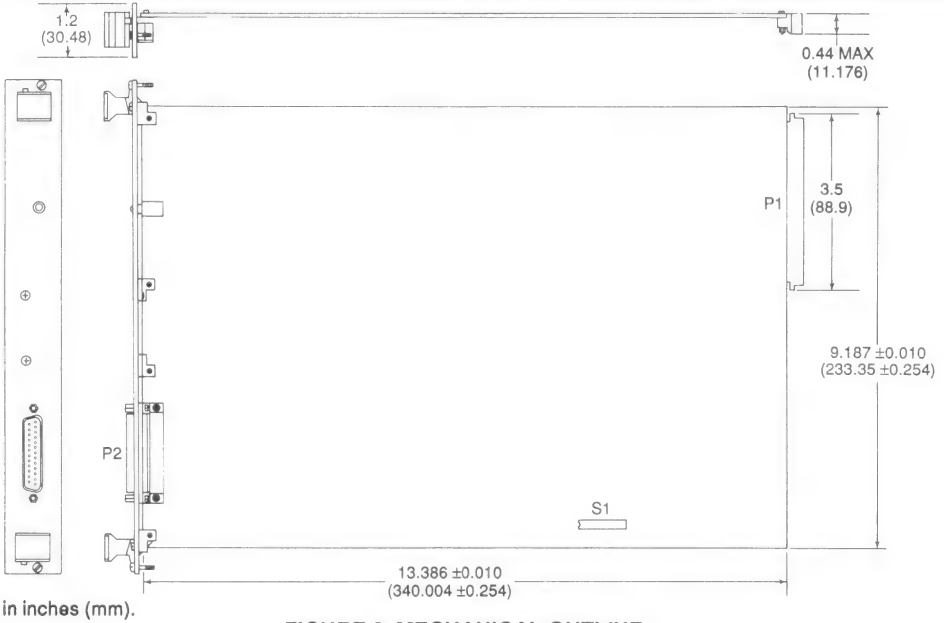
ORDERING INFORMATION
IAC-37001

TABLE 4.

PIN	ROW A	ROW B	ROW C
1	D00	—	D08
2	D01	—	D09
3	D02	—	D10
4	D03	$\overline{BG0IN}$	D11
5	D04	$\overline{BG0OUT}$	D12
6	D05	$\overline{BG1IN}$	D13
7	D06	$\overline{BG1OUT}$	D14
8	D07	$\overline{BG2IN}$	D15
9	GND	$\overline{BG2OUT}$	GND
10	SYSCLK	$\overline{BG3IN}$	—
11	GND	$\overline{BG3OUT}$	$\overline{BERR}$
12	$\overline{DS1}$	—	$\overline{SYSRESET}$
13	$\overline{DS0}$	—	$\overline{LWORD}$
14	$\overline{WRITE}$	—	AM5
15	GND	—	—
16	$\overline{DTACK}$	AM0	—
17	GND	AM1	—
18	$\overline{AS}$	AM2	—
19	GND	AM3	—
20	$\overline{IACK}$	GND	—
21	$\overline{IACKIN}$	—	—
22	$\overline{IACKOUT}$	—	—
23	AM4	GND	A15
24	A07	—	A14
25	A06	—	A13
26	A05	—	A12
27	A04	—	A11
28	A03	—	A10
29	A02	—	A09
30	A01	—	A08
31	-12V	—	+12V
32	+5V	+5V	+5V

TABLE 5.

PIN	SIGNAL
1	GROUND
2	—
3	SG REF RL
4	—
5	SM REF RL
6	—
7	SG S2
8	SG S4
9	—
10	SM S2
11	SM S4
12	EXT RATE POLARITY
13	GROUND
14	—
15	SG REF RH
16	—
17	SM REF RH
18	—
19	SG S1
20	SG S3
21	—
22	SM S1
23	SM S3
24	GROUND
25	EXT SPEED CLOCK

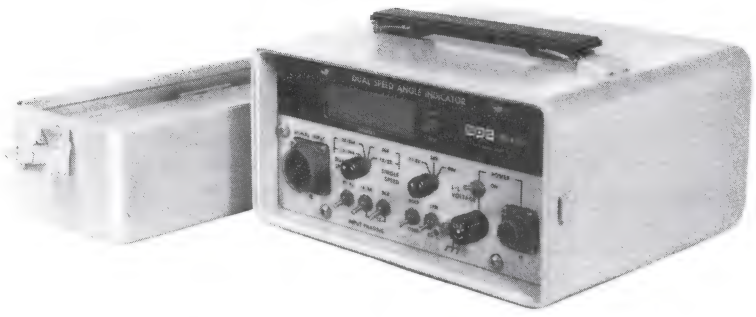


Dimensions are in inches (mm).
c

FIGURE 2. MECHANICAL OUTLINE with DIP SWITCH location

MSR-236

MULTISPEED SYNCHRO/RESOLVER ANGLE INDICATOR
Measures Single/Dual Speeds in Dual Speed Systems



MSR-236
MILITARIZED
PACKAGE

DESCRIPTION

The MSR-236 is a versatile angle indicator instrument for dual speed synchro and resolver systems. Front panel switches can be used not only to select the input (synchro or resolver, L-L voltage level, speed ratio) and to control (inhibit, lamp test) but also to change the measurement after the system has been connected (dual speed or single speed at either input; reverse direction of rotation). The MSR-236 is housed in a rugged, militarized MIL-T-21200 type drip-proof combination case designed for shipboard use. The instrument can be used to display angle, to test synchro or resolver systems, and to interface single or dual speed systems with a computer. No adjustments or calibrations are required, and there is no warm-up period, drift, or jitter.

APPLICATIONS

Designed as a rugged, all-purpose multispeed angle indicator, the MSR-236 can be used wherever the accuracy of two-speed conversion is required. It can be used as test and measuring equipment, or it can be installed as part of a system control loop, serving as a converter with a display. Since the single speed of each two-speed input can be measured independently, the MSR-236 is useful for system alignment. Applications are found in radar antenna systems, fire control systems, navigation sensors, and automatic machine tool control monitoring.

FEATURES

- *MEASURES ANGLE IN SINGLE OR DUAL SPEED MODES IN 1:36 AND 2:36 SPEED SYSTEMS*
- *DISPLAYS 5 DECADE ANGLE WITH .01° RESOLUTION AND PRODUCES PARALLEL BCD DIGITAL OUTPUT*
- *ACCURACY:*
  ±0.01° in multispeed mode
  ±0.1° ±1 LSB in single speed mode
- *SIGNAL AND REF INPUT:*
  Transformer isolation
  All common synchro and resolver L-L voltage levels and frequencies
  Front panel switches can change reference and signal phasing to reverse sense of rotation
- *LOGIC:*
  TTL compatible
  Converter Busy and Inhibit
- *OPERATES FROM STANDARD LINE VOLTAGES, 115/230V WITH TRANSFORMER ISOLATION, AND 47–440 Hz*

MSR-236

SPECIFICATIONS

PARAMETER	VALUE
RESOLUTION	0.01°
ACCURACY (All Causes)	
Dual Speed Mode	±0.01°
Single Speed Mode	±0.1° ±1 LSB
ANGLE RANGE	000.00° to 359.99°, continuous rotation for 1X and 1:36 speed modes ±89.99° in 2X and 2:36 speed modes
CONVERSION RATE	Greater than 30 times/sec Harmonic oscillator type converter
FRONT PANEL DISPLAY	5 digit, 7 segment, LED display
REFERENCE INPUT	
Input Type	Transformer isolation
Voltage	10 to 130V
Frequency	47 to 500 Hz
Input Impedance	25K ohms min
Allowed Phase Shift	±20° relative to signal, for full accuracy
Breakdown Voltage	±500 VDC to Logic GND
SIGNAL INPUT	
Input Type	Transformer isolation Dual speed synchro or resolver input
Voltage	11.8V, 26V, or 90V Line-to-Line
Frequency	Same as Reference
Impedance	100 KΩ min
Tolerances:	
Voltage	±20%
Harmonics	±10%
Breakdown Voltage	±500 VDC to Logic GND
DIGITAL INPUT/OUTPUT (TTL Compatible)	
Digital Angle Output	5 BCD decades, 18 data lines total, positive true logic, continuously available: 200°, 100°, 80°, 40°, 20°, 10°, 8°, 4°, 2°, 1°, 0.8°, 0.4°, 0.2°, 0.1°, 0.08°, 0.04°, 0.02°, 0.01° Drive capability is 5 Std TTL loads, buffered outputs
Converter Busy Output	2 µsec positive pulse (logic 1 = busy) Drive capability is 5 Std TTL loads, buffered output
Inhibit Input	Logic 0 inhibits update of angle display and BCD output Loading is 1 Std TTL load
FRONT PANEL CONTROLS	
Synchro/Resolver	Selects synchro or resolver mode
Line-to-Line Voltage	Selects 11.8V or 26V or 90V
Measurement Mode	Selects dual speed 1:36, or dual speed 2:36, or single speed of 1X or 2X input, or single speed of 36X input
Hold/Convert	Applies Inhibit
Lamp Test	Tests LED display by lighting all segments (888.88 display)
Power ON/OFF	Main power control
TEMPERATURE RANGES	
Operating	0°C to +55°C
Storage	−55°C to +125°C
POWER INPUT	
Voltage	115/230V rms ±10%
Power Frequency	47 to 440 Hz
Fuse (on Rear Panel)	Buss, GMW -1, 1 Amp
Isolation	Transformer
PHYSICAL CHARACTERISTICS	
MSR-236	MIL-T-21200 type drip-proof combination case Removable front cover stores signal and power cables. Color either "Flight-Line" yellow or "Standard" grey.
Size	12 x 9.6 x 4.8 inch (30.5 x 24.4 x 12.2 cm)
Weight	11.7 lbs typ, including cables (5.3 kg)
Connectors	Standard MS connectors on front panel; 15 ft signal cable for reference and signal inputs terminates with clearly identified alligator clips; 8 ft power cord.

PIN ASSIGNMENTS

J1 POWER CONNECTOR

MSR-236 Pin No.	Function
A	115V/230V High
B	115V/230V Low (Neutral)
C	Chassis GND

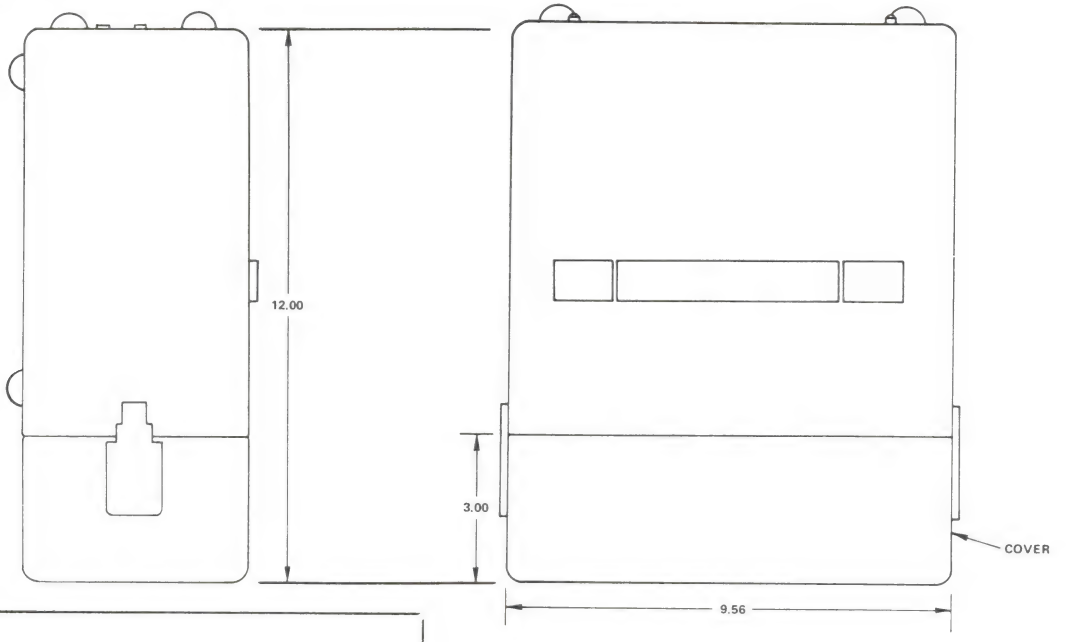
NOTE: 115V or 230V operation is selected by a switch inside the case. Units are set for 115V unless specified otherwise.

J2 INPUT/OUTPUT CONNECTOR

MSR-236 Pin No.	Function
A	S1 } X36 INPUT
B	S3 } S4 for
C	S4 } resolver
D	S2 } inputs only
E	200°
F	100°
G	80°
H	40°
J	20°
K	10°
L	8°
M	4°
N	2°
P	S1 } X1 INPUT
R	S3 } S4 for
S	S4 } resolver
T	S2 } inputs only
U	RH Reference high
V	RL Reference low
W	.8°
X	.4°
Y	.2°
Z	.1°
a	.08°
b	.04°
c	.02°
d	.01°
e	CB Converter Busy
f	GND Digital ground
g	INH Inhibit
h	Spare pin
j	1°
—	Spare pins

G

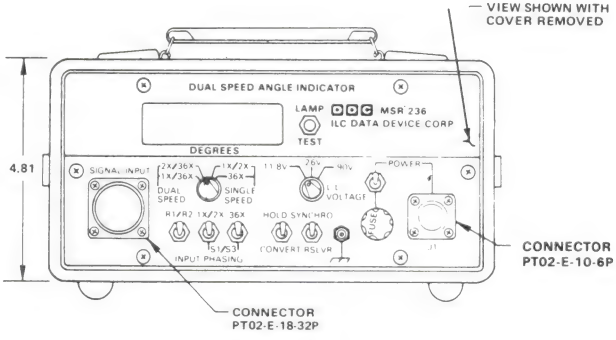
MSR-236 MECHANICAL OUTLINE



ORDERING INFORMATION

MSR-236* Instrument packaged in a MIL-T-21200 combination case. MS connectors, signal cord, line cord and instruction manual are included.

*MSR-236 case will be "standard" grey unless another color is requested.

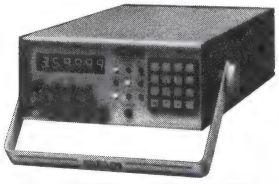


A

DDC
ILC DATA DEVICE CORPORATION

SIM-31200 SERIES

SYNCHRO AND RESOLVER ANGLE SIMULATORS



High Frequency Option (SIM-31205) Available (contact factory)

DESCRIPTION

The SIM-31200 Series are high quality synchro and resolver simulators, which incorporate microprocessor control of digital input multiplexing, front panel display, internal 20-bit digital to resolver converter and status/fault flag outputs. The internal 20-bit binary converter provides resolution of .001° BCD or .00034° binary, with accuracy up to ±.003° (10 arc seconds). The angle input may be entered locally via the keyboard, or remotely through the rear panel parallel data connector. The remote input format (BCD or binary) is selectable via a rear panel switch. An optional IEEE-488 interface is available for using the SIM-31200 with instruments connected to a General Purpose IEEE Parallel Data Bus.

The front panel keyboard is for local programming of output formats, increment/decrement, output voltage levels, angle entry and calibration/test functions.

The reference input (26 or 115V rms) is broadband (47 Hz to 11 KHz) and may be supplied to the rear panel connector or front panel terminals.

The outputs are transformer isolated synchro or resolver signals programmable to 11.8, 26, or 90V rms line-to-line.

The microprocessor provides control for analog signal output formats and levels. In addition, the microprocessor works in conjunction with a nonvolatile memory and a counting circuit to measure the reference frequency which is used to generate a digital correction and calibration scheme.

The instrument is powered by 115V or 230V rms, and has internal EMI/RFI filtering. Bench top and rack mounted configurations with or without front panel keyboard or display are available.

APPLICATIONS

Applications for SIM-31200 Series include production testing, quality control inspections and laboratory instrumentation. Due to its I/O flexibility, the SIM-31200 functions well for testing navigation equipment, antenna position and calibration systems.

FEATURES

- *5 VA DRIVE CAPABILITY*
- *HIGH ACCURACY:*
  ±.003° NO LOAD
  ±.008° FULL LOAD
- *WIDEBAND: 47 Hz TO 11 KHz*
- *IEEE INTERFACE (OPTIONAL)*
- *PROGRAMMABLE OUTPUT STANDARD SYNCHRO AND RESOLVER LEVELS*
- *OVERLOAD PROTECTED*
- *DIGITAL CALIBRATION FOR IMPROVED MAINTAINABILITY*

G

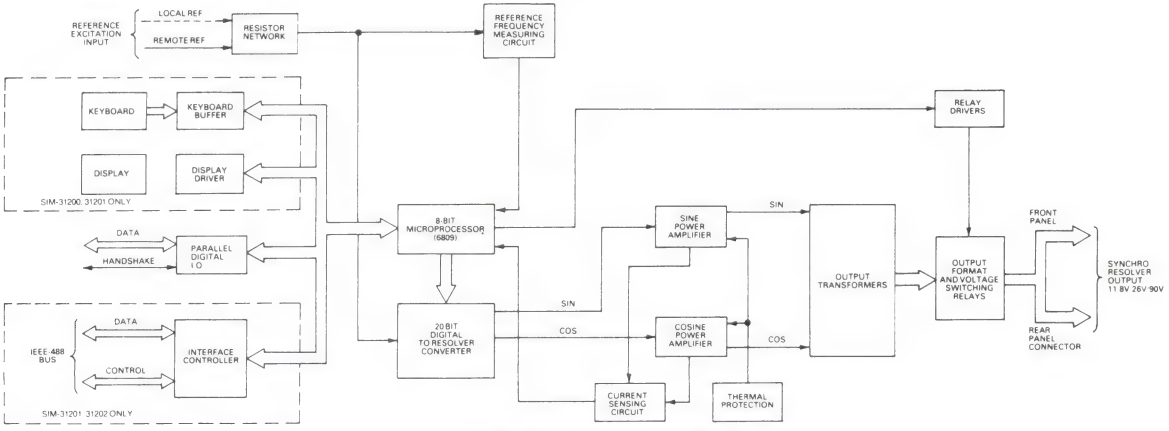


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, ±10% reference voltage and frequency variation, and ±10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	.001° BCD; .00034° Binary
ACCURACY*	
47Hz-2KHz	±.003° (no load); ±.004° 1.5VA load; ±.008° 5VA load
10KHz	±.015° (no load); ±.03° 1.5VA load.
	*Accuracy degrades as a linear function of frequency from 2KHz to 11KHz. For higher accuracy consult factory.
ANGLE RANGE	000.000° To 359.999° (BCD) 000.000° To 359.99966° (Binary); continuous rotation
DISPLAY	
Output Angle	6-digit, 7-segment LED with polarized filter
Status Indications	Local, Remote, Synchro, Resolver, 11.8V, 26V., 90V., Overload, Reference Missing LEDs.
DIGITAL INPUT/OUT	
Parallel I/O Type	TTL Compatible Open = Logic 1; Ground = Logic 0
Inputs	
Loading	1 LS TTL Load
BCD/Binary Angle Input	Switch selectable format; 22 data lines; 6 decades BCD, or 20-bit binary; 200°, 100°, 180/80°, 90/40°, 45/20°, 22.5/10°, 11.25/8°, 5.625/4°, 2.812/2°, 1.406/1°, .703/.8°, .351/.4°, .176/.2°, .088/.1°, .044/.08°, .022/.4°, .011/.2°, .0056/.01°, .0027/.008°, .0014/.004°, .00069/.002°, .00034/.001°
Other Inputs	Synchro/Resolver, 11.8 volt, 90 volt, Data Track/Hold, MPU Reset
Outputs	
Drive Capability	5 Standard TTL loads
Signal	Reference Missing, Overload, Parallel Input Ready, Binary/BCD, GPIB/Parallel
GPIB IEEE Interface	Optional, See Below
REFERENCE INPUT	
Input Type	Transformer Isolated
Voltage Levels	26 VRMS/115 VRMS; Others Special: Consult Factory
Frequency	47Hz. - 11KHz.
Input Impedance	26V-50K min., 115V-230K min.
Harmonic Content	10% maximum allowable
Location	Through either front panel or rear connector for both local and remote modes.
Max. Allowable Voltage Operating	127V for 115V nominal 29V for 26V nominal
Max. Allowable Voltage No Damage	35V for 26V nominal 150V for 115V nominal
Breakdown Voltage	±500 VDC to Logic Ground
FACTORY CALIBRATION FREQUENCIES AND RANGES	
Synchro	90V, 47-150Hz (Cal at 60Hz), 151-1000Hz (Cal 400Hz); 11.8V-360-2000Hz (Cal at 400Hz)
Resolver	11.8V-360-2000Hz (Cal at 400Hz); 2000Hz-11KHz (Cal at 10KHz) 90V-151-2000Hz (Cal at 400Hz)
User calibration frequencies	Anywhere within specified ranges.

PARAMETER	VALUE
SYNCHRO/RESOLVER OUTPUT	
Type of Output	Synchro (S1, S2, S3 outputs) or resolver (S1, S2, S3, S4 outputs) with transformer isolation.
Line-to-Line Output Voltages	Programmable 11.8, 26 and 90 VRMS
Output Accuracy	±0.5% nominal due to all causes
Output Locations	Front Panel and rear connector, active in both local and remote modes.
Minimum L-L Load Impedance Z_{L-L}	$90V_{L-L}$ / $26V_{L-L}$ / $11.8V_{L-L}$
Synchro (47-2000Hz)	1215 ohms / -- / 21 ohms
Resolver (47-2000Hz)	1620 ohms / 135 ohms / 28 ohms
Resolver (2-11KHz)	——— / ——— / 93 ohms
Drive capability	Will drive loads with any phase angle from −90° to +90°.
Time phase	±.4° max. up to 2 KHz; ±1° at 11KHz with respect to reference input
Scale factor variation	±.025% simultaneous amplitude variation in all output lines as a function of digital angle
Protection	Momentary and continuous overcurrent protection; Output overload and reference input missing indications to user; Over temperature shutdown protection
Breakdown voltage	±500 VDC to GND
RESPONSE TIME	7.5ms max. upon receipt of input from parallel I/O or IEEE bus
FACTORY CALIBRATION	Instrument not specified for 26V Synchro operation
WARM UP TIME	30 sec. max.
FRONT PANEL CONTROLS	
Power	On/Off switch
Keyboard	Local/Remote, Synchro/Resolver, 11.8/26/90 volt Lamp Test, Angle "Delta" Entry, Increment/Decrement Angle, clear entry, decimal point, calibrate, angle entry
FRONT PANEL I/O	Reference Input (115R, 26R, RL): Synchro/Resolver Output (S1, S2, S3, S4); Case Ground; Digital Ground
REAR PANEL	
Connectors	J1 (50-Pin Analog/Digital I/O) Standard** J2 (24-pin GPIB I/O) optional** J3 (3-pin Power)
Control Switches	GPIB/Parallel (Optional) BCD/Binary GPIB Address-5 bits (Optional) 115/230 volt-Power Input
POWER INPUT	
Connector	Rear Connector including internal EMI/RFI filter, separate line cord supplied.
Voltage	Switch selectable 115/230V rms ±10%
Power frequency	47 to 63Hz (For 400Hz line power operation contact factory)
Fuse (on rear panel)	Buss, GMW-2, 2 Amp
Isolation	Transformer
PHYSICAL CHARACTERISTICS	
Size	8 1/8 x 3 1/2 x 14 1/2 Inches (20.6 x 8.9 x 36.8 cm.)
Weight	14 lbs (6.4 kg.)
Mounting**	Half-rack; full-rack
TEMPERATURE RANGE	
Operating	0° to 50°C
Storage	−65°C to +100°C

**See Ordering Information

TECHNICAL INFORMATION

INTRODUCTION

The SIM-31200 Series Simulator is a third generation unit featuring μP control and calibration. It is available in three configurations:

1. SIM-31200 is the standard bench top unit with front panel controls and a parallel digital output at the rear for remote operation.
2. SIM-31201 is the same as the SIM-31200 but with optional IEEE GPIB interface.
3. SIM-31202 is a unit optimized for ATE applications. It has a blank front panel to prevent inadvertent operation. The interface is solely through the rear panel IEEE GPIB port or parallel digital I/O.

All versions may be bench operated or rack mounted with appropriate mounting hardware.

KEYBOARD OPERATION

Local operation of the SIM-31200 Series is through a 16 pad keyboard, which allows for selection of operating mode, output level and format, test and calibration functions, six digit numerical angle programming, digital angle input enable and angle increment/decrement with programmable delta angle. The keyboard has 10 dual-function keys (highlighted in grey in Figure 2) which are identified by the presence of numerals in the lower case position. The remaining keys are single function keys. A description of the keyboard functions is provided in Table 1.

FRONT PANEL CONNECTIONS

Front panel signal output terminals (S1, S2, S3 and S4) permit direct access to selected signal levels in synchro or resolver format. The reference input terminals may be used for local or remote operation to provide the instrument with 115V or 26V reference excitation. Care must be taken to operate with only *one* reference source (rear connector or front panel terminals). Accidental duplication of reference input signals will not damage the instrument, but will cause errors in angular information in the display (SIM-31200 and SIM-31202) and synchro and resolver outputs on all models.

CALIBRATION

The internal microprocessor operates in conjunction with a non-volatile RAM and the reference measuring circuit (Figure 1) to implement a calibration scheme. This allows compensation for angular errors caused by the output transformers. The procedure will allow calibration to a total error that is equal to or less than ±.003°. A detailed calibration procedure is in the Instruction Manual supplied with each instrument.

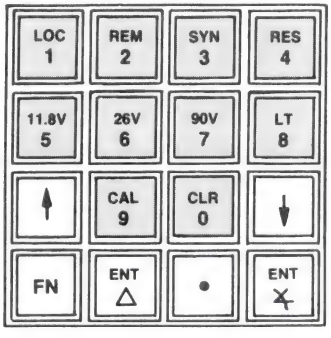
DIGITAL PARALLEL I/O

Operating any of the Simulator models through the rear parallel digital I/O port requires that the instrument be connected according to the connection scheme shown in the Parallel I/O (J1) Pin Function Table. The user must also position the rear panel switch (PRL) to select the parallel interface and then select the proper angle format with the Binary or BCD (BIN/BCD) switch. The user must manually set the remote mode, since all models, except the SIM-31202, initialize to the local mode when power is turned on.

REMOTE OPERATION VIA THE IEEE GPIB

When operating via the IEEE-488 Interface, a remote mode command signal is provided by the Interface (SIM-31201 and SIM-31202). The front panel indicator lights will illuminate, even though the instrument is controlled remotely (except SIM-31202). They will function as if in the local operating mode, by indicating synchro or resolver signal output and line-to-line voltage level. In the event of a fault condition, such as current overload or reference voltage drop below 5V rms (26V reference) or 22V rms (115V reference) the front panel lights (OVLD or REF LOSS) will illuminate in either local or remote mode.

The SIM-31202 requires that all signals access the device through the J1 Interface Connector (rear panel). The user must further insure that the rear panel function switches are set for proper signal and power input (see Mechanical Outline). If operating SIM-31201 or SIM-31202 with IEEE-488 General Purpose Interface Bus (GPIB), the user must program the appropriate 5-digit device address, select the GPIB position and BCD or Binary code on the rear panel to facilitate communication via the IEEE-488 data bus. All GPIB signals are provided to the J2 Interface Connector with the exception of the Reference input, which must be supplied through the J1 Connector or the appropriate front panel binding post.



Indicates dual function key

FIGURE 2. SIM-31200 SERIES KEYBOARD (LOCAL OPERATION)

DRIVE CAPABILITY

SIM-31200 Series Simulators can drive up to 5 VA over the frequency range of 47 Hz to 2 kHz and 1.5 VA at frequencies up to 10 kHz. When driving tuned loads the tuning capacitors should not exceed .01μF on 90 V L-L synchros or resolvers, .15μF on 26V L-L resolvers, .75μF on 11.8V L-L synchros or resolvers or .4μF on 11.8V resolvers operating over 2 kHz. These are beyond the range of most tuning capacitors and so should not be a problem.

KEYBOARD FUNCTIONS

KEY-BOARD PAD	FN ENABLED FUNCTION*	FUNCTION**
FN	When depressed, enables user to select upper functions of the dual function keys.	N/A
LOC 1	Selects local mode.	Enters numerical value of "1".
REM 2	Selects remote mode.	Enters numerical value of "2".
SYN 3	Selects synchro output.	Enters numerical value of "3".
RES 4	Selects resolver output.	Enters numerical value of "4".
11.8V 5	Selects 11.8V output level.	Enters numerical value of "5".
26V 6	Selects 26V output level.	Enters numerical value of "6".
90V 7	Selects 90V output level.	Enters numerical value of "7".
LT 8	Initiates lamp test for approximately 1 second displaying 888.888 and causing all front panel indicators to light.	Enters numerical value of "8".
▲	N/A	Increments input angle by the delta value.
CAL 9	Used for instrument calibration.	Enters numerical value of "9".
CLR 0	Clears angular display.	Enters numerical value of "0".
ENT ▲	N/A	Enters selected delta angle into instrument
▼	N/A	Decrements input angle by delta value.
ENT	N/A	Enters displayed angle into instrument
•	N/A	Enters numerical value representing a fractional part of an angle entry.

*FN enabled functions are called out in red alphanumerics and are collocated with angle entry digits, which are blue.

**Functions are activated after FN configuration has been selected.

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PARALLEL I/O J1 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	Spare Pin	17	.0027/.008°	38	DATA T/$\overline{H}$ Handshake Input "1" = Track Parallel Angle Input Data "0" = Hold Parallel Angle Input Data
2	Spare Pin	18	115R } Remote Ref Input		
3	Case GND	19	RL		
4	J1 Return	20	26R		
5	SYN/RES Input[1] "1" = Synchro "0" = Resolver	21	GPIB/$\overline{\text{PARALLEL}}$ Input/Output[4]		
		22	Signal Output Programming[2]	39	BIN/$\overline{\text{BCD}}$ "0" = Binary I/O "1" = BCD I/O
6	Output Level Programming[2]	23	NU/100°		
7	90/40° [3]	24	180/80°		
8	22.5/10°	25	1.406/1°	40	NU/200°
9	5.625/4°	26	11.25/8°	41	45/20°
10	.703/.8°	27	.088/.1°	42	2.812/2°
11	.176/.2°	28	$\underline{\text{Spare}}$	43	.352/.4°
12	$\overline{\text{MPU RESET}}$ Input "1" = Normal Operation "0" = Resets Microprocessor	29	$\overline{\text{REF MISSING}}$ Output	44	Spare
		30	$\overline{\text{PARALLEL INPUT RDY}}$ Output[1]	45	Converter SIN/COS Common (6)
		31	Spare	46	Converter SIN
		32	.0055/.01°	47	Converter COS
13	OVERLOAD Output "1" = Overcurrent Sensed "0" = No Overcurrent	33	.0014/.004°	48	.044/.08°
		34	S2	49	Spare
		35	S3 } Synchro/Resolver Output	50	.0003/.001°
14	.022/.04°	36	S4[5]		
15	.011/.002°	37	S1		
16	.0007/.002°				

Notes: (1) Pins used in all parallel I/O modes only.
(2) Signal output programming is as follows:

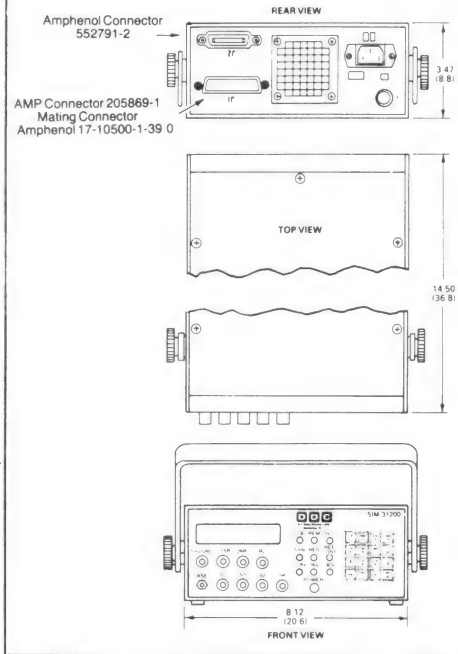
J1-6 Logic	J1-22 Logic	L-L Voltage Level
"0"	"0"	90 Volts
"0"	"1"	26 Volts
"1"	"0"	Illegal
"1"	"1"	11.8 Volts

(3) J1 Connector pins 7-11, 14-17, 23-27, 32-33, 40-43, 48 and 50 are Binary/BCD (NU = not used Binary)
(4) Switch Selectable (rear panel)
"1" = IEEE-488 Bus controlled "0" = Parallel I/O controlled
(5) S4 used for resolver operation only.
(6) Converter SIN/COS Common is to be used only for the analog calibration of the internal Digital to Resolver Converter Module. Refer to the SIM-31200 Manual for calibration procedures. It should not be connected to J1 Return or other system grounds

IEEE-488 PIN FUNCTIONS

Pin	Function
1	D101 Data I/O Line
2	D102 Data I/O Line
3	D103 Data I/O Line
4	D104 Data I/O Line
5	EOI
6	DAV
7	RFD
8	DAC
9	IFC
10	SRQ
11	ATN
12	Case GND
13	D105 Data I/O Line
14	D106 Data I/O Line
15	D107 Data I/O Line
16	D108 Data I/O Line
17	REN
18-24	GND

MECHANICAL OUTLINE Dimensions in inches (centimeters).



ORDERING INFORMATION

All instruments are supplied with detachable line cord, mating connector (J1) and instruction manual.

SIM-31200
└ Options:
0 = Bench top with keyboard
1 = Bench top with keyboard and IEEE-488
2 = Blank front panel with IEEE-488

High Frequency Option (SIM-31205) Available (contact factory)

Notes: 1. SIM-31201 and SIM-31202 are supplied with carry/support handle. For ½ rack mounting brackets order P.N 33395. For full rack mounting brackets order P/N 33396.
2. SIM-31202 is supplied with ½ rack mounting brackets. For full rack mounting brackets order P/N 33396.

SIM-31203 ADDENDUM

The SIM-31203 is identical to the SIM-31200 series with the addition of "rate" mode.

The implementation of the new Rate feature takes advantage of the fact that the main Firmware loop in the SIM-31200 is interrupt driven by a 20 millisecond timer (ie. 50 times a second). What we have done is to utilize this consistent 20 millisecond clock as a time base for stepping the Synchro/Resolver output of the Simulator. The amount that the output steps each interval is controlled by the Delta Angle function already incorporated in the SIM-31200. This implementation does however require that the user calculate the Delta Angle (ie. step size) required for the desired rotational rate. The formula for calculating the Delta Angle knowing the desired output rate in degrees/second is the following:

Delta Angle = Desired rate * 0.02

The limitation on the slowest possible programmable rate is based on the fact that the smallest programmable Delta Angle is 0.001 Degrees. Therefore the slowest programmable Rate (and also the resolution of the Rate feature) is 50 * 0.001 deg/sec or 0.05 deg/sec. The upper limit for the Rate feature is basically meaningless as it can theoretically be programmed for a rate of 360 * 50 = 18000 degrees/second.

Because of the implementation technique utilized only linear rates (constant velocity) are available, however the output can be programmed for either the Positive of Negative rotation. The Rate feature is only available via the IEEE bus as no modifications have been made to the Keyboard of associated circuitry. It should also be noted that because of time restraints the display is not updated while in the Rate mode. Finally, in order to provide as much flexibility as possible the Delta Angle, the Angle, and the Direction can be changed while in the Rate mode should someone find it advantageous to do this.

The four new IEEE commands added to the SIM-31200 to facilitate the Rate feature are as follows:

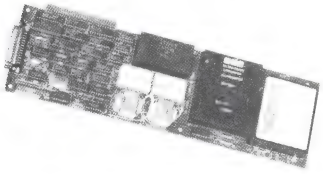
G	Starts the rotation
H	Halts the rotation
I	Positive (Increasing angle) Rotation
J	Negative (Decreasing angle) Rotation

Typical operation of the Rate feature would involve calculating and programming the Delta Angle, programming the desired direction, and then issuing the start command.

ORDERING INFORMATION: SIM-31203

SIM-36010

SYNCHRO/RESOLVER ANGLE SIMULATOR IBM PC® CARD INSTRUMENT



PRELIMINARY

DESCRIPTION

The SIM-36010 is a full size IBM PC card containing a broadband, high-accuracy instrumentation-grade Synchro/Resolver Simulator Instrument. The instrument accepts either a 26 Vrms or 115 Vrms Reference signal and can provide Synchro or Resolver output signals at 11.8, 26, or 90 Volts Line-to-Line with a drive capability of 1.5 VA. The SIM-36010 also includes a programmable Dynamic Rotation feature which provides for a programmable constant rate, either clockwise or counterclockwise, from 0.17 degrees/second up to 30.5 rps. If nonlinear motion is required provisions are made for external Rate Clock and Direction signals.

Demonstration software, which shows the SIM-36010 capabilities is available with the card.

APPLICATIONS

The SIM-36010 is a versatile high-accuracy, high-drive capability Synchro/Resolver Simulator Instrument for IBM PC based test systems. Data to-and-from the instrument is more than an order-of-magnitude faster than conventional IEEE bus test systems, because the card plugs directly into the PC bus structure. It is ideal for use as a stand-alone angle simulator in the engineering lab or as part of the PC based automatic test equipment (ATE).

FEATURES

- *ACCURACY OF ± 25 ARC SECONDS NO LOAD, ± 36 ARC SECONDS FULL LOAD*
- *1.5 VA DRIVE CAPABILITY*
- *PROGRAMMABLE DYNAMIC ROTATION 0.17 DEG/SEC TO 30.5 RPS*
- *± 0.025% SCALE FACTOR VARIATION*
- *BROADBAND FREQUENCY COVERAGE 360 Hz TO 5,000 Hz*
- *FAULT REGISTER*

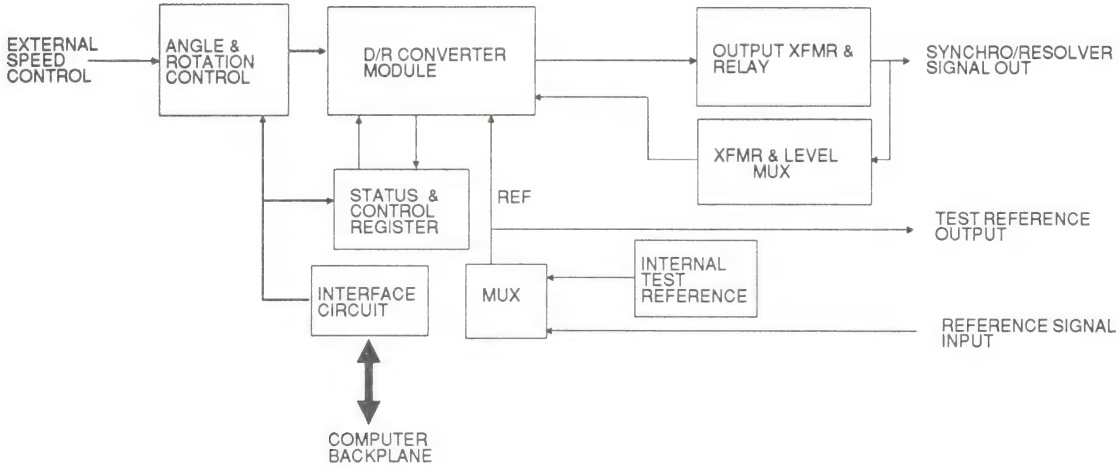


FIGURE 1. SIM-36010 BLOCK DIAGRAM

TABLE 1. SIM-36010 SPECIFICATIONS		
PARAMETER	**UNIT**	**VALUE**
RESOLUTION	Bits	16
ACCURACY	Arc Sec.	25 No Load, 36 Full Load
ANGULAR RANGE	Degrees	0 to 360
REFERENCE INPUT		
Type		transformer isolated
Voltage	Vrms	26/115 programmable
Frequency	Hz	360 - 5,000
Breakdown Voltage	V	1000 min.
Harmonic Content	%	10 max for full accurracy
SIGNAL OUTPUT		
Type		transformer isolated
Format		synchro or resolver
Voltages L-L	V L-L	11.8, 26, and 90
Drive Capability	VA	1.5
Scale Factor	%	± 2.5
Scale Factor Variation with angle	%	± 0.025
Protection		output overload thermal overload
Breakdown Voltage	V	1000 min.
DYNAMIC ROTATION (INT)		
Rotation		constant rate CW or CCW
Resolution		12 bits binary plus sign
Range 1 (Output Steps of 0.0055 Deg.)	Deg/Sec	0.17 min (LSB Weight) 686.48 (1.91 RPS) max
Range 2 (Output Steps of 0.088 Deg.)	Deg/Sec	2.68 min (LSB Weight) 10983.6 (30.5 RPS) max
DYNAMIC ROTATION (EXT)		
Range 1	Deg	0.0055 per clock tick
Range 2	Deg	0.088 per clock tick
Direction		CW or CCW
PROGRAMMABLE FEATURES		
L-L Voltage Output	—	—
Ref Level (115/26Vrms)	—	—
Synchro/Resolver	—	—
Dynamic Rate and Direction	—	—
Int/Ext Rate Signals	—	—
Disconnect	—	—
POWER SUPPLY	V	+5v, 400mA max +12V, 500mA max
TEMPERATURE RANGE		
Operating	°C	0 to +70
Storage	°C	-65 to +150

INTRODUCTION

The SIM-36010 is a full size IBM PC card which contains a broadband instrument grade Digital to Synchro/Resolver converter. The output signals are fully transformer isolated and the card can be programmed to generate 11.8, 26, or 90 Volts Line-to-Line in either Synchro or Resolver format over the frequency range of 360 Hz to 5000 Hz. The Simulator provides 16 bits of resolution and has a accuracy of ± 25 arc seconds at no load and ± 36 arc seconds at full load. The digital binary angular information is presented to the converter as two bytes of information (Most Significant Byte and Least Significant Byte). This data is transparently latched into the converter via double buffered latches thereby presenting the 16 bits of data to the converter simultaneously. The Simulator can drive a 1.5 VA load and contains full thermal and overload protection circuitry. Two fault signals available. The $\overline{BIT}$ signal is asserted during an electrical or thermal overload condition on the output amplifier, and the $\overline{LOR}$ signal is asserted upon detection of a missing input Reference signal.

The Dynamic Rotation feature provides for a constant clockwise or counterclockwise rotation in two ranges. The low range covers the range from 0.1676 degrees/second to 686.4779 degrees/second with a resolution of 0.1676 degrees/second, and the high range covers the range of 2.6822 degrees/second to 10983.6459 degrees/second (30.5101 RPS) with a resolution of 2.6822 degrees/second. Provisions for external rate and direction inputs are provided for special applications where very low rates or nonlinear rotation is required.

A block diagram of the SIM-36010 is shown in Figure 1.

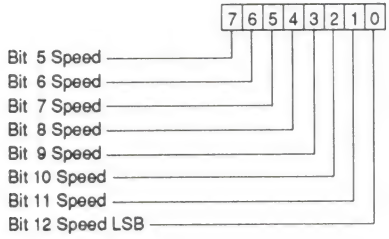
INTERNAL REGISTERS

REGISTER ADDRESSING

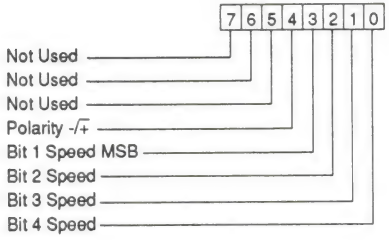
The SIM-36010 is addressed in typical Base Address and Offset fashion and uses 8 contiguous bytes of memory in the I/O address space. To decode these 8 bytes requires the use of the three LSBs of the I/O address. The remaining 7 address lines are used for setting the Base Address via a DIP switch located on the circuit card assembly. The Base Address of the card is preset at the factory to HEX address 300. In this configuration the card will occupy the address space of 300h to 307h. Table 4 shows the DIP switch settings as the card leaves the factory. The base address can be changed to any address from 000h to 3F8h in increments of 8 using Table 4 as a reference. Table 2 contains a I/O Memory Map of the SIM-36010.

TABLE 2.				
A2	**A1**	**A0**	**I/O Write**	**I/O Read**
0	0	0	NOT USED	NOT USED
0	0	1	NOT USED	NOT USED
0	1	0	SPEED LSBs	NOT USED
0	1	1	SPEED MSBs & POLARITY	NOT USED
1	0	0	CONTROL WORD A	STATUS REGISTER
1	0	1	CONTROL WORD B	NOT USED
1	1	0	ANGLE LSBs	NOT USED
1	1	1	ANGLE MSBs	NOT USED

SPEED LSBs BIT MAP



SPEED MSBs & POLARITY BIT MAP



- Polarity -/+ - A logic high for this bit causes the dynamic rotation to be in the direction of decreasing angular values. A logic low for this bit causes the dynamic rotation to be in the direction of increasing angular values.
- Speed bits 1-12 - This binary value sets the rate of rotational velocity. The speed data is represented as a 12 bit binary word which can have a value from 0 to 4095. This word is related to the Low-Range rotational velocity output using the Internal 125 kHz clock as follows:

$$\text{Rotation (Deg/Sec)} = \frac{360}{65536} \times 125{,}000 \times \frac{\text{Speed Data}}{4096}$$

$$= 0.167638063 \times \text{Speed Data}$$

If the High-Speed Range is selected (see bit 1 in control word B) the output rotational rate will be 16 times faster.

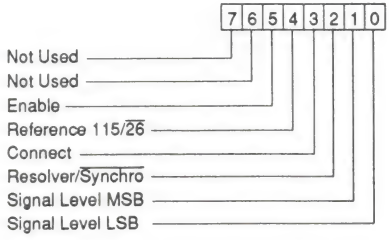
For an External Rate Clock the rotational velocity in the Low Range will be

$$\text{Rotation (Deg/Sec)} = \frac{360}{65536} \times \text{Ext clock}$$

In the High Range the rate will be 16 times faster.

NOTE: For a discussion on decimal to binary conversion techniques refer to the section headed Binary Angular Data, which follows.

CONTROL WORD A BIT MAP



- Enable - A logic high for this bit enables the output power driver of the Simulator. A logic low disables the output drive stage.
- Reference 115/26 - A logic high for this bit configures the converter to accept a Reference signal of 115 Vrms, a logic low configures the card to accept a 26 Vrms Reference.
- Connect - A logic high for this bit energizes the relays which connect the Synchro/Resolver output signals to the Output pins of the I/O connector on the circuit card assembly. A logic low disconnects the Simulator output signals from the Output pins 7 through 10 of the I/O connector. This bit is used to disconnect the Simulator output from the external test equipment.

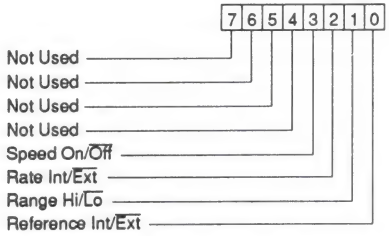
NOTE: When the Simulator output signals are disconnected from the Output pins 7 through 10 of the I/O connector, they are switched to pins 19 through 22.

- Resolver/Synchro - A logic high for this bit configures the Simulator to generate Resolver format output signals, a logic low configures the card to generate Synchro format signals.
- Signal level bits - These two bits set the Line-to-Line signal voltage in accordance with Table 3.

TABLE 3.

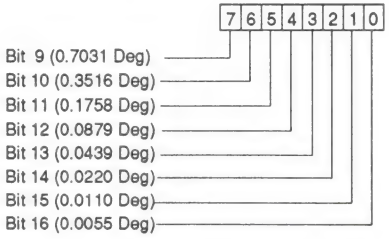
MSB	LSB	INPUT SELECT
0	0	11.8 Volt L-L input
0	1	11.8 Volt L-L input
1	0	26 Volt L-L
1	1	90 Volt L-L

CONTROL WORD B BIT MAP

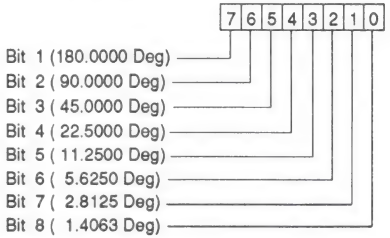


- Speed On/$\overline{\text{Off}}$ - A logic high for this bit enables the Simulator to rotate at the programmed dynamic rotation value. A logic low inhibits the dynamic rotation of the Simulator.
- Rate Int/$\overline{\text{Ext}}$ - A logic high for this bit selects the internal programmable dynamic rotation clock. A logic low selects an externally supplied clock.
- Range Hi/$\overline{\text{Lo}}$ - a logic high for this bit selects the High dynamic rotation range i.e., 2.6822 Degrees/Second to 10983.6459 Degrees/Second (30.5101 RPS). A logic low selects the Low dynamic range of 0.1676 Degrees/Second to 686.4779 Degrees/second. From a hardware point of view this bit controls whether the rate clock is connected to the LSB (bit 16) or the 5th LSB (bit 12) of the up/down counter driving the Digital to Synchro/Resolver Converter in the Simulator.
- Reference Int/$\overline{\text{Ext}}$ - A logic high for this bit selects the internally generated reference signal. A logic low selects a externally supplied reference.

ANGLE LSBs BIT MAP



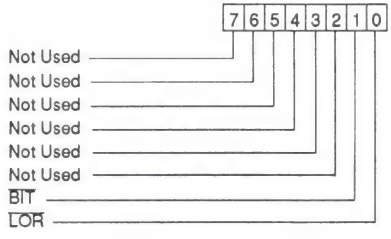
ANGLE MSBs BIT MAP



- Binary Angle bits 1-16 - This binary value sets the Synchro/Resolver output angle. NOTE: For a discussion on decimal to binary conversion techniques refer to the section headed Binary Angular Data which follows.

IMPORTANT - When the Binary Angular Data is loaded into the SIM-36010 it MUST be loaded into the registers Least Significant Byte first followed by the Most Significant Byte. If this sequence is not followed the double buffering circuitry for the associated converter will not function properly and the angle generated will be incorrect (the new MSB data will be used with the previous LSB data, and the new LSB data will be put into temporary storage to be used for the next update).

STATUS REGISTER BIT MAP



- $\overline{\text{BIT}}$ - This bit is normally at a logic high state. A logic low for this bit indicates that a fault condition exists in the driver stage of the Simulator. This fault may be due to an electrical overload on the Simulator output, a thermal shutdown condition in the power stage of the Simulator, or in some cases it may occur for a short time duration if a large angular change is made and the power stage momentarily goes into current limit.
- $\overline{\text{LOR}}$ - This bit is normally at a logic high state. A logic low for this bit indicates that the Reference input to the Simulator is missing (Loss-Of-Reference) or too low.

G

BINARY ANGULAR DATA

The Most Significant Bit of the Most Significant Byte represents the Binary Angular value of 180 Degrees. The second Most Significant Bit of the same Byte represents the angular value of 90 Degrees, and the third represents 45 Degrees, etc., down to the Least Significant Bit of this Byte which represents 1.406 Degrees (rounded to 3 decimal places).

The Most Significant Bit of the Least Significant Byte represents 0.703 Degrees (rounded to 3 decimal places) and following suit the Least Significant Bit has the weight of 0.005 Degrees (rounded to 3 decimal places).

Algorithms to convert Decimal angular data into Binary angular data consist of testing the magnitude of the Decimal value against the Binary values to see which Binary values can be added together in order to come closest to the Decimal value. This test generally starts with the most significant Binary bit weight of 180 Degrees and determines whether it is more or less than the Decimal value. If the Decimal value is larger than 180 degrees then obviously this Binary bit is part of the final Binary value, if the Decimal value is less than 180 degrees then this Bit is not part of the final Binary value. This same test is now done using the second Binary Bit (90 degrees) and so on down to the LSB of 0.005 Degrees.

For example to convert 135.703 Degrees to a Binary value the following steps are taken.

- 1.The Most Significant Binary bit is 180 Degrees and is obviously too large to be contained in the final Binary value so it is set to logic 0.
- 2.The Second Binary Bit has the value of 90 Degrees which is smaller than the Decimal value of 135.703 Degrees. It is obviously part of the final Binary value so it is set to logic 1 and 90 Degrees is subtracted from the Decimal value leaving 45.703 degrees.
- 3.The Third Binary bit has the value of 45 Degrees which again is smaller than the Decimal remainder of 45.703. It obviously is part of the final Binary value so it is set to logic 1 and 45 Degrees is subtracted from the Decimal remainder leaving 0.703 Degrees.
- 4.The Forth Binary Bit has a value of 22.5 Degrees which is too big to fit. It is set of logic 0 and the testing continues using the Decimal value of 0.703. So far we have tested the 4 MSBs of the Binary values and the Binary solution at this point is "0 1 1 0" with 12 more Binary Bits to test.
- 5.The 5th, 6th, 7th, and 8th Binary bits are all too large and are therefore set to logic 0. The Binary value at this point is "0 1 1 0 0 0 0 0" with 8 more Binary Bits to test.
- 6.The Binary Bit weight of the 9th bit is 0.703 Degrees and it fits exactly into the Decimal value of 0.703. The Binary Bit is therefore set to logic 1 and the Binary answer at this point is "0 1 1 0 0 0 0 0 1". The Binary value of 0.703 is subtracted from the Decimal Value and the remainder is 0.
- 7.As the Decimal remainder is now 0 obviously none of the remaining Binary Bits will Fit into the Decimal value so they can all be set to logic 0. The final Binary answer is therefore "0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0"
- 8.The Most Significant Byte of the Binary angle contains the value "0 1 1 0 0 0 0 0" and the Least Significant Byte contains the Binary value "1 0 0 0 0 0 0 0".

TIMING REQUIREMENTS

Data to and from the SIM-36010 card is controlled by the computer using standard I/O Read/Write cycles. All of the interface logic uses high-speed components, allowing the card to be addressed in zero wait state time cycles, however the following precautions must be taken.

- Relays are used to switch the Synchro/Resolver Line-to-Line levels and to implement the Connect feature. Enough time must be allocated for the relays to settle out (around 10 ms) so that the Simulator output is stable.
- If a step input is given to the Simulator allow at least 50 ms for the output to stabilize.
- The binary data value for the output angle must be loaded Least Significant Byte first (the 8 LSBs of the angle) followed by the Most Significant Byte (the 8 MSBs of the angle), or the double buffering scheme will not function properly causing an incorrect angle to be generated.
- If the output power driver is disabled (Control Word A, bit 5), the simulator feedback loop may drift into saturation. It could take up to 3 seconds to stabilize after the output power driver is re-enabled.

BASE ADDRESS SWITCH

The Base Address of the card is preset at the factory to HEX 300 as shown in Table 4. The Base Address can be changed to any address from 000h to 3F8h increments of 8 using the Table 4 as a reference.

TABLE 4.

Address	Switch	OFF(OPEN)	ON	Function
A9	SW4	X		HEX 3
A8	SW5	X		
A7	SW6		X	HEX 0
A6	SW7		X	
A5	SW8		X	
A4	SW9		X	
A3	SW10		X	P/O HEX 0
A2		—	—	A0, A1, and A2 are
A1		—	—	not part of the
A0		—	—	base address

CONNECTORS

SIGNAL I/O CONNECTOR

The Simulator I/O signals are brought off the circuit card assembly via a 25 pin 'D' type connector. The signal connections to this connector are shown in Table 5.

TABLE 5.

SIGNAL	PIN
S1 Output	10
S2 Output	9
S3 Output	8
S4 Output	7
S1 Output (For alternate output)	22
S2 Output (For alternate output)	21
S3 Output (For alternate output)	20
S4 Output (For alternate output)	19
RH Input	12
RL Input	11
Test Reference (For optional API-36005)	13
External Rate Polarity Input	5
External Rate Input	4
Circuit Ground	1, 6, 23, 25

COMPUTER INTERFACE CONNECTOR

The SIM-36010 inputs place one LS-TTL load on each of the IBM data bus lines and uses one standard TTL signal level to drive the data bus. The pin number and function of the computer interface signals are listed in Table 6.

TABLE 6. SIM-36010 PIN FUNCTIONS

PIN NO.	SIGNAL NAME	FUNCTION
A1	$\overline{\text{I/O CHECK}}$	NOT USED
A2	D7	DATA BIT 7
A3	D6	DATA BIT 6
A4	D5	DATA BIT 5
A5	D4	DATA BIT 4
A6	D3	DATA BIT 3
A7	D2	DATA BIT 2
A8	D1	DATA BIT 1
A9	D0	DATA BIT 0
A10	I/O READY	NOT USED
A11	AEN	ADDRESS ENABLE
A12	A19	NOT USED
A13	A18	NOT USED
A14	A17	NOT USED
A15	A16	NOT USED
A16	A15	NOT USED
A17	A14	NOT USED
A18	A13	NOT USED
A19	A12	NOT USED
A20	A11	NOT USED
A21	A10	NOT USED
A22	A9	ADDRESS BIT 9
A23	A8	ADDRESS BIT 8
A24	A7	ADDRESS BIT 7
A25	A6	ADDRESS BIT 6
A26	A5	ADDRESS BIT 5
A27	A4	ADDRESS BIT 4
A28	A3	ADDRESS BIT 3
A29	A2	ADDRESS BIT 2
A30	A1	ADDRESS BIT 1
A31	A0	ADDRESS BIT 0
B1	GROUND	GROUND
B2	RESET	SYSTEM RESET
B3	+5V	POWER SUPPLY
B4	IRQ2	NOT USED
B5	-5V	NOT USED
B6	DRQ2	NOT USED
B7	$\overline{\text{-12V}}$	NOT USED
B8	$\overline{\text{0WS}}$	NOT USED
B9	+12V	POWER SUPPLY
B10	GROUND	GROUND
B11	$\overline{\text{MEMW}}$	NOT USED
B12	$\overline{\text{MEMR}}$	NOT USED
B13	$\overline{\text{IOW}}$	I/O WRITE
B14	$\overline{\text{IOR}}$	I/O READ
B15	$\overline{\text{DACK3}}$	NOT USED
B16	DRQ3	NOT USED
B17	$\overline{\text{DACK1}}$	NOT USED
B18	DRQ1	NOT USED
B19	$\overline{\text{DACK0}}$	NOT USED
B20	CLOCK	NOT USED
B21	IRQ7	NOT USED
B22	IRQ6	NOT USED
B23	IRQ5	NOT USED
B24	IRQ4	NOT USED
B25	IRQ3	NOT USED
B26	$\overline{\text{DACK2}}$	NOT USED
B27	T/C	NOT USED
B28	ALE	NOT USED
B29	+5V	POWER SUPPLY
B30	OSC	NOT USED
B31	GROUND	GROUND

G

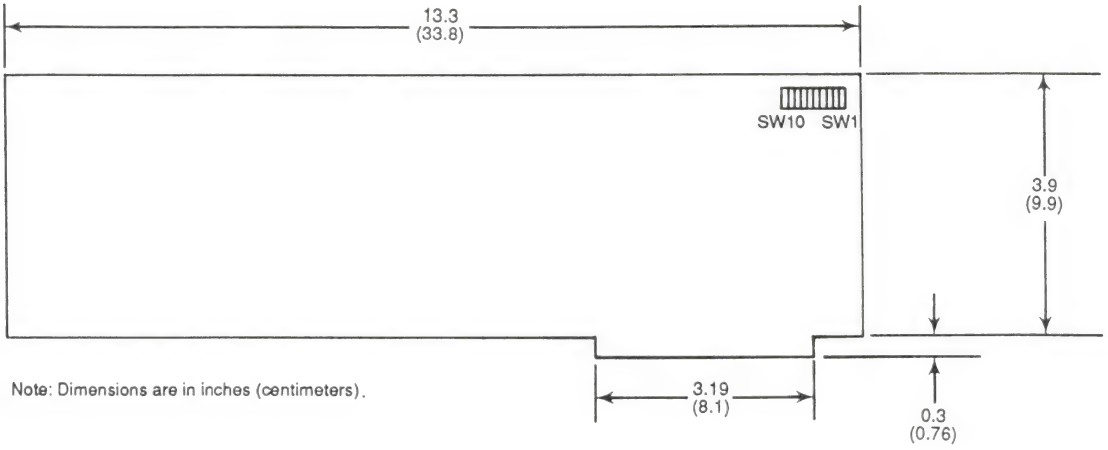


FIGURE 2. MECHANICAL OUTLINE
with DIP Switch location

ORDERING INFORMATION
SIM-36010

SR-103* AND HSR-103*

±.005° SYNCHRO AND RESOLVER ANGLE INDICATOR
Converts Synchro and Resolver Signals to BCD Angle

DESCRIPTION

The SR-103 and HSR-103 are improved high quality angle indicators used in precision synchro and resolver test equipment. They accept synchro or resolver signals at the rear connector and provide BCD angle output which is also displayed on the front panel. Intended primarily for dedicated applications, the SR-103 and HSR-103 are logic programmable via the rear connector and easily interfaced with computers and digital control equipment. An IEEE-488 bus adaptor is a standard option. Because they can accept a broad range of voltages and frequencies without programming and signal-to-reference phase shifts of up to ±50°, the SR-103 and HSR-103 are ideal for situations in which a variety of different inputs must be accommodated quickly.

Using a Type II servo loop for continuous tracking, these instruments have no velocity lag up to the specified tracking rates. There can be no hangup 180° away from the input angle. A fault indicator shows when the unit is not tracking the input signal, and an ambiguity indicator shows when the output data is changing. The SR-103 and HSR-103 require no adjustments or calibrations and logic is TTL compatible.

APPLICATIONS

The SR-103 and HSR-103 can be used wherever accurate angle information is required for display, control, testing purposes, or computation. Applications include production testing of synchros and resolvers, information translators in quality control systems, machine tool control, ship and aircraft navigation systems, and antenna positioning. The IEEE-488 adaptor option is convenient for interfacing these units with other instruments, for automatic test equipment (ATE) (see DBA-488 data sheet).

FEATURES

- *DOES NOT REQUIRE VOLTAGE OR FREQUENCY PROGRAMMING:*
  Automatically adjusts to reference levels of 10–150V and signal levels of 10–100V
  Broadband 47–1000 Hz frequency range
- *RESOLUTION AND ACCURACY:*
  SR-103 has 0.01° resolution and ±0.03° accuracy
  HSR-103 has 0.001° resolution and ±0.005° accuracy
- *TRANSFORMER ISOLATION FOR SIGNAL AND REFERENCE INPUTS*
- *TYPE II SERVO TRACKING LOOP:*
  No velocity lag and continuously available output for rates up to 2 rps (720°/sec)
- *LOGIC CONTROLS:*
  Converter Busy, Inhibit, High/Low Bandwidth, Unipolar/Bipolar display, Lamp Test
- *FAULT MONITOR INDICATES FAILURE TO TRACK*
- *DUAL SYNCHRO/RESOLVER INPUT CHANNELS WITH FRONT PANEL SELECTOR SWITCH*
- *TRANSFORMER ISOLATION FROM LINE VOLTAGE:*
  115/230V and 47–440 Hz power input

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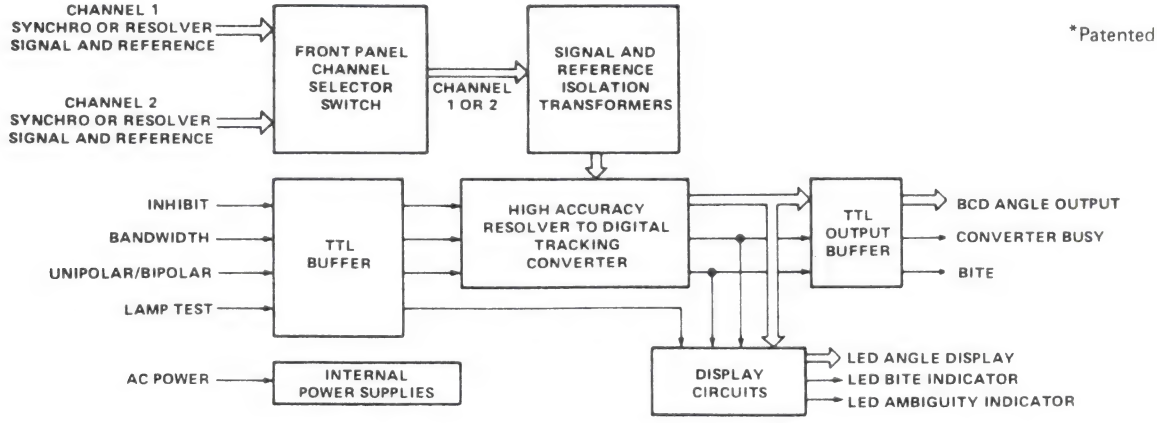
*Patented



SR-103 OR HSR-103 BLOCK DIAGRAM

SR-103* AND HSR-103*

SPECIFICATIONS

PARAMETER	VALUE	
	SR-103	HSR-103
RESOLUTION	0.01° (5 BCD digits)	0.001° (6 BCD digits)
ACCURACY (All Causes)	±0.03°	±0.005°
REPEATABILITY	Within 0.01°	Within 0.002°
ANGLE RANGE (Continuous Rotation)		
Unipolar	0° to +359.99°	0° to +359.999°
Bipolar	0° to ±179.99°	0° to ±179.999°
DISPLAY		
7-Segment 0.43" LED	5 digits	6 digits
REFERENCE INPUT		
Input Type	Transformer isolation	
Voltage Level	10–150V rms	
Frequency	47–1000 Hz	
Input Impedance	100 KΩ min	
Breakdown Voltage	1000V min to logic ground	
Harmonic Content	-10% max	
SIGNAL INPUTS		
Input Type	Synchro or Resolver, transformer isolated	
Line-to-Line Voltage	Auto-leveling, 10–100V	
Frequency	Same as reference	
Allowed Phase Shift	±50° max, relative to reference	
Input Impedance		
SR-103	150 KΩ min at 47 Hz 250 KΩ min between 60 and 1000 Hz	
HSR-103	1 MΩ min	
Breakdown Voltage	1000V min to logic ground	
DYNAMIC CHARACTERISTICS	**SR-103**	**HSR-103**
Tracking Rate (Full Accuracy)		
400 Hz	720°/sec	72°/sec
50–60 Hz	180°/sec	18°/sec
Settling Time (To Within 1 LSB)		
Lo Bandwidth (47–1000 Hz)	1.7 sec	8 sec
Hi Bandwidth (360–1000 Hz)	0.6 sec	3.5 sec
Open Loop Transfer Function	$G = \frac{A^2(\frac{S}{B}+1)}{S^2(\frac{S}{10B}+1)}$	
Lo Bandwidth (47–1000 Hz)	A = 18, B = 10	A = 13, B = 10
Hi Bandwidth (360–1000 Hz)	A = 86, B = 46	A = 42, B = 21

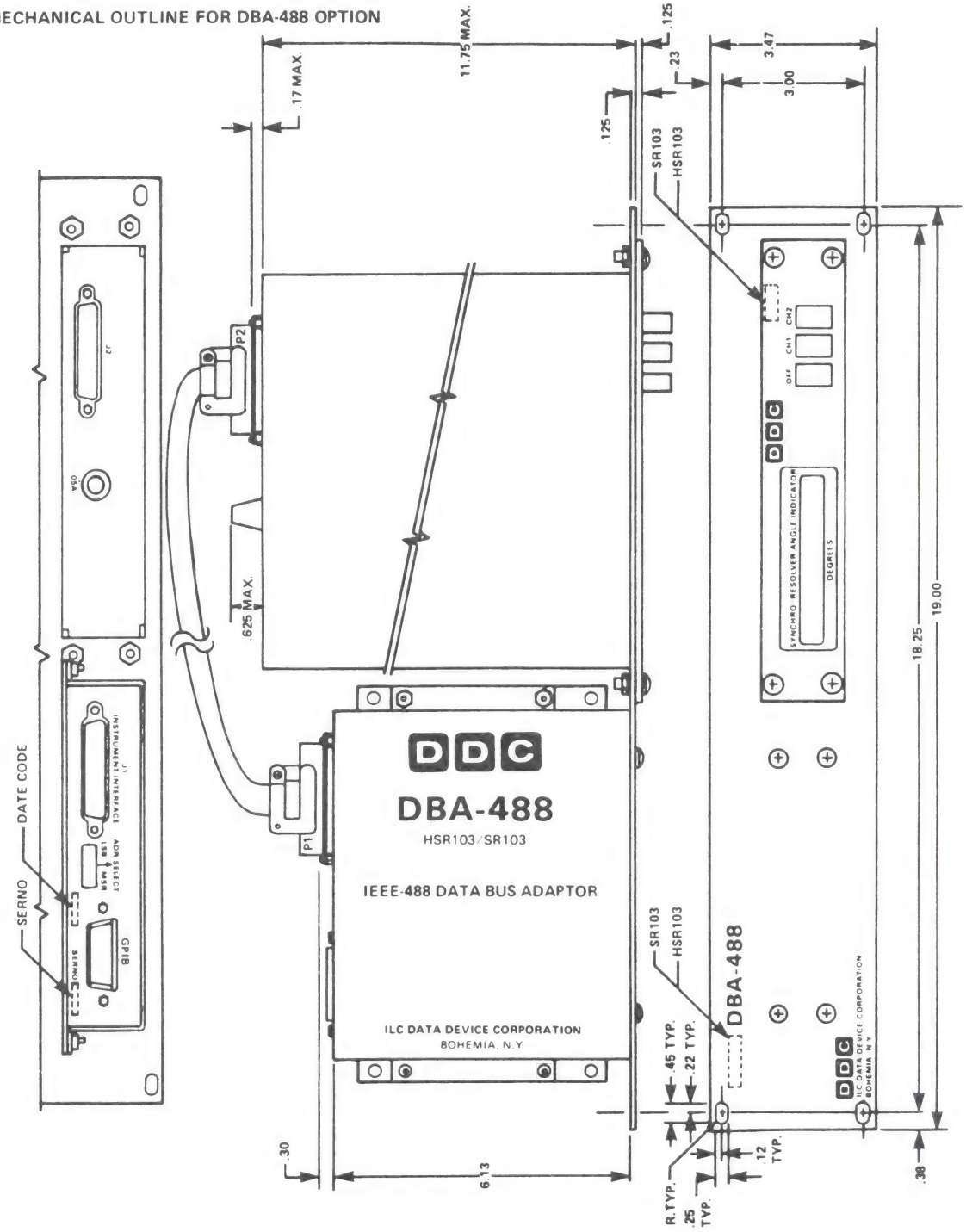
PARAMETER	VALUE
DIGITAL INPUTS (TTL Compatible)	
Loading	0.5 Std TTL loads max
Inhibit (INH)	"1" or open = track "0" or GND = inhibits
Bandwidth Selector (BW)	"1" or open = Lo Bandwidth (47–1000 Hz) "0" or GND = Hi Bandwidth (360–1000 Hz)
Unipolar/Bipolar Selector (U/B)	"1" or open = unipolar operation (0° to 360°) "0" or GND = bipolar operation (–180° to +180°)
Lamp Test	"1" or open = normal operation "1" or GND = all LED segments on
DIGITAL OUTPUTS (TTL Compatible)	
Drive Capability	4 Std TTL loads, buffered output
Synchro or Resolver Angle	Parallel data bits; BCD angle, positive logic MSB becomes minus sign for bipolar operation SR-103 has 5 decades, 18 lines HSR-103 has 6 decades, 22 lines
Converter Busy (CB)	4 µsec positive pulse, leading edge initiates conversion
BITE	Indicates tracking failure from any cause (including excessive speed or equipment malfunction). "1" = fault
FRONT PANEL CONTROLS	
CH1/CH2	Selects input channel to be displayed
ON/OFF	Main power control
TEMPERATURE RANGES	
Operating	0°C to +50°C
Storage	–65°C to +125°C
POWER INPUT	
Voltage	115V or 230V rms, selected by switch on chassis
Power	10 VA max
Frequency	47–500 Hz
Isolation	Transformer isolated
Breakdown Voltage	1000 VDC min to logic ground
PHYSICAL CHARACTERISTICS	
Size	11-3/4 x 9-1/2 x 1-3/4 inch (29.8 x 24.1 x 4.45 cm)
Weight	4 lbs (1.8 kg)

REAR CONNECTOR PIN ASSIGNMENTS

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	AC power high	20	Bandwidth control "1" or open = LO BW = 47-1000 Hz "0" or GND = HI BW = 360-1000 Hz	37	Spare pin
2	AC power low			38	Lamp Test control "1" or open = normal operation "0" or GND = all LED segments on
3	Case GND				
4	Digital GND (can be connected to case GND)	21	S1 } Channel 2 inputs. S4 for resolver use only.	39	Unipolar/Bipolar control "1" or open = unipolar operation "0" or GND = bipolar operation
5	S1 } Channel 1 inputs. S4 for resolver use only.	22	S2		
6	S2	23	S3		
7	S3	24	S4	40	BITE output "1" = not tracking (fault) "0" = normal tracking
8	S4	25	Ref high } Channel 2 ref inputs		
9	Ref high } Channel 1	26	Ref low		
10	Ref low } ref input	27	Inhibit input "1" or open = track "0" or GND = hold (freeze)	41	.008° } For HSR-103 units only
11	Converter Busy output "1" = converter busy "0" = data stable			42	.004°	
				43	.002	
		28	.02°	44	.001	
12	.04°	29	.08°	45	20°
13	.01°	30	.1°	46	40°
14	.8°	31	.4°	47	80°
15	.2°	32	2°	48	10°
16	4°	33	8°	49	100°
17	1°	34	S-Ch1. For channel 1 synchro operation only, connect pin 34 to pin 35.	50	Unipolar: 200° Bipolar: "1" = minus sign
18	S-Ch 2. For channel 2 synchro operation only, connect pin 18 to pin 35.	35	SS Scott-T center tap		
19	Spare pin	36	Spare pin		

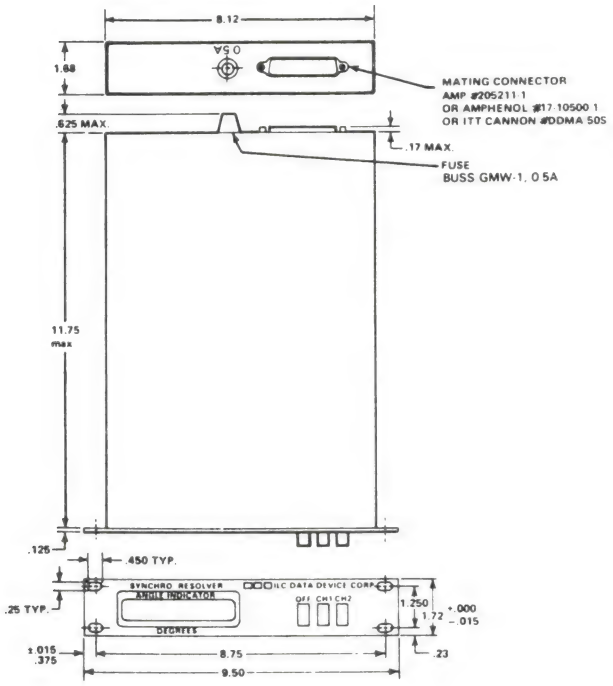
SR-103* AND HSR-103*

MECHANICAL OUTLINE FOR DBA-488 OPTION



The diagram on this page shows an SR-103 or HSR-103 instrument mounted together with a DBA-488 on a rack-mounting panel.

MECHANICAL OUTLINE FOR SR-103 AND HSR-103



ORDERING INFORMATION

All instruments are supplied with a mating connector and an instruction manual.

SR – 103 -3- DBA-488

- DBA-488: IEEE-488 Data Bus Adaptor:
  - Blank = SR-103 or HSR-103 only
  - DBA-488 = SR-103 or HSR-103 mounted together with a DBA-488 on a 3-1/2" high, 19" wide rack mounting panel, including cable connections
- -3-: Options:
  - Blank = SR-103
  - 3 = OPTION 3 (Center Rack Mount)
- SR – 103: Resolution and Accuracy:
  - SR = .01° resolution and ±.03° accuracy
  - HSR = .001° resolution and ±.005° accuracy

B

High Frequency Option (API-30702) Available (contact factory)

SYNCHRO AND RESOLVER ANGLE INDICATOR

DESCRIPTION AND APPLICATIONS

The SR-203 and HSR-203 are improved high quality angle indicators used in precision synchro and resolver test equipment. They accept synchro or resolver signals from a front panel input channel or either of two rear connector input channels. Output data, formatted to BCD angle information, is provided and displayed on the front panel. Both models are enclosed bench-type instruments, with a carry handle, which may be used as a tilt stand. Control functions, such as input channel select, input type, bandwidth, unipolar/bipolar, lamp test and inhibit, may be controlled either manually by front panel switches or remotely with control logic to the rear connector. A single switch multiplexes control between local and remote sources and front panel and rear connector input channels. An internal IEEE-488 data bus interface is available as an option. The SR-203 and HSR-203 instruments differ only in their accuracy and resolution. The SR-203 is accurate to ± 0.03°, while the HRS-203 is accurate to ±.005°. Resolution for the devices is ±0.01° and ±0.001° respectively (see Specifications). Because they can accept a broad range of voltages and frequencies, without programming, and signal to reference phase shifts of ± 50° (max), the SR-203 and HSR-203 are ideal for situations where a variety of inputs must be quickly accomodated. Using a type II servo loop for continuous tracking, these instruments have no velocity lag up to the specified tracking rates. There can be no hangup 180° away from the input angle. A fault indicator shows when the unit is not tracking the input signal, and an ambiguity indicator shows when the output data is changing. The SR-203 and HSR-203 require no adjustments or calibrations and logic is TTL compatible. The SR-203 and HSR-203, in addition to serving as high performance bench instruments, can be used wherever accurate angle information is required for display, control, testing purposes, or computation. Applications include production testing of synchros and resolvers, information translators in quality control systems, machine tool control, ship and aircraft navigation systems and antenna positioning. The IEEE-488 adapter option is convenient for interfacing these units with other instruments for automatic test equipment (ATE).

FEATURES

- *RESOLUTION TO .001°*
- *FRONT PANEL CONTROLS*
- *OPTIONAL IEEE-488 I/O*
- *FAULT INDICATOR*
- *PHASE SHIFT COMPENSATION*
- *BROADBAND (47-1000 Hz)*

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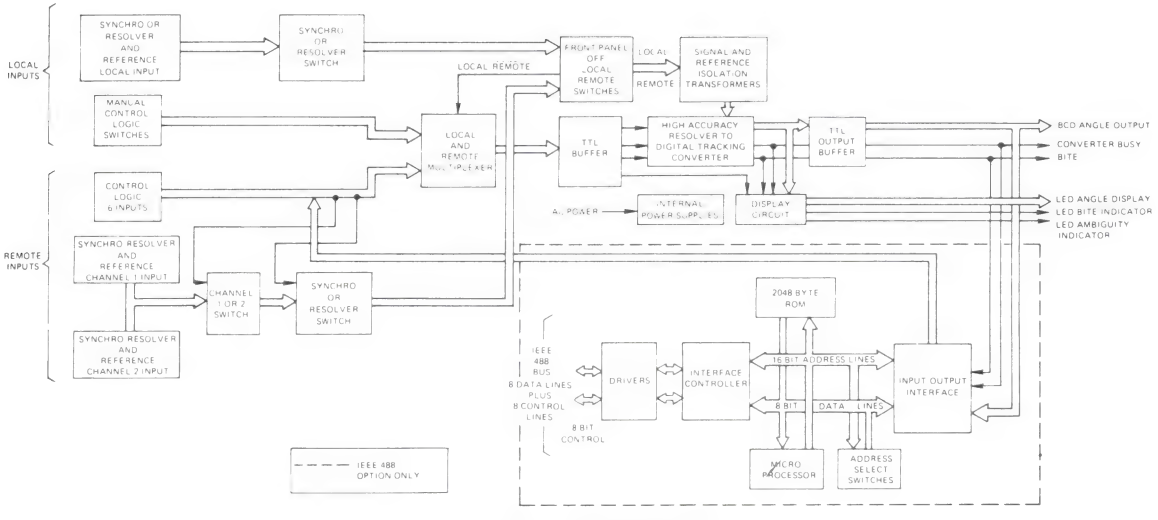


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

PARAMETER	UNITS	VALUE	
		SR-203	HSR-203
RESOLUTION	deg	0.01 (5 BCD digits)	0.001 (6 BCD digits)
ACCURACY (all causes)	deg	±0.03	±0.005
REPEATABILITY	deg	Within 0.01	Within 0.002
ANGLE RANGE (Continuous Rotation)			
Unipolar	deg	0 to +359.99	0 to +359.999
Bipolar	deg	0 to ±179.99	0 to ±179.999
DISPLAY			
7 Segment 0.43" LED		5 Digits	6 Digits
REFERENCE INPUT			
Input Type		Transformer isolation	
Voltage Level	V	10 to 150 rms	
Frequency	Hz	47 to 1000	
Input Impedance	Ω	100k min	
Breakdown Voltage	V	1000 min to logic ground	
Harmonic Content	%	±10 max	
SIGNAL INPUTS			
Input Type		Synchro or resolver, transformer isolated	
Line-to-Line Voltage	V	Auto-leveling, 10 to 100	
Frequency	Hz	Same as Reference	
Allowed Phase Shift	deg	±50 max, relative to reference	
Input Impedance			
SR-203	Ω	150k min at 47 Hz	
	Ω	250k min between 60 and 1000 Hz	
HSR-203	Ω	1M min	
Breakdown Voltage	V	1000 min to logic ground	
DYNAMIC CHARACTERISTICS		SR-203	HSR-203 TRACKING / SLEW
Tracking Rate (Full Accuracy)			
400 Hz	deg/sec	720	72 / 720 max
50 to 60 Hz	deg/sec	180	18 / 180 max
Settling Time (To Within 1 LSB)			
Lo Bandwidth (47 to 1000 Hz)	sec	1.7	2
Hi Bandwidth (360 to 1000 Hz)	sec	0.6	1.5
Open Loop Transfer Function			
$G = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{108}+1\right)^4}$			
Lo Bandwidth (47 to 1000 Hz)		A = 18, B = 10	A = 13, B = 10
Hi Bandwidth (360 to 1000 Hz)		A = 86, B = 46	A = 42, B = 21
DIGITAL INPUTS (TTL Compatible)			
Loading		0.5 std TTL loads max	
Inhibit (INH)		"1" or open = track "0" or GND = inhibits	
Bandwidth Selector (BW)		"1" or open = 47 to 1000 Hz (Lo Bandwidth) "0" or GND = 360 to 1000 Hz (Hi Bandwidth)	

PARAMETER	UNITS	VALUE
DIGITAL INPUTS (TTL Compatible)		
Loading		0.5 std TTL loads max
Inhibit (INH)		"1" or open = track "0" or GND = inhibits
Bandwidth Selector (BW)		"1" or open = 47 to 1000 Hz (Lo Bandwidth) "0" or GND = 360 to 1000 Hz (Hi Bandwidth)
Unipolar/Biopolar Selector (U/B)		"1" or open = unipolar operation (0° to 360°) "0" or GND = bipolar operation (−180° to +180°)
Lamp Test		"1" or open = normal operation "0" or GND = all LED segments on
Remote Channel Select		"1" or open = channel 2 "0" or GND = channel 1
Remote Synchro/Resolver Select		"1" or open = resolver "0" or GND = synchro
DIGITAL OUTPUTS (TTL Compatible)		
Drive Capability		4 std TTL loads, buffered output
Synchro or Resolver Angle		Parallel data bits, BCD angle, positive logic MSB becomes minus sign for bipolar operation SR203 has 5 decades, 18 lines; HSR203 has 6 decades, 22 lines
Converter Busy		4 μsec positive pulse, leading edge initiates conversion indicates tracking failure from any cause (including excessive speed or equipment malfunction) "1" = fault
FRONT PANEL FUNCTIONS		
Local/Remote Select		Select input panel from front panel or rear connector
On/Off		Main power control
Lamp Test		ALL LED segments on
Inhibit		Inhibits converter tracking
Synchro/Resolver Bandwidth		Synchro or Resolver select Select between HI and LO band widths (Controls applicable for local mode (front panel inputs) only)
Readout		Selects between unipolar and bipolar display and output
FRONT PANEL INPUTS TERMINALS		
Local Signal Inputs		
S1		Synchro/Resolver
S2		Synchro/Resolver
S3		Synchro/Resolver
S4		Resolver only
Local Reference Inputs		
RH		Reference HIGH
RL		Reference LOW
DIG GND and CASE		Digital and case ground respectively
POWER INPUT		
Voltage	Vrms	115/230; selectable via two internal switches (set for 115V unless otherwise specified).
Power	VA	20 max
Frequency	Hz	47 - 500
Isolation		Transformer
Breakdown Voltage (To Logic Gnd)	VDC	1000
TEMPERATURE RANGES		
Operating	°C	0 to +55
Storage	°C	−55 to +125
PHYSICAL CHARACTERISTICS		
Size	in	14.5 x 8.125 x 3.5 (368 x 201 x 89 mm)
Weight	lbs	11.0 (4.9 Kg)

REAR CONNECTOR

PIN CONNECTION TABLE

PIN	FUNCTION
1	Spare Pin
2	Spare Pin
3	Case GND
4	Digital GND (may be connected to case GND)
5	S1
6	S2 — Remote Channel 1 inputs
7	S3 — (S-4 for Resolver use only
8	S4
9	REF HI
10	REF — Channel 1 Ref input
11	Converter Busy Output 1 = Data Stable 0 = Converter Busy
12	.04°
13	.01°
14	.8°
15	.2°
16	4°
17	1°
18	Spare Pin
19	Lamp Test Input* 1 = Normal Operation 0 = Lamp Test (Remote Mode)
20	Channel 1/Channel 2 Inputs* 1 = Channel 2 0 = Channel 1

PIN	FUNCTION
21	S1
22	S2 — Channel 2 inputs
23	S3 — (S4 for Resolver use only)
24	S4
25	REF HI
26	REF LO — Channel 2 Ref Input
27	Inhibit Input* 1 = Track 0 = Inhibit
28	.02°
29	.08°
30	.1°
31	.4°
32	2°
33	8°
34	Reset Input (TTL logic) 1 = Normal Operation 0 = Reset — IEEE Interface
35	Unipolar/Bipolar Output 1 = Unipolar 0 = Bipolar — Remote Mode
36	Local/Remote Output 1 = Local Mode 0 = Remote Mode
37	Synchro/Resolver Input* 1 = Resolver 0 = Synchro — Remote Mode

PIN	FUNCTION
38	Unipolar/Bipolar Input* 1 = unipolar 0 = bipolar — Remote Mode
39	Bandwidth Input*
40	BITE Output 1 = Not Tracking (fault) 0 = Normal Tracking
41	.008°
42	.004°
43	.002°
44	.001°
45	20°
46	40°
47	80°
48	10°
49	100°
50	Unipolar = 200° Bipolar = 1 = minus sign (-)

* The User must supply digital input signals for standard (Non-I-EEE-488) units. For units including the IEEE-488 interface option, these pins *must not* have external connections.

TECHNICAL INFORMATION

Both SR-203 and HSR-203 instruments are available with an IEEE-488 Data Bus Interface circuit built in (see Figure 1). This option must be specified when the instruments are ordered. Add "-488" to the part number as shown in ORDERING INFORMATION.

The IEEE-488 option provides the capability to process signals received from or transmitted to a parallel data bus as described in the IEEE-488 Data Bus Standard of 1975. When programmed to operate with the "488" Data Bus Controller, the SR/HSR-203-488 will perform the command sequences shown in Figures 2 and 3.

In the talk routine (Figure 2), the instrument transmits a sign byte (+, – or E for error) followed by 5 (for SR-203) or 6 (HSR-203) BCD ASCII data bytes, followed by CR (carriage return), followed by LF (line feed), with EOI (End or Identify), when interrogated by the controller.

Figure 4 indicates the possible ASCII control words that would be transmitted from a controller to the instrument as shown in the listen routine (Figure 3).

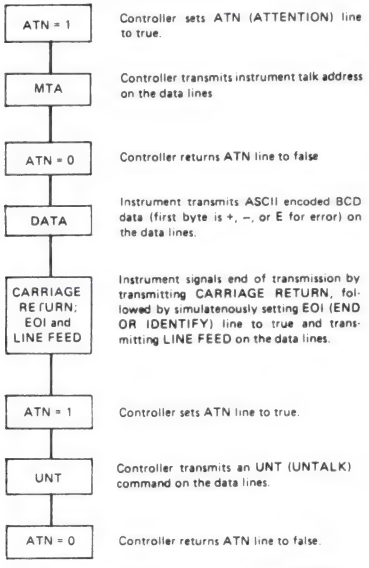

ATN = 1
Controller sets ATN (ATTENTION) line to true.
MTA
Controller transmits instrument talk address on the data lines
ATN = 0
Controller returns ATN line to false
DATA
Instrument transmits ASCII encoded BCD data (first byte is +, –, or E for error) on the data lines.
CARRIAGE RETURN; EOI and LINE FEED
Instrument signals end of transmission by transmitting CARRIAGE RETURN, followed by simultaneously setting EOI (END OR IDENTIFY) line to true and transmitting LINE FEED on the data lines.
ATN = 1
Controller sets ATN line to true.
UNT
Controller transmits an UNT (UNTALK) command on the data lines.
ATN = 0
Controller returns ATN line to false.

FIGURE 2. COMMAND SEQUENCE FOR TALKING

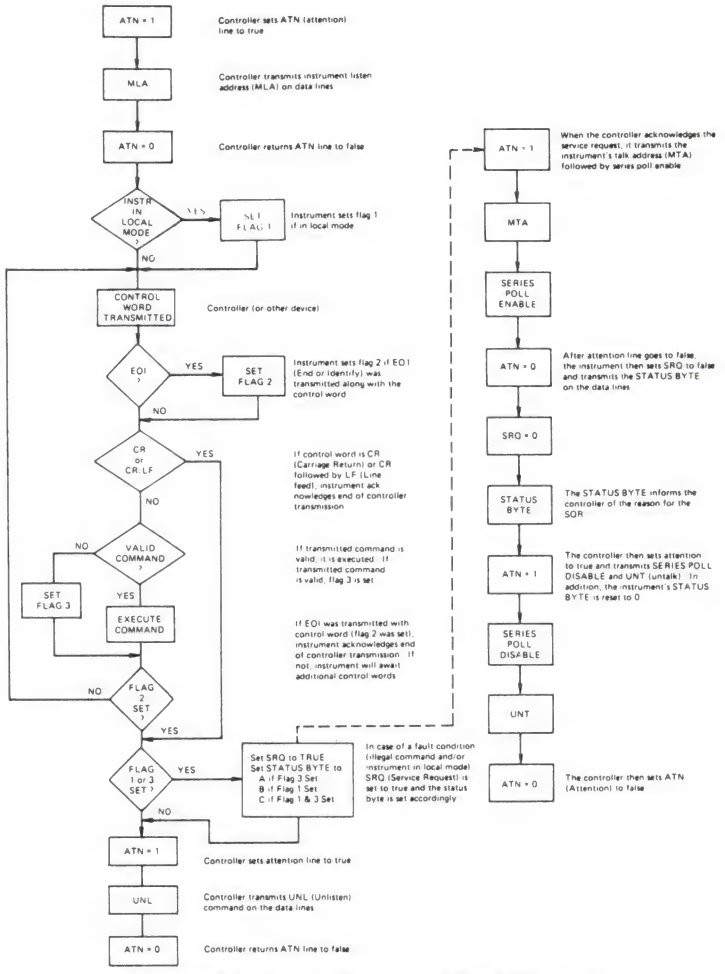

ATN = 1
Controller sets ATN (attention) line to true
MLA
Controller transmits instrument listen address (MLA) on data lines
ATN = 0
Controller returns ATN line to false
INSTR IN LOCAL MODE ?
YES
NO
SET FLAG 1
Instrument sets flag 1 if in local mode
CONTROL WORD TRANSMITTED
Controller (or other device)
EOI ?
YES
NO
SET FLAG 2
Instrument sets flag 2 if EOI (End or Identify) was transmitted along with the control word
CR or CR-LF
YES
NO
If control word is CR (Carriage Return) or CR followed by LF (Line feed), instrument acknowledges end of controller transmission
VALID COMMAND ?
NO
YES
SET FLAG 3
If transmitted command is valid, it is executed. If transmitted command is valid, flag 3 is set
EXECUTE COMMAND
If EOI was transmitted with control word (flag 2 was set), instrument acknowledges end of controller transmission. If not, instrument will await additional control words
FLAG 2 SET ?
NO
YES
FLAG 1 or 3 SET ?
YES
NO
Set SRQ to TRUE
Set STATUS BYTE to
A: if Flag 3 Set
B: if Flag 1 Set
C: if Flag 1 & 3 Set
In case of a fault condition (illegal command and/or instrument in local mode) SRQ (Service Request) is set to true and the status byte is set accordingly
ATN = 1
Controller sets attention line to true
UNL
Controller transmits UNL (Unlisten) command on the data lines
ATN = 0
Controller returns ATN line to false
ATN = 1
When the controller acknowledges the service request, it transmits the instrument's talk address (MTA) followed by series poll enable
MTA
SERIES POLL ENABLE
ATN = 0
After attention line goes to false, the instrument then sets SRQ to false and transmits the STATUS BYTE on the data lines
SRQ = 0
STATUS BYTE
The STATUS BYTE informs the controller of the reason for the SQR
ATN = 1
The controller then sets attention to true and transmits SERIES POLL DISABLE and UNT (untalk). In addition, the instrument's STATUS BYTE is reset to 0
SERIES POLL DISABLE
UNT
ATN = 0
The controller then sets ATN (Attention) to false

FIGURE 3. COMMAND SEQUENCE FOR LISTENING

COMMAND FUNCTIONS FOR IEEE-488 OPTION

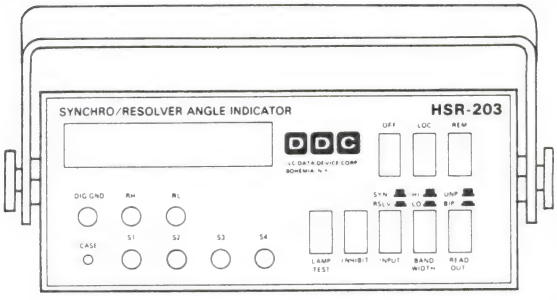
NOTE: 1. IEEE-488 Interface will accept all input commands, regardless of input mode selected (local or remote). When the instrument is switched to Remote mode, the last commands received will take effect.

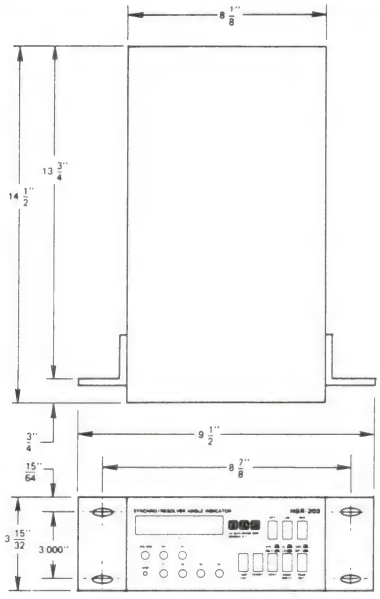
2. The SR–203 is controlled exclusively by front panel switching when local mode is selected. Lamp test switch will illuminate all LED segments regardless of input mode.

CONTROL WORD (ASCII)	FUNCTION
P (Preset)	Preset to: Channel 1, Synchro input, No inhibit, No lamp test, High bandwidth, Unipolar Output
S (Synchro) R (Resolver)	Sets Synchro or Resolver input mode
1 (Channel 1) 2 (Channel 2)	Selects between remote Input channels 1 and 2 on rear connector
H (High) L (Low)	Select high or low bandwidth
U (Unipolar) B (Bipolar)	Selects unipolar or bipolar readout and output
I (Inhibit) F (Follow)	Inhibits the converter or allows it to follow (track) the input
T (Test) D (Data)	Tests lamps (T) or display data (D)

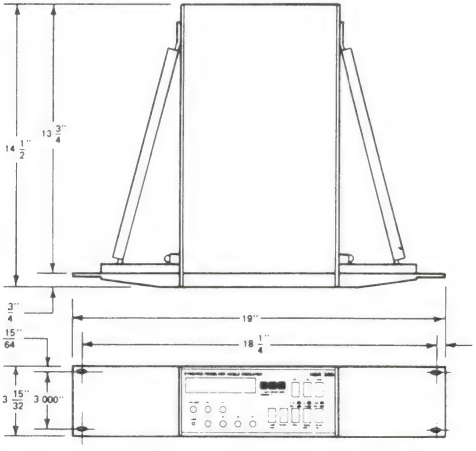
FIGURE 4. CONTROL CODE FUNCTIONS

G



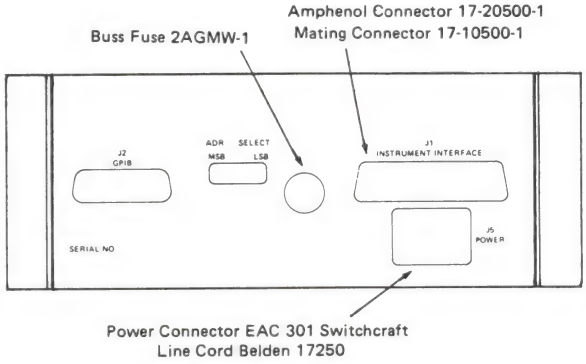


OPTION 2 Half Rack Mount



OPTION 3 Center Mount 19" Panel

POWER CONNECTOR EAC 301 SWITCHCRAFT



ORDERING INFORMATION

SR – 203 – 1 – DBA-488

- IEEE-488 Option:
  - 488 = Built-in IEEE-488 Interface
- Configuration Options:
  - Blank = SR-203
  - 1 = Standard option 1 carryhandle
  - 2 = Option 2 half-rack mount
  - 3 = Option 3 center mount on 19" panel
- Accuracy (worst case, all causes)
  - SR = ± 0.03°
  - HSR = ± 0.005°

High Frequency Option (API-30702) Available (contact factory)

All instruments are supplied with a mating connector, a detachable line cord and instruction manual.

D

SECTION H
SYNCHRO AND RESOLVER CARDS

PRODUCT SUMMARY TABLE

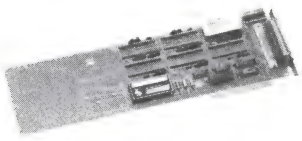
	MODEL	RESOLUTION	ACCURACY	PACKAGE	DESCRIPTION/FEATURES	PAGE
*	API-36005	SEE SYNCHRO AND RESOLVER INSTRUMENTS FOR THE API-36005.				G-6
*	DSC-36020	—	—	Full Size IBM PC ® Card	1 TO 6 CHANNEL D/S-R CONVERTER CARD. Uses either the DSC-11520 (low power)or DSC-11524 (higher drive). All binary angular information needed to control the D/S-R converters is presented to the SDC-36020 through memory mapped I/O space. Two bytes of angular information (16 bits) are required for each converter for a total of 12 bytes of data if all 6 channels of converters are installed on the DSC-36020. Has demo software.	H-2
*	DSC-36022	—	—	Full Size IBM PC ® Card	1 TO 6 CHANNEL D/S-R CONVERTER CARD. Uses either the DSC-644 or DSC-544 series of high-power modular converters. Similar, in operation, as the DSC-36020. Has demo software.	H-8
*	IAC-37001	SEE SYNCHRO AND RESOLVER INSTRUMENTS FOR THE IAC-37001.				G-12
	SDC-36015	10,12,14, or 16 Bits	± 3'	4.5 x 13.5 x 0.44"	R/D-S/D CONVERTER CARD. Full size IBM card for 1 to 6 channel of Resolver or Synchro to Digital conversion. It uses either the RDC-19200 Series (for resolver inputs) or SDC-14560 (for synchro inputs) hybrid converters.	H-14
*	SIM-36010	SEE SYNCHRO AND RESOLVER INSTRUMENTS FOR THE SIM-36010.				G-28

H

NOTES: Most hybrid products are available with Military Processing (Contact Factory).
® IBM PC is a registered trademark of International Business Machines.
* New Product

DDC
ILC DATA DEVICE CORPORATION

DSC-36020



IBM PC® COMPATIBLE 6 CHANNEL D/R-D/S CONVERTER CARD

DESCRIPTION

The DSC-36020 is a versatile, full size IBM PC card designed for 1 to 6 channels of Digital-to-Synchro/Resolver conversion. The DSC-36020 uses either the DSC-11520 series hybrid converters for low power applications or the DSC-11524 series converters if higher drive capability is required.

Specific information concerning the hybrid converters can be obtained directly from the associated converter's data sheet. The DSC-36020 circuit card assembly is the interface to mount (plug-in) the hybrid converter components.

All binary angular information needed to control the Digital-to-Synchro/Resolver converters is presented to the DSC-36020 through switch selectable I/O address space. Two bytes of angular information (16 bits) are required for each converter for a total of 12 bytes of data if all 6 channels of converters are installed on the DSC-36020. Demonstration software displaying the capabilities of the DSC-36020 is available upon request.

APPLICATIONS

The multichannel DSC-36020 is designed for use in test systems, high-performance simulation systems, and control systems. With the various hybrid converter selections available for drive and accuracy a mixture of converters can be used to accommodate many applications including motor control, antenna positioning, CNC machine tooling, robot axis control, and process control.

FEATURES

- ***1 to 6 Channels***
- ***Generates Synchro or Resolver Output Signals***
- ***No External Power Supply Required***
- ***Accuracy to ±1 Minute of Arc***

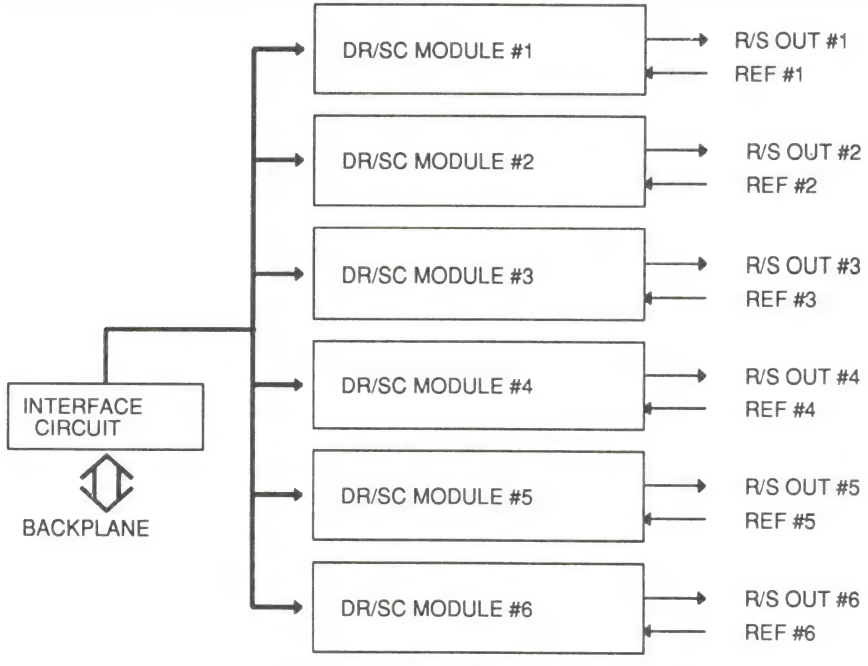


FIGURE 1. DSC-36020 BLOCK DIAGRAM

TABLE 1. DSC-36020 SPECIFICATIONS		
HARDWARE REQUIREMENTS		
IBM PC/XT/AT or compatible.		
PARAMETER	**UNITS**	**VALUE**
POWER SUPPLY (+5V)		
Current Drain		
■ Without Any Hybrids	mA	285 max
■ With One (1) DSC-11520 Hybrid	mA	430 max
■ With Six (6) DSC-11520 Hybrids	mA	1150 max
■ With One (1) DSC-11524 Hybrid	mA	540 max
■ With Six (6) DSC-11524 Hybrids	mA	1800 max
TEMPERATURE RANGE		
Operating	°C	0 to +50
Storage	°C	-25 to +85
PHYSICAL CHARACTERISTICS		
Size (Full size IBM PC card)	in	3.9 x 13.3 x 0.44
	(cm)	(9.9 x 33.8 x 1.1)
Note: Specifications for the DSC-11520 and DSC-11524 Series are detailed in the individual data sheets.		

TECHNICAL INFORMATION

INTRODUCTION

The DSC-36020 is a full size IBM PC card which generates up to six channels of sine/cosine, synchro, or resolver signals. The output signal configuration is jumper programmable and can be set for sine/cosine information, three wire synchro information, or 4 wire resolver information.

The Digital Angular information is presented to each converter on the DSC-36020 in 2 bytes (Most Significant Byte and Least Significant Byte) of binary information. This data is then transparently latched into the Hybrid converters through double buffered latches thereby presenting the 16 bits of angular data to the selected converter simultaneously. Figure 1 illustrates the DSC-36020 Block Diagram.

CONVERTER INFORMATION

Two types of converters can be used. The DSC-11520 are low power types that can drive 11.8V synchro or 6.8V resolver loads up to 2 mA. For higher drive applications, the DSC-11524 series can be used. These will drive 11.8V synchro or resolver loads up to 15 mA. For more detailed converter information consult the individual product data sheets. The DSC-36020 is supplied without the converter(s). The converter(s) are ordered separately and are easily installed into sockets on the DSC-36020.

REGISTER ADDRESSING

The DSC-36020 is I/O addressed in typical I/O Base Address and Offset fashion. As the DSC-36020 can accommodate six channels of hybrid converters, the memory map for the DSC-36020 appears as 12 contiguous bytes of I/O address space.

Decoding these 12 bytes requires using 4 LSBs of the I/O address. The remaining six address lines are used for setting the I/O Base Address through a DIP switch located on the DSC-36020. The I/O Base Address of the DSC-36020 is preset at the factory to address 300h (HEX). In this configuration the DSC-36020 occupies the I/O address space of 300h-30Bh. Locations 30Ch-30Fh will select the DSC-36020, however no registers are provided at these locations. Table 2 lists the DSC-36020's I/O Offset Address Map.

TABLE 2. DSC-36020 I/O OFFSET ADDRESS MAP				
A3	**A2**	**A1**	**A0**	**I/O Write**
0	0	0	0	8 LSBs of Channel 1
0	0	0	1	8 MSBs of Channel 1
0	0	1	0	8 LSBs of Channel 2
0	0	1	1	8 MSBs of Channel 2
0	1	0	0	8 LSBs of Channel 3
0	1	0	1	8 MSBs of Channel 3
0	1	1	0	8 LSBs of Channel 4
0	1	1	1	8 MSBs of Channel 4
1	0	0	0	8 LSBs of Channel 5
1	0	0	1	8 MSBs of Channel 5
1	0	1	0	8 LSBs of Channel 6
1	0	1	1	8 MSBs of Channel 6
1	1	0	0	Not Used
1	1	0	1	Not Used
1	1	1	0	Not Used
1	1	1	1	Not Used

I/O BASE ADDRESS DIP SWITCH

The I/O Base Address of the DSC-36020 is preset at the factory to 300h as shown in Table 3. There are no Readable registers located on the DSC-36020 so any I/O Read operation performed on the DSC-36020 will most likely return FFh. The I/O Base Address can be changed to any address from 000h to 3F0h, in increments of 10h, using Table 3 as a reference.

TABLE 3. I/O BASE ADDRESS SETTINGS				
ADDRESS	SWITCH	OFF (OPEN)	ON	PRESET HEX VALUE
A9	SW5	X		3
A8	SW6	X		
A7	SW7		X	0
A6	SW8		X	
A5	SW9		X	
A4	SW10		X	
A3	-	-	-	A0, A1, A2, and A3 are not switch selectable
A2	-	-	-	
A1	-	-	-	
A0		-	-	

BINARY ANGULAR DATA

The Most Significant Bit of the Most Significant Byte represents the Binary Angular value of 180°. The second Most Significant Bit of the same Byte represents the angular value of 90°, and the third represents 45° etc, down to the Least Significant Bit of this Byte which represents 1.406° (rounded to 3 decimal places).

The Most Significant Bit of the Least Significant Byte represents 0.703° (rounded to 3 decimal places) and following suit the Least Significant Bit has the weight of 0.005° (rounded to 3 decimal places).

Algorithms to convert Decimal angular data into Binary angular data consist of testing the magnitude of the Decimal value against the Binary values to see which Binary values can be added together in order to come closest to the Decimal value. This test generally starts with the most significant Binary bit weight of 180° and determines if it is more or less than the Decimal value. If the Decimal is larger than 180° then obviously this Binary bit is part of the final Binary value, if the Decimal value is less than 180° then this Bit is not part of the final Binary value. This same test is now performed using the second Binary Bit (90°) and so on down to the LSB of 0.005°.

For example to convert 135.703° to a Binary value, the following steps are taken:

- 1. The Most Significant Binary bit is 180° and is obviously too large to be contained in the final Binary value so it is set to logic 0.
- 2. The Second Binary Bit has the value of 90° which is smaller than the Decimal value of 135.703°. It is obviously part of the final Binary value so it is set to logic 1 and 90° is subtracted from the Decimal value leaving 45.703°.
- 3. The Third Binary bit has the value of 45° which again is smaller than the Decimal remainder of 45.703. It obviously is part of the final Binary value so it is set to logic 1 and 45° is subtracted from the Decimal remainder leaving 0.703°.
- 4. The Forth Binary Bit has a value of 22.5° which is too big to fit. It is set of logic 0 and the testing continues using the Decimal value of 0.703. So far we have tested the 4 MSBs of the Binary values and the Binary solution at this point is "0 1 1 0" with 12 more Binary Bits to test.
- 5. The 5th, 6th, 7th, and 8th Binary bits are all too large and are therefore set to logic 0. The Binary value at this point is "0 1 1 0 0 0 0 0" with 8 more Binary Bits to test.
- 6. The Binary Bit weight of the 9th bit is 0.703° and it fits exactly into the Decimal value of 0.703. The Binary Bit is therefore set to logic 1 and the Binary answer at this point is "0 1 1 0 0 0 0 0 1". The Binary value of 0.703 is subtracted from the Decimal Value and the remainder is 0.
- 7. As the Decimal remainder is now 0 obviously none of the remaining Binary Bits will Fit into the Decimal value so they can all be set to logic 0. The final Binary answer is therefore "0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0"
- 8. The Most Significant Byte of the Binary angle contains the value "0 1 1 0 0 0 0 0" and the Least Significant Byte contains the Binary value "1 0 0 0 0 0 0 0".

IMPORTANT - When the Binary Angular Data is loaded into any channel of the DSC-36020 it **MUST** be loaded into the registers Least Significant Byte first followed by the Most Significant Byte. If this sequence is not followed the double buffering circuitry for the associated converter will not function properly and the generated angle will be incorrect (the new MSB data will be used with the previous LSB data, and the new LSB data will be put into temporary storage to be used for the next update).

CONFIGURATION JUMPERS

Each hybrid converter has 3 jumper strips associated with it which are identified as A, B, and C. A and B jumper strips are used to set the output signal format; C jumper strip is used for the reference input circuitry. As the DSC-36020 assembly is shipped from the factory these jumpers are preset to accept a 26V ac reference signal, and to generate 11.8 V_{L-L} synchro output format.

REFERENCE CONFIGURATION JUMPERS

As the DSC-36020 leaves the factory the initial reference jumpers are preset to accept a 26V ac reference signal. If a reference signal other than 26V ac is to be used for any channel the initial jumper settings may have to be changed. In addition external resistors may have to be added to reduce the voltage level applied to the hybrid converter. If this feature is to be utilized the detailed data sheet for the associated hybrid converter should be consulted to ascertain the required configuration.

Jumper block C is initially configured with jumpers from 1-2 and 4-5. In this configuration the RH and RL signals on the I/O connector are connected to the RH and RL pins on the hybrid converter (refer to the detailed hybrid converter data sheet). If the RH' and RL' Reference inputs on the hybrid converter are to be utilized these jumpers will have to be moved to jumper 2-3 and 5-6. External resistors may also be required in this configuration (refer to the detailed hybrid converter data sheet).

OUTPUT SIGNAL CONFIGURATION JUMPERS

Each channel can be separately configured to provide sine/cosine, synchro, or resolver output signal format. As the DSC-36020 leaves the factory the output signal jumper configuration is preset for 11.8 V_{L-L} synchro output format through the associated Jumper blocks A and B. Table 4 lists the jumper settings for all of the various output formats.

TABLE 4. OUTPUT FORMAT JUMPER SETTINGS

OUTPUT FORMAT	BLOCK A	BLOCK B
11.8 V_{L-L} Synchro (default)	1-2	1-2 and 4-5
11.8 V_{L-L} Resolver *	2-3	4-5
6.8V Sine/Cosine	1-2	5-6

* The DSC-11520 Series does not support this mode.

COMPUTER INTERFACE CONNECTOR

The DSC-36020 conforms to standard PC BUS specifications. The pin number and function of the computer interface signals are listed in Table 5.

TABLE 5. DSC-36020 COMPUTER INTERFACE PIN FUNCTIONS

PIN NO.	SIGNAL NAME	FUNCTION
A1	$\overline{\text{I/O CHECK}}$	NOT USED
A2	D7	DATA BIT 7
A3	D6	DATA BIT 6
A4	D5	DATA BIT 5
A5	D4	DATA BIT 4
A6	D3	DATA BIT 3
A7	D2	DATA BIT 2
A8	D1	DATA BIT 1
A9	D0	DATA BIT 0
A10	I/O READY	NOT USED
A11	AEN	ADDRESS ENABLE
A12	A19	NOT USED
A13	A18	NOT USED
A14	A17	NOT USED
A15	A16	NOT USED
A16	A15	NOT USED
A17	A14	NOT USED
A18	A13	NOT USED
A19	A12	NOT USED
A20	A11	NOT USED
A21	A10	NOT USED
A22	A9	ADDRESS BIT 9
A23	A8	ADDRESS BIT 8
A24	A7	ADDRESS BIT 7
A25	A6	ADDRESS BIT 6
A26	A5	ADDRESS BIT 5
A27	A4	ADDRESS BIT 4
A28	A3	ADDRESS BIT 3
A29	A2	ADDRESS BIT 2
A30	A1	ADDRESS BIT 1
A31	A0	ADDRESS BIT 0
B1	GROUND	GROUND
B2	RESET	NOT USED
B3	+5V	POWER SUPPLY
B4	IRQ2	NOT USED
B5	-5V	NOT USED
B6	DRQ2	NOT USED
B7	-12V	NOT USED
B8	$\overline{\text{0WS}}$	NOT USED
B9	+12V	NOT USED
B10	GROUND	GROUND
B11	$\overline{\text{MEMW}}$	NOT USED
B12	$\overline{\text{MEMR}}$	NOT USED
B13	$\overline{\text{IOW}}$	I/O WRITE
B14	$\overline{\text{IOR}}$	I/O READ
B15	$\overline{\text{DACK3}}$	NOT USED
B16	DRQ3	NOT USED
B17	$\overline{\text{DACK1}}$	NOT USED
B18	DRQ1	NOT USED
B19	$\overline{\text{DACK0}}$	NOT USED
B20	CLOCK	NOT USED
B21	IRQ7	NOT USED
B22	IRQ6	NOT USED
B23	IRQ5	NOT USED
B24	IRQ4	NOT USED
B25	IRQ3	NOT USED
B26	$\overline{\text{DACK2}}$	NOT USED
B27	T/C	NOT USED
B28	ALE	NOT USED
B29	+5V	POWER SUPPLY
B30	OSC	NOT USED
B31	GROUND	GROUND

H

SIGNAL I/O CONNECTOR

The converter I/O signals are brought off the DSC-36020 through a 37 pin D type connector with male pins. The signal connections are listed in Table 6.

TABLE 6. I/O CONNECTOR PIN FUNCTIONS

	CHANNELS					
SIGNAL*	1 (U1)	2 (U2)	3 (U3)	4 (U4)	5 (U5)	6 (U6)
S1	19	16	13	10	7	4
S2 (COS)	37	34	31	28	25	22
S3 (SIN)	18	15	12	9	6	3
S4 (COM)	36	33	30	27	24	21
RH	17	14	11	8	5	2
RL	35	32	29	26	23	20

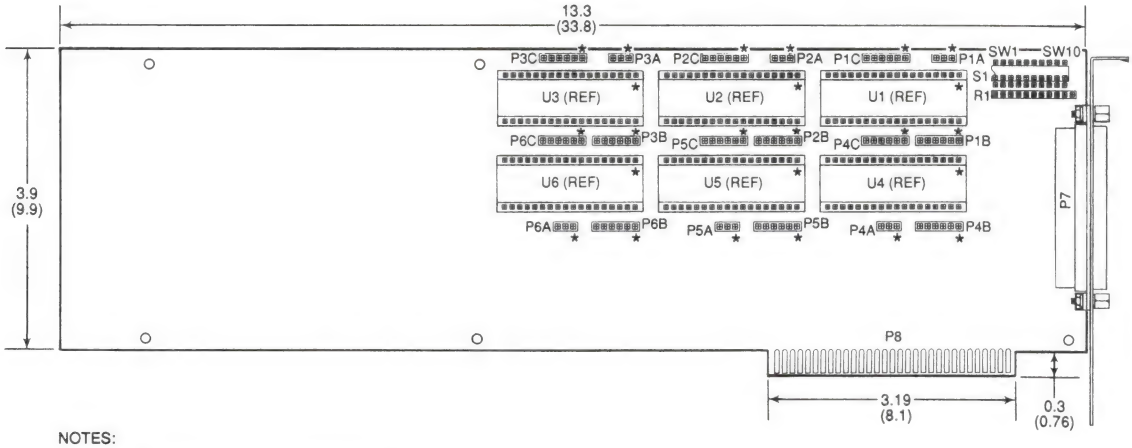
*Note: In addition to these signals, the circuit ground connection is brought out on pin 1.

TIMING REQUIREMENTS

Data to the DSC-36020 is sent by the computer using standard I/O Write cycles (there are no readable registers). All of the interface logic utilizes high-speed components allowing the DSC-36020 to be addressable in zero wait state time cycles, however the following precautions must be taken.

If a step input is given to a converter, allow at least 20 µs for the output signals to stabilize.

The binary data value for the output angle must be loaded Least Significant Byte first (the 8 LSBs of the angle) followed by the Most Significant Byte (the 8 MSBs of the angle), or the double buffering scheme will not function properly causing and incorrect angle to be generated.



NOTES:

THE "*" DESIGNATED PIN 1 LOCATION.
DIMENSIONS ARE IN INCHES (CENTIMETERS).

FIGURE 2. DSC-36020 MECHANICAL OUTLINE

ORDERING INFORMATION

CARD ASSEMBLY:

DSC-36020

CONVERTERS:

DSC-11520

DSC-11524

Notes:

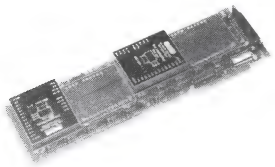
1. The DSC-36020 is a standard, full-size IBM PC/XT/AT card (3.9 x 13.3 x 0.44 inches).
2. Converters are ordered separately as listed above and installed by the user. Sockets are included on the DSC-36020.
3. Mating connectors are supplied with the DSC-36020. The connectors are part of Positronic's MD 37F 20Y00 kit.

   Positronic's address is 423 N. Cambell Ave., Springfield, Missouri 65801

DDC
ILC DATA DEVICE CORPORATION

DSC-36022

IBM PC® COMPATIBLE 4 CHANNEL D/R-D/S CONVERTER CARD



DESCRIPTION

The DSC-36022 is a versatile, full size IBM PC® card designed to provide one to four channels of Digital-to-Synchro/Resolver conversion. The card is equiped with sockets and can accomodate either the DSC-544 or DSC-644 Series converter modules (or both) in any socket position. The DSC-544 Series can provide up to 4.5 VA of 90V synchro output, and the DSC-644 can provide 1.5VA of synchro or resolver, 90V or 11.8V.

The DSC-36022 circuit card assembly provides the interface to mount(plug-in) the modules.

All binary angular information needed to control the Digital-to-Synchro/Resolver converter is presented to the DSC-36022 card through switch selectable I/O address space.

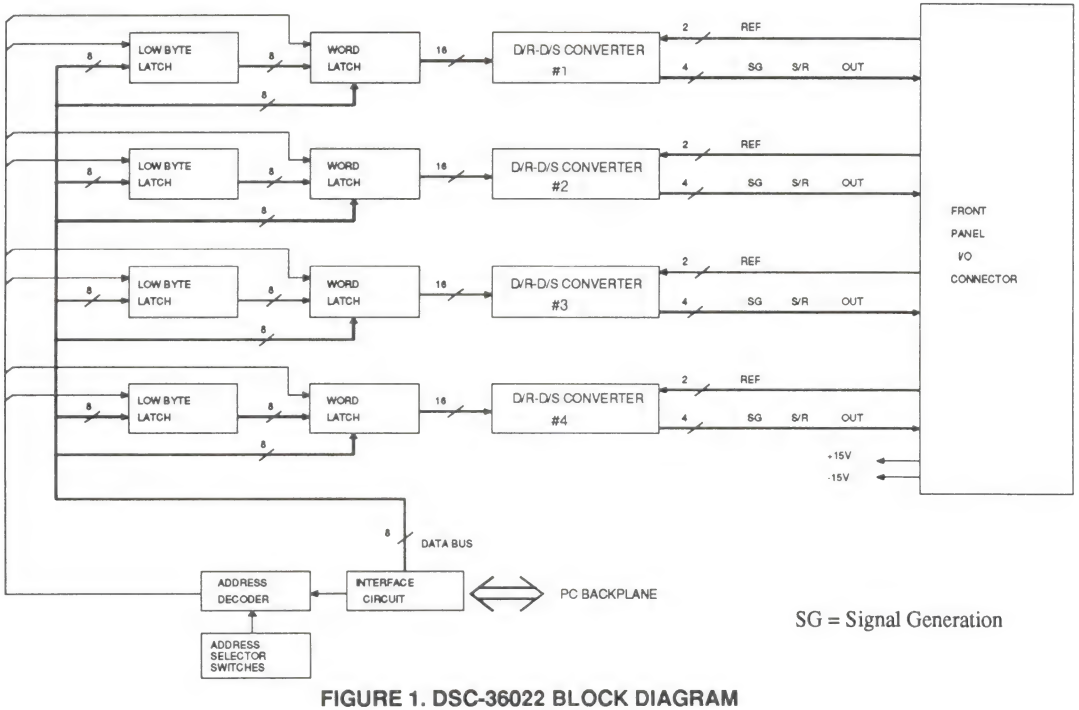
Demonstration software which illustrates the DSC-36022's capabilities, is available upon request.

APPLICATIONS

The multichannel DSC-36022 is designed for use in test systems, high-performance simulation systems, and control systems. With the two types of drive capability available, a mix of converters can be utilized to accommodate many applications including antenna positioning, process control, automated test systems, and simulation systems.

FEATURES

- ***Accuracy to ±4 Minutes of Arc***
- ***±0.1% Scale Factor Variation***
- ***Generates Synchro or Resolver Output Signals***
- ***1 to 4 Channels of Converters per Card***
- ***1.5 VA or 4.5 VA Output Drive Capability***
- ***Transparent Double Buffered Latches for Data Input***



SG = Signal Generation

FIGURE 1. DSC-36022 BLOCK DIAGRAM

TABLE 1. DSC-36022 SPECIFICATIONS		
HARDWARE REQUIREMENTS		
IBM PC/XT/AT or compatible.		
PARAMETER	**UNITS**	**VALUE**
POWER SUPPLY (+5V)		
Current Drain		
■ Without Any Converters	mA	350 max
■ With One (1) DSC-544 Module	mA	370 max
■ With Four (4) DSC-544 Modules	mA	430 max
■ With One (1) DSC-644 Module	mA	355 max
■ With Four (4) DSC-644 Modules	mA	370 max
TEMPERATURE RANGE		
Operating	°C	0 to +50
Storage	°C	-25 to +85
PHYSICAL CHARACTERISTICS		
Size (Full size IBM PC card)	in (cm)	3.9 x 13.3 x [note 2] (9.9 x 33.8 x [note 2])

Notes:
1. Specifications for the DSC-544 and DSC-644 Series are detailed in the individual data sheets. The user must supply reference voltage. The DSC-644 also requires ±15Vdc.
2. Component height:
   with DSC-644 modules installed, 0.565"(14.4mm) max;
   with DSC-544 modules installed, 0.865"(22mm) max.
3. Cut modules leads to 0.195"(4.95mm)

TECHNICAL INFORMATION

INTRODUCTION

The DSC-36022 is a full size IBM PC card which generates up to four channels of Synchro or Resolver output signals. For applications requiring up to 1.5 VA of drive capability the DSC-644 Series of converter modules can be used. They are available with $90V_{L\text{-}L}$ Synchro and $11.8V_{L\text{-}L}$ Synchro or Resolver outputs (for operation down to 47 Hz, a transformer external to the DSC-36022 is required). These modules require external ±15Vdc power supplies which are connected to the DSC-36022 by a 37 pin I/O connector.

For higher drive, $90V_{L\text{-}L}$ 400 Hz Synchro applications, the DSC-544 can be used. The DSC-544 can supply up to 4.5 VA of drive; a $90V_{L\text{-}L}$ 60 Hz version can supply up to 1.5 VA of drive. Both models of the DSC-544 are powered by the Reference input signal. Both the DSC-644 and DSC-544 family of converter modules provide complete transformer isolation for the Reference input and the Synchro/Resolver output signals.

The Digital Angular information is presented to each converter on the DSC-36022 card in two bytes (Most Significant Byte and Least Significant Byte) of binary information. This data is transparently latched into the converters through double buffered latches thereby presenting the 14 bits of angular data to the selected converter simultaneously.

Two bytes of angular information are required for each converter for a total of 8 bytes of data if all 4 channels of converters are installed on the DSC-36022. Figure 1 illustrates the DSC-36022 Block Diagram.

REGISTER ADDRESSING

The DSC-36022 is I/O addressed in a typical I/O Base Address and Offset manner. As the DSC-36022 can accommodate up to four channels of converter modules, its memory map appears as 8 contiguous bytes of I/O address space.

Decoding these 8 bytes (plus a few spare bytes for expansion) requires the use of the 4 LSBs of the I/O address. The next 6 address lines are used for setting the I/O Base Address through a DIP switch located on the DSC-36022.

The I/O Base Address of the DSC-36022 is preset at the factory to HEX address 300. In this configuration the DSC-36022 will occupy the I/O address space of 300h through 307h. The I/O Base Address can be set to any address from 000h to 3F0h in increments of 10h (described in I/O BASE ADDRESS DIP SWITCH paragraph). There are no Readable registers located on the DSC-36022 so any I/O Read operation performed on the card will most likely return FFh. Table 2 lists the I/O Offset Address Map of the DSC-36022.

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TABLE 2. DSC-36022 I/O OFFSET ADDRESS MAP				
A3	**A2**	**A1**	**A0**	**I/O Write**
0	0	0	0	6 LSBs of Channel 1*
0	0	0	1	8 MSBs of Channel 1
0	0	1	0	6 LSBs of Channel 2*
0	0	1	1	8 MSBs of Channel 2
0	1	0	0	6 LSBs of Channel 3*
0	1	0	1	8 MSBs of Channel 3
0	1	1	0	6 LSBs of Channel 4*
0	1	1	1	8 MSBs of Channel 4
1	0	0	0	Not Used
1	0	0	1	Not Used
1	0	1	0	Not Used
1	0	1	1	Not Used
1	1	0	0	Not Used
1	1	0	1	Not Used
1	1	1	0	Not Used
1	1	1	1	Not Used

*The Digital to Synchro/Resolver converters used on the DSC-36022 are 14 bit converters. The two least significant bits of each Least Significant Byte are not used.

I/O BASE ADDRESS DIP SWITCH

The I/O Base Address of the DSC-36022 is preset at the factory to HEX 300. The I/O Base Address can be changed to any address from 000h to 3F0h in increments of 10h using Table 3 as a reference.

TABLE 3. I/O BASE ADDRESS SETTINGS

ADDRESS	SWITCH	OFF (OPEN)	ON	PRESET HEX VALUE
A9	SW6	X		3
A8	SW5	X		
A7	SW4		X	0
A6	SW3		X	
A5	SW2		X	
A4	SW1		X	
A3	-	-	-	A0-A3 are not switch selectable.
A2	-	-	-	
A1	-	-	-	
A0	-	-	-	

BINARY ANGULAR DATA

The Most Significant Bit of the Most Significant Byte represents the Binary Angular value of 180°. The second Most Significant Bit of the same byte represents the angular value of 90°, and the third represents 45° etc., down to the Least Significant Bit of this byte which represents 1.406° (rounded to 3 decimal places).

The Most Significant Bit of the Least Significant Byte represents 0.703° (rounded to 3 decimal places); following suit the Least Significant Bit, if using a 16 bit converter, would have the weight of 0.005° (rounded to 3 decimal places).

Algorithms to convert Decimal angular data into Binary angular data consist of testing the magnitude of the Decimal value against the Binary values to see which Binary values can be added together in order to come closest to the Decimal value. This test generally starts with the most significant Binary bit weight of 180° and determines if it is more or less than the Decimal value. If the Decimal is larger than 180° then obviously this Binary bit is part of the final Binary value, if the Decimal value is less than 180° then this Bit is not part of the final Binary value. This same test is now performed using the second Binary Bit (90°) and so on down to the LSB of 0.005°.

For example to convert 135.703° to a Binary value, the following steps are taken:

- 1. The Most Significant Binary bit is 180° and is obviously too large to be contained in the final Binary value so it is set to logic 0.
- 2. The Second Binary Bit has the value of 90° which is smaller than the Decimal value of 135.703°. It is part of the final Binary value so it is set to logic 1 and 90° is subtracted from the Decimal value leaving 45.703°.
- 3. The Third Binary bit has the value of 45° which again is smaller than the Decimal remainder of 45.703. It is part of the final Binary value so it is set to logic 1 and 45° is subtracted from the Decimal remainder leaving 0.703°.
- 4. The Forth Binary Bit has a value of 22.5° which is too big to fit. It is set of logic 0 and the testing continues using the Decimal value of 0.703. So far we have tested the 4 MSBs of the Binary values and the Binary solution at this point is "0 1 1 0" with 12 more Binary Bits to test.
- 5. The 5th, 6th, 7th, and 8th Binary bits are all too large and are therefore set to logic 0. The Binary value at this point is "0 1 1 0 0 0 0" with 8 more Binary Bits to test.
- 6. The Binary Bit weight of the 9th bit is 0.703° and it fits exactly into the Decimal value of 0.703. The Binary Bit is therefore set to logic 1 and the Binary answer at this point is "0 1 1 0 0 0 0 0 1". The Binary value of 0.703 is subtracted from the Decimal Value and the remainder is 0.
- 7. As the Decimal remainder is now 0 obviously none of the remaining Binary Bits will Fit into the Decimal value so they can all be set to logic 0. The final Binary answer is therefore "0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0"
- 8. The Most Significant Byte of the Binary angle contains the value "0 1 1 0 0 0 0 0" and the Least Significant Byte contains the Binary value "1 0 0 0 0 0 0 0".

IMPORTANT - When the Binary Angular Data is loaded into any channel of the DSC-36022 it **MUST** be loaded into the registers Least Significant Byte first followed by the Most Significant Byte. If this sequence is not followed the double buffering circuitry for the associated converter will not function properly; the generated angle will be incorrect (the new MSB data will be used with the previous LSB data, and the new LSB data will be put into temporary storage to be used for the next update).

The Digital to Synchro/Resolver converters used on the DSC-36022 are 14 bit converters. The two least significant bits of each Least Significant Byte are not used.

COMPUTER INTERFACE CONNECTOR

The DSC-36022 follows IBM guidelines for bus interfacing. The pin number and function of the computer interface signals are listed in Table 4.

SIGNAL I/O CONNECTOR

The converter I/O signals are brought off the DSC-36022 through a 37 pin, D type connector. These signals are listed in Table 5.

TABLE 5. I/O CONNECTOR (J1) PIN FUNCTIONS

SIGNAL	CHANNELS			
	1 (U22)	2 (U23)	3 (U24)	4 (U25)
S1	36	14	29	26
S2	18	33	11	7
S3	37	15	30	25
S4	19	34	12	6
RH	17	32	10	8
RL	35	13	28	27
+15V INPUT	22 & 3	22 & 3	22 & 3	22 & 3
-15V INPUT	21 & 2	21 & 2	21 & 2	21 & 2
GROUND	20 & 1	20 & 1	20 & 1	20 & 1

Note: External ± 15V power supplies are NOT REQUIRED if only the DSC-544 series of converter modules are mounted on the DSC-36022 circuit card assembly. These converters are powered from the Reference input signal and do not require any ± 15V power supplies.

HAZARDOUS VOLTAGES

Before use, screw the card down to the PC chassis; this is due to possible reference and signal **high voltages** present on the card.

TABLE 4. DSC-36022 COMPUTER INTERFACE PIN FUNCTIONS

PIN NO.	SIGNAL NAME	FUNCTION
A1	$\overline{\text{I/O CHECK}}$	NOT USED
A2	D7	DATA BIT 7
A3	D6	DATA BIT 6
A4	D5	DATA BIT 5
A5	D4	DATA BIT 4
A6	D3	DATA BIT 3
A7	D2	DATA BIT 2
A8	D1	DATA BIT 1
A9	D0	DATA BIT 0
A10	I/O READY	NOT USED
A11	AEN	ADDRESS ENABLE
A12	A19	NOT USED
A13	A18	NOT USED
A14	A17	NOT USED
A15	A16	NOT USED
A16	A15	NOT USED
A17	A14	NOT USED
A18	A13	NOT USED
A19	A12	NOT USED
A20	A11	NOT USED
A21	A10	NOT USED
A22	A9	ADDRESS BIT 9
A23	A8	ADDRESS BIT 8
A24	A7	ADDRESS BIT 7
A25	A6	ADDRESS BIT 6
A26	A5	ADDRESS BIT 5
A27	A4	ADDRESS BIT 4
A28	A3	ADDRESS BIT 3
A29	A2	ADDRESS BIT 2
A30	A1	ADDRESS BIT 1
A31	A0	ADDRESS BIT 0
B1	GROUND	GROUND
B2	RESET	NOT USED
B3	+5V	POWER SUPPLY
B4	IRQ2	NOT USED
B5	-5V	NOT USED
B6	DRQ2	NOT USED
B7	-12V	NOT USED
B8	$\overline{\text{0WS}}$	NOT USED
B9	+12V	NOT USED
B10	GROUND	GROUND
B11	$\overline{\text{MEMW}}$	NOT USED
B12	$\overline{\text{MEMR}}$	NOT USED
B13	$\overline{\text{IOW}}$	I/O WRITE
B14	$\overline{\text{IOR}}$	I/O READ
B15	$\overline{\text{DACK3}}$	NOT USED
B16	DRQ3	NOT USED
B17	$\overline{\text{DACK1}}$	NOT USED
B18	DRQ1	NOT USED
B19	$\overline{\text{DACK0}}$	NOT USED
B20	CLOCK	NOT USED
B21	IRQ7	NOT USED
B22	IRQ6	NOT USED
B23	IRQ5	NOT USED
B24	IRQ4	NOT USED
B25	IRQ3	NOT USED
B26	$\overline{\text{DACK2}}$	NOT USED
B27	T/C	NOT USED
B28	ALE	NOT USED
B29	+5V	POWER SUPPLY
B30	OSC	NOT USED
B31	GROUND	GROUND

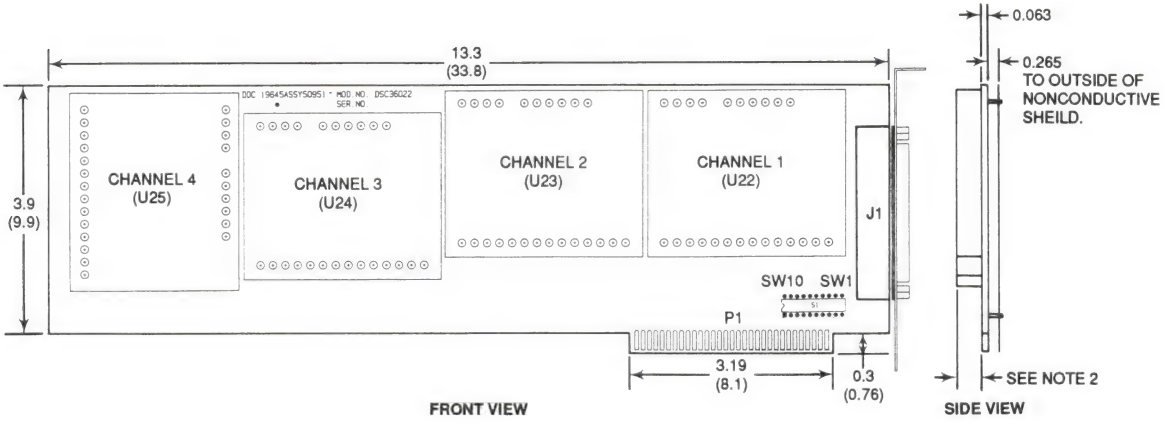
H

TIMING REQUIREMENTS

Data to the DSC-36022 is sent by the computer using standard I/O Write cycles (there are no readable registers). All of the interface logic utilizes high-speed components allowing the DSC-36022 to be addressable in zero wait state time cycles, however the following precautions must be taken.

If a step input is given to a converter, allow at least 50 ms for the output signals to stabilize.

The binary data value for the output angle must be loaded Least Significant Byte first (the 6 LSBs of the angle) followed by the Most Significant Byte (the 8 MSBs of the angle), or the double buffering scheme will not function properly causing an incorrect angle to be generated.



PHYSICAL CHARACTERISTICS		
Size (Full size IBM PC card)	in (cm)	3.9 x 13.3 x [note 2] (9.9 x 33.8 x [note 2])

Notes:
1. Specifications for the DSC-544 and DSC-644 Series are detailed in the individual data sheets. The user must supply reference voltage. The DSC-644 also requires ±15Vdc.
2. Component height: with DSC-644 modules installed, 0.565"(14.4mm) max; with DSC-544 modules installed, 0.865"(22mm) max.
3. Cut modules leads to 0.195"(4.95mm)
4. J1 ia a DB37 Jack, with male pins.

FIGURE 2. DSC-36022 MECHANICAL OUTLINE

ORDERING INFORMATION

CARD ASSEMBLY:

DSC-36022

CONVERTERS:

DSC-544

DSC-644

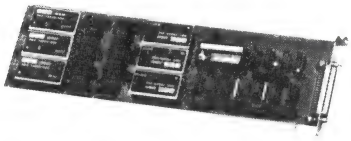
Notes:

1. The DSC-36022 is a standard, full-size IBM PC/XT/AT card 3.9"(9.9cm) x 13.3"(33.8cm) x [note 2]
2. Component Height: with DSC-644 modules installed, 0.565"(14.4mm) max; with DSC-544 modules installed, 0.865"(22mm) max.
3. Cut modules leads to 0.195"(4.95mm)
4. Modules are ordered separately as listed above and installed by the user. Sockets are included on the DSC-36022.
5. A mating connector is supplied with the DSC-36022. The connector is part of Positronic's MD 37F 20Y00 kit.

   Positronic's address is 423 N. Cambell Ave., Springfield, Missouri 65801

SDC-36015

IBM PC® COMPATIBLE 6 CHANNEL R/D-S/D CONVERTER CARD



DESCRIPTION

The SDC-36015 is a versatile, full size IBM PC card designed for 1 to 6 channels of Resolver to Digital or Synchro to Digital conversion. The SDC-36015 uses either the RDC-19200 Series (for resolver inputs) or SDC-14560 Series (for synchro inputs) hybrid converters.

The converters feature jumper programmable resolution (10, 12, 14 or 16 bits), programmable high or low bandwidth, and a high quality velocity output voltage (VEL). Output angle information is provided in two 8 bit bytes to the computer.

All information generated by the SDC-36015 is I/O mapped in four RAM locations and is available to the computer with a read command. This includes digital angle, 4 bits of turns counting, Built-In-Test (BIT), and Loss-of-Signal (LOS) information for each channel.

APPLICATIONS

Demonstration software, which shows the SDC-36015 capabilities is available with the card. The multi-channel SDC-36015 is designed for use in test systems and high performance simulation and control systems. With programmable resolution and high accuracy, the SDC-36015 is an excellent choice for applications including motor control, antenna positioning, CNC machine tooling, robot axis control and process control.

FEATURES

- *LOW COST*
- *ACCURACY TO ±1.3 ARC MINUTES*
- *EACH CHANNEL OFFERS:*

  PROGRAMMABLE RESOLUTION & BANDWIDTH

  HIGH QUALITY VELOCITY OUTPUT

  BIT, LOS, AND 4-BITS TURNS COUNTING

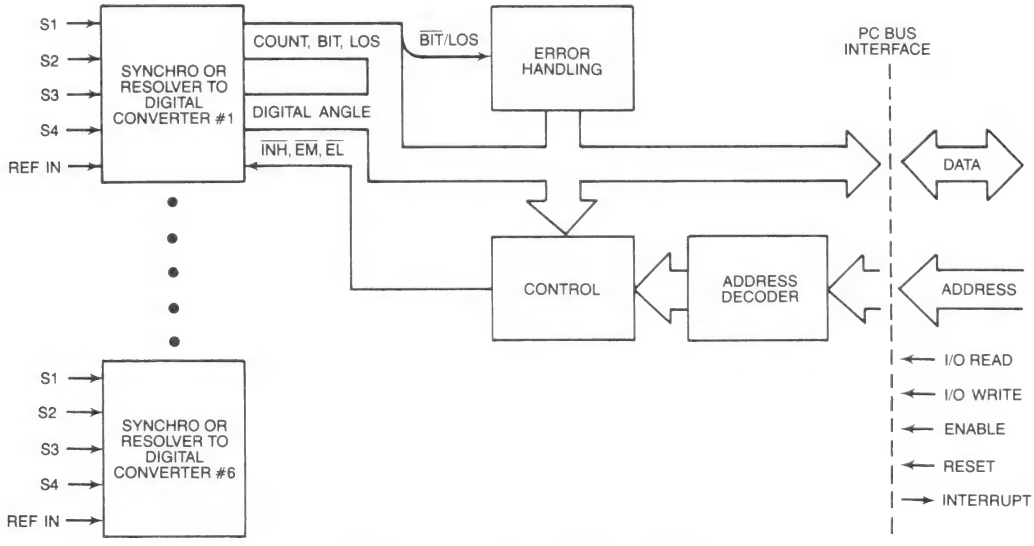


FIGURE 1. SDC-36015 BLOCK DIAGRAM

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TABLE 1. SDC-36015 REQUIREMENTS AND CAPABILITIES		
HARDWARE REQUIREMENTS IBM PC/XT/AT or Compatible with 512K RAM DDC's SDC-36015 Card		
PARAMETER	**UNITS**	**VALUE**
POWER SUPPLY Current Drain	mA	950 max with 6 channels
TEMPERATURE RANGE Operating (Case) Storage	°C °C	0 to +50 -65 to +150
PHYSICAL CHARACTERISTICS Size (Full size IBM PC card)	in (cm)	4.5 x 13.5 x 0.44 (11.4 x 34.3 x 1.1)
*Specifications for the RDC-19200 Series and SDC-14560 Series are detailed in individual data sheets.		

TECHNICAL INFORMATION

INTRODUCTION

The SDC-36015 is a full size IBM PC card which accepts up to six channels of synchro or resolver signals. Resolution (10, 12, 14, or 16 bits) and bandwidth (high or low) are jumper programmable for each converter on the SDC-36015 card.

The synchro or resolver signals are converted to digital angle information which is then stored in latches and output to the computer during read cycles. Also available for each channel are turns counting, error status, and velocity (VEL) information.

A block diagram of the SDC-36015 is shown in figure 1. The circuit provides the following information from each channel to the computer over the data bus:

1.Digital angle data in two 8 bit bytes (LSB and MSB).

2.Turns count data along with status information (BIT and LOS).

3.An error map showing the status of all channels simultaneously.

The SDC-36015 receives commands from the computer to initiate the above tasks.

Selection of SDC/RDC-1920X and SDC-1456X:
Set jumper switch "DS" (Device Select) to +5 to select SDC/RDC-1920X; GND to select SDC-1456X.

ADDRESSING REQUIREMENTS

The SDC-36015 card is preset at the factory to reside at address 300 HEX to 303 HEX. This location may be changed by moving the jumpers on the SDC-36015. Refer to table 4 for jumper positioning.

SDC-36015 OPERATION

The SDC-36015 operation begins with the computer writing a Command Word to the card to setup for the desired function. The card then updates its information, storing it in its latches. The computer then retrieves the information during a read.

The Command Word is (refer to table 4) written to the card indicating the desired channel to get information from and the condition of Interrupt, Counter Reset, and Inhibit. The COMMAND WORD is shown in figure 2 and its functions listed in table 2.

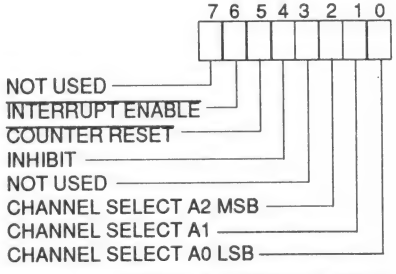


FIGURE 2. COMMAND WORD

TABLE 2. COMMAND WORD FUNCTIONS								
FUNCTION	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CHANNEL 1 ENABLED	X	X	X	X	X	0	0	0
CHANNEL 2 ENABLED	X	X	X	X	X	0	0	1
CHANNEL 3 ENABLED	X	X	X	X	X	0	1	0
CHANNEL 4 ENABLED	X	X	X	X	X	0	1	1
CHANNEL 5 ENABLED	X	X	X	X	X	1	0	0
CHANNEL 6 ENABLED	X	X	X	X	X	1	0	1
INHIBITT ON	X	X	X	0	X	X	X	X
COUNTER RESET (TURNS)	X	X	1	X	X	X	X	X
INTERRUPT ENABLED	X	1	X	X	X	X	X	X
X = don't care								

OUTPUT FUNCTION CODE SELECTION

After the Command Word is latched in memory and the desired function initialized, the SDC-36015 will output information to its data bus. The two LSBs of the Address Bus (A0 and A1) select which parameter is to be read. Table 3 lists the outupt funciton codes.

TABLE 3. OUTPUT FUNCTION CODES		
FUNCTION	**A1**	**A0**
8 LSBs of Angle	0	0
8 MSBs of Angle	0	1
Status/Count	1	0
Status/Error Map	1	1

DECODING THE 8 LSBs AND 8 MSBs OF ANGLE. The resolver shaft angle is decoded from the combination of the LSB and MSB with the following formula:

Shaft Angle = 360 • (MSB • 256 + LSB) / 65536

Where:
Shaft angle is in decimal degrees.
LSB and MSB are the decimal equivalent of the two 8 bit bytes representing angle.

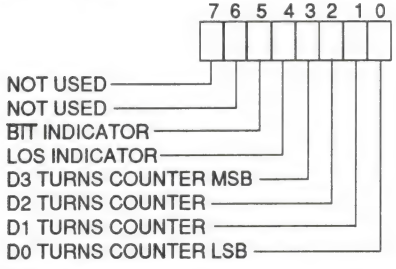
For example:
If the following digital angle data was output:

MSB 0 1 0 1 1 1 1 0
LSB 0 1 0 0 0 1 1 0

the decimal equivalent for the LSB is 69
the decimal equivalent for the MSB is 94

inserted into equation is:
Shaft angle = 360 • (94 • 256 + 69) / 65536
Shaft Angle = 132.48

STATUS/COUNT INFORMATION. Figure 3 shows the status and count information for the selected channel.



LOS Indicator - Loss-of-Signal Indicator. A logic 1 at this location indicate a loss of synchro or resolver signal to the converter.

BIT Indicator - Built-In-Test Indicator. A logic 1 at this location indicates the BIT fault flag has been raised. This occurs if the loop error signal in the converter exceeds a specified limit.

Turns Count - D0-D3. D0 is the LSB of a four bit word indicating turns count. The counter will increment/decrement at each complete revolution of the resolver or synchro shaft input.

FIGURE 3. STATUS/COUNT WORD (EACH CHANNEL)

STATUS ERROR MAP. When a BIT or LOS is indicated by any converter, the Status Error Map (see figure 4) is latched to store the status information at the precise time the error occurred. Interrupt line, IRQ3 is also latched low to indicate the fault to the computer. The interrupt handling routine should reset the interrupt flag using the interrupt enable lines as part of its function.

A logic 1 at any position indicates that either a BIT or LOS error has occurred.

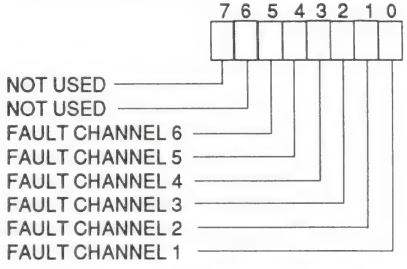


FIGURE 4. STATUS/ERROR MAP

OPERATING THE SDC-36105 WITH LESS THAN 6 CHANNELS
If the SDC-36015 is to be used with less than all six channels, or, if it is required that a specific channel does not set the INTERRUPT line, then those channels should have the interrupt function disabled.

To disable the INTERRUPT, use jumper switches E1 to E6 (for channels 1 to 6). The interrupt is disabled when the jumper is in the OFF position (The jumper position for ERR1 to ERR6 when set towards the top of the board turns the channel off and when set towars the bottom of the card turns the channel on.). The BIT and LOS information going to the data bus and the STATUS ERROR MAP is not affected by the disable function.

PROGRAMMABLE RESOLUTION AND BANDWIDTH
Each individual converter can be jumper-programmed for either 10, 12, 14 or 16 bits resolution and low (130 Hz) or high (530 Hz) bandwidth.

RESOLUTION. The resolution for each channel is set by the A and B jumper switches as follows:

A	B	Resolution
0	0	10 Bits
0	1	12 Bits
1	0	14 Bits
1	1	16 Bits

0 = jumper in OFF position
1 = jumper in ON position

BANDWIDTH. The BW jumper is set to 1 for high bandwidth (530 Hz) and set to 0 for low (130 Hz).

Switch position (BW, A, B): For channels 1,3, and 5 - the jumper positon towards the top of the card is Logic "1" ; For channels 2, 4, and 6 - the bottom of the card is Logic "1".

VELOCITY AND DYNAMIC CHARACTERISTICS
An analog voltage is generated by the converter prportional to the rate of change of the shaft angle, and is avaialble at the SDC-36015's edge connector as teh Velocity (VEL) signal.

The dynamic characteristics can be determined from the specific tables on the RDC-19200 and SDC-14560 data sheets.

The velocity output scale factor can be changed from nominal by inserting resistors R1 to R6 for channels 1 to 6, respectively. The individual converter's data sheet specifies the values of the resistors.

SOFTWARE DEVELOPMENT

For a program in assembly and a clock speed of 4.77 MHz (standard IBM XT speed) it will take approximately 15 usec to cycle the converter. If a memory refresh occurs during this period, the time will be extended; faster clock speed will reduce this time.

ADDRESSING. The SDC-36015 is pre-set to reside from address 300H to 303H. These locations may be changed by repositioning the jumpers as shown in table 4.

TABLE 4. SDC-36015 ADDRESS JUMPERS

JUMPER	ADDRESS	ON	OFF	FUNCTION
W9	A9	X		Decode 3rd LSB of HEX I/O address.
W8	A8	X		Decode 3rd LSB of HEX I/O address
W7	A7		X	Decode 2nd LSB of HEX I/O address.
W6	A6		X	Decode 2nd LSB of HEX I/O address.
W5	A5		X	Decode 2nd LSB of HEX I/O address.
W4	A4		X	Decode 2nd LSB of HEX I/O address.
W3	A3		X	Decode 1st LSB of HEX I/O address.
W2	A2		X	Decode 1st LSB of HEX I/O address.
	A1			Decoded elsewhere, not programmable

Switch position for W2-W9: The jumper position toward the top of the card is Logic "0".

INTERFACE SPECIFICATIONS

The SDC-36015 inputs place one LS TTL load each on the IBM bus and use one standard TTL signal levels to drive it. The pin number, signal name, and function of the I/O interface is listed in table 5.

TABLE 5. SDC-36015 I/O INTERFACE PIN FUNCTIONS

PIN NO.	SIGNAL NAME	FUNCTION
A1	I/O CHECK	NOT USED
A2	D7	DATA BIT 7
A3	D6	DATA BIT 6
A4	D5	DATA BIT 5
A5	D4	DATA BIT 4
A6	D3	DATA BIT 3
A7	D2	DATA BIT 2
A8	D1	DATA BIT 1
A9	D0	DATA BIT 0
A10	I/O READY	NOT USED
A11	AEN	ADDRESS ENABLE
A12	A19	ADDRESS BIT 19
A13	A18	ADDRESS BIT 18
A14	A17	ADDRESS BIT 17
A15	A16	ADDRESS BIT 16
A16	A15	ADDRESS BIT 15
A17	A14	ADDRESS BIT 14
A18	A13	ADDRESS BIT 13
A19	A12	ADDRESS BIT 12
A20	A11	ADDRESS BIT 11
A21	A10	ADDRESS BIT 10
A22	A9	ADDRESS BIT 9
A23	A8	ADDRESS BIT 8
A34	A7	ADDRESS BIT 7
A25	A6	ADDRESS BIT 6
A26	A5	ADDRESS BIT 5
A27	A4	ADDRESS BIT 4
A28	A3	ADDRESS BIT 3
A29	A2	ADDRESS BIT 2
A30	A1	ADDRESS BIT 1
A31	A0	ADDRESS BIT 0

TABLE 5. SDC-36015 - continued

PIN NO.	SIGNAL NAME	FUNCTION
B1	GROUND	Ground
B2	RESET	System Reset
B3	+5V	Power Supply
B4	IRQ2	Not Used
B5	-5V	Power Supply
B6	DRQ2	Not Used
B7	-12V	Power Supply
B8	$\overline{0WS}$	Not Used
B9	+12V	Power Supply
B10	GROUND	Ground
B11	$\overline{MEMW}$	Not Used
B12	$\overline{MEMR}$	Not Used
B13	$\overline{IOW}$	I/O Write
B14	$\overline{IOR}$	I/O Read
B15	$\overline{DACK3}$	Not Used
B16	DRQ3	Not Used
B17	$\overline{DACK1}$	Not Used
B18	DRQ1	Not Used
B19	DACK0	Not Used
B20	CLOCK	Not Used
B21	IRQ7	Not Used
B22	IRQ6	Not Used
B23	IRQ5	Not Used
B24	IRQ4	Not Used
B25	IRQ3	Interrupt 3
B26	$\overline{DACK2}$	Not Used
B27	T/C	Not Used
B28	ALE	Not Used
B29	+5V	Power Supply
B30	OSC	Not Used
B31	GROUND	Ground

SDC-36015 EDGE CONNECTOR

The SDC-36015's edge connector is wired as listed in table 6.

WARNING:
Before using , screw the card down to the PC chassis; this is due to possible reference and signal **high voltages** present on the card.

TABLE 6. SDC-36015 EDGE CONNECTOR WIRING

CHANNEL	1	2	3	4	5	6
S1	18	9	15	24	12	21
S2	37	27	34	6	31	3
S3	19	28	16	25	13	22
S4	30	10	35	7	32	4
VEL	29	8	36	5	33	2
REF IN	11	26	17	23	14	20
GND	1	1	1	1	1	1

CAUTION:
Do not connect REF IN to GND; the reference is single-ended on the card, and GND is PC chassis ground.

TIMING REQUIREMENTS

The timing requirements of the converters (RDC-19200 or SDC-14560) are shown in figures 5 to 7. The CPU I/O Read and Write timing of the IBM Bus are shown in figure 8.

When the Inhibit command is initiated there is a 500 nsec delay before data from the converter is valid. If the converter is in the middle of updating its count, then a 400 to 700 nsec delay may also occur. As a result of these two delays, the converter's repetition rate for retrieving data can not be faster than 1200 nsec.

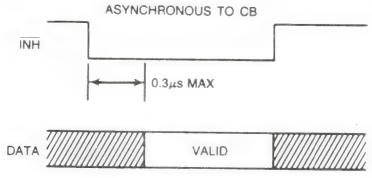


FIGURE 5. INHIBIT TIMING

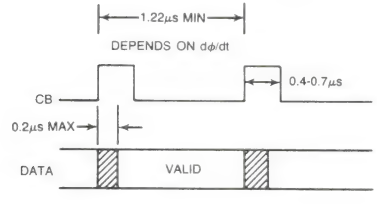


FIGURE 6. CONVERTER BUSY TIMING

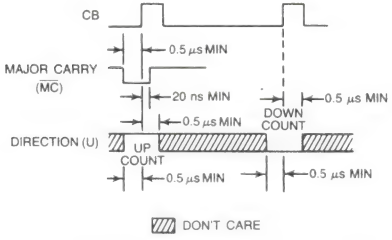


FIGURE 7. INCREMENTAL AND TURNS COUNTING TIMING

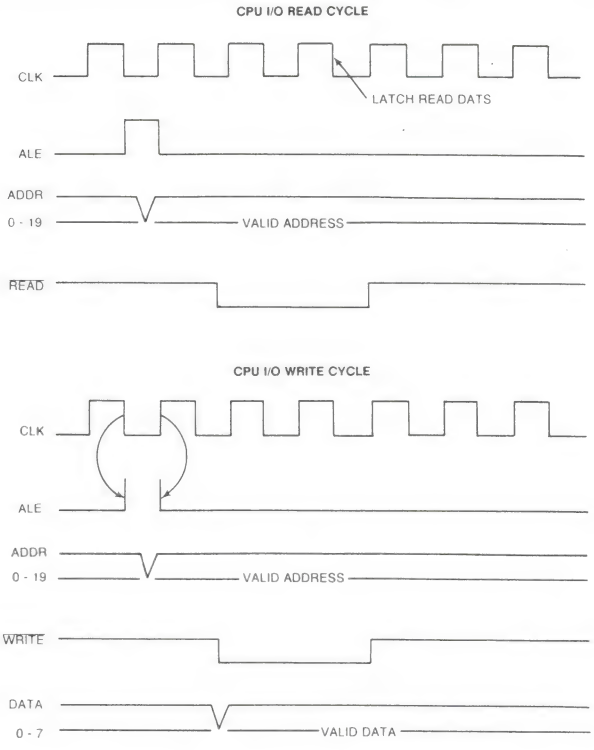


FIGURE 8. CPU I/O READ AND WRITE CYCLES

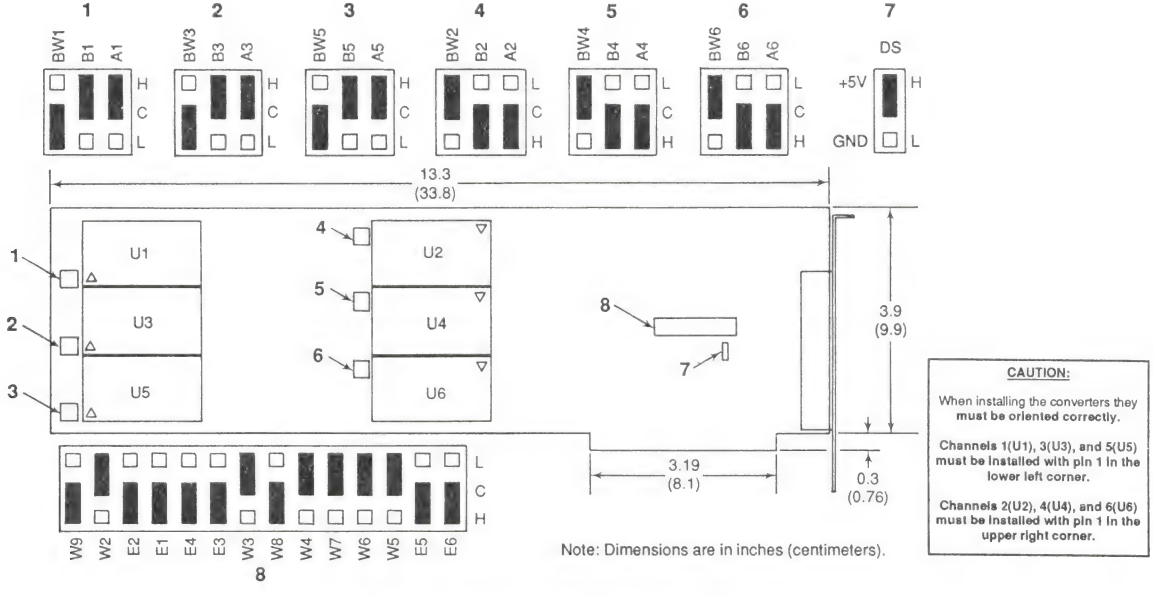


FIGURE 9. SDC-36015 MECHANICAL OUTLINE

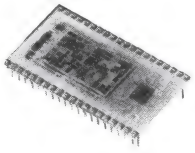
ORDERING INFORMATION

CARD ASSEMBLY:

SDC-36015

Notes:
1. The SDC-36015 is a standard, full-size IBM PC/XT/AT card (4.5 x 13.5 x 0.44 inches).
2. Converters are ordered separately as listed below and installed by the user. Sockets are included with the SDC-36015.

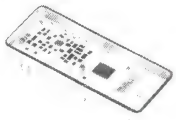
CONVERTERS:



RDC-1920X-30X

- Accuracy
  - 0 = 10 min +1 LSB(1) (16 LSBs Differential Linearity, RDC-19200 and RDC-19202 only)
  - 1 = 8 min +1 LSB (12 LSBs Differential Linearity)
  - 2 = 4 min +1 LSB (8 LSBs Differential Linearity)
  - 3 = 3 min +1 LSB (4 LSBs Differential Linearity)
  - 4 = 2 min +1 LSB (4 LSBs Differential Linearity)
- Configuration:
  - 0 = 11.8V, 2% Linearity
  - 1 = 11.8V, 0.7% Linearity
  - 2 = 2V, 2% Linearity
  - 3 = 2V, 0.7% Linearity
- RDC = RDC-19200 Series
- SDC = SDC-19204 Series (see note 3)

Notes:
(1) Vel and e not characterized on models RDC-19200-300 and RDC-19202-300.
(2) Differential Linearity is x LSB in the 16th bit.
(3) See SDC-19204 data sheet and/or contact factory for synchro input option.



SDC-1456X-XXX

- Accuracy:
  - 1 = 6 min. +1LSB
  - 2 = 4 min. +1LSB
  - 4 = 2 min. +1LSB
  - 5 = 1 min. +1LSB
- Reliability Grade:
  - 0 = Standard DDC procedures.
  - 1 = Military processing available.*
  - 2 = Military processing available but without QCI testing.*

  *Consult factory for details.
- Operation temperature range:
  - 1 = −55°C to +125°C
  - 3 = 0°C to + 70°C
- Configuraton:
  - 0 = 11.8V, 400Hz, Synchro
  - 1 = 90V, 400Hz, Synchro
  - 2 = 90V, 60Hz, Synchro
  - 3 = 11.8V, 400Hz, Synchro, trimmed velocity
  - 4 = 26V, 400Hz, Resolver
  - 5 = 11.8V, 400Hz, Resolver
  - 6 = 11.8V, 400Hz, Resolver, trimmed velocity
  - 7 = 1V, 400Hz, Direct Resolver
  - 8 = 1V, 60Hz, Direct Resolver
  - 9 = 1.0V, 400Hz, Direct Resolver trimmed velocity

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SECTION I
SPECIAL FUNCTIONS

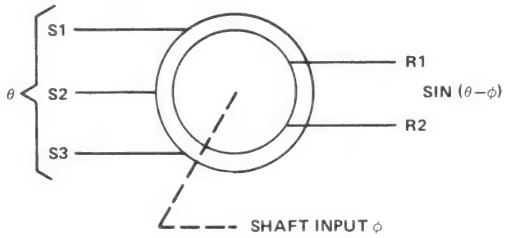
PRODUCT SUMMARY TABLE

FUNCTION	RESOLUTION	MODEL	ACCURACY	PACKAGE	DESCRIPTION/FEATURES	PAGE
LVDT/RVDT TO DIGITAL CONVERTER	12 Bit or 14 Bit	**DTC-19300**	0.25%, 0.05%	36 Pin DDIP 0.78 x 1.9 x 0.21"	12 or 14 Bit LVDT (Linear Variable Differential Transformer) or RVDT (Rotary VDT) to digital converter which also supplies the ac excitation; Frequency, signal gain, and resolution are all programmable. Also features velocity and Built-In-Test outputs.	I-3
* **LVDT/RVDT TO DIGITAL CONVERTER**	12 bit	**DTC-19305**	0.15%	1.0 x 0.8 x 0.2"	Low cost. 12 Bit LVDT or RVDT to digital converter in a very small package. Based upon a monolithic ratiometric tracking converter. Resistor programmable sum and difference input range.	I-9
SYNCHRO BOOSTER AMPLIFIER	—	**SBA-SERIES AMPLIFIER**	± 3'	7.4 x 5.1 x 1.8" (400Hz) 7.4 x 5.1 x 2.6" (60Hz) Chassis	25 VA drive (6 Ω active load). Kick circuit prevents 180° hang-up. powered from reference. Short circuit, transient, and overload protected.	I-12
U.S. NAVY STANDARD ELECTRONIC MODULES	—	**SEM MODULES**	—	—	Many S/D, D/S, A/D, D/A, and 1553 Data Bus key codes. Consult factory.	D-3

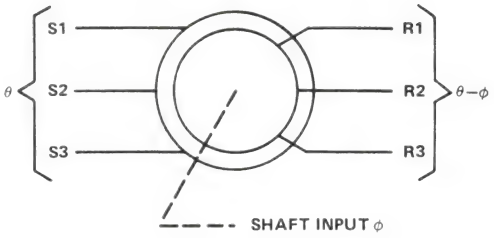
NOTES: Most hybrid products are available with Military Processing (Contact Factory)

* New Product

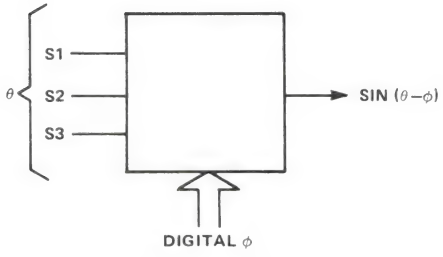
BACKGROUND INFORMATION



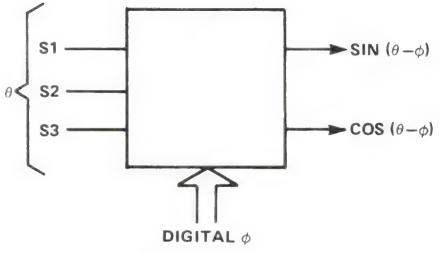
MECHANICAL CT



MECHANICAL CDX



SOLID STATE CT



SOLID STATE CDX

FIGURE 1

INTRODUCTION

This section will explain several special synchro conversion functions and their applications. The functions discussed (Figure 1) will be a solid state control transformer (CT) and a solid state control differential transmitter (CDX).

THEORY OF OPERATION

Solid state CTs and CDXs are the electronic equivalents of their mechanical counterparts, the major difference being that the mechanical shaft is replaced with a digital word (see Figure 1). Thus, the two inputs are a synchro angle here referred to as θ, and a digital input referred to as ϕ. The output from a CT is a voltage derived from the reference whose amplitude is equal to $\sin(\theta-\phi)$, while the output from a CDX includes both $\sin(\theta-\phi)$ and $\cos(\theta-\phi)$ to form a resolver output. Both devices use special multiplying D/As to solve the equation:

$$\sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi.$$

The CDX also uses a cos control transformer to generate $\cos(\theta-\phi)$.

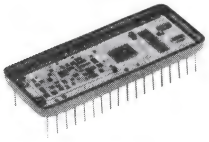
APPLICATIONS

Control transformers are most frequently used as error signal generators in closed loop servos. They are useful whenever digital angles must be subtracted from analog synchro or resolver angles, particularly when offset or correction angles must be provided under computer control.

Control differential transmitters (CDX) subtract digital angles from analog synchro or resolver angles. They are used to provide angle offsets or correction angles when a resolver or synchro type output is required, and are especially adapted to computer controlled systems.

DTC-19300

LVDT/RVDT TO DIGITAL CONVERTER



DESCRIPTION

The DTC-19300 is a 12 or 14 bit LVDT (Linear Variable Differential Transformer) or RVDT (Rotary Variable Differential Transformer) to digital converter which also supplies the AC excitation to drive the LVDT. Internal AC excitation voltage, frequency, signal gain, and resolution are all programmable for optimum system performance. Packaged in a 36 pin hybrid, the DTC-19300 also features Velocity (VEL), and Built-In-Test (BIT) outputs. The three-state digital outputs are provided in a two byte format, for easy computer interface.

The DTC-19300 has been designed precisely for use with the LVDT. Inherent characteristics of the DTC-19300, such as the input to output phase shift, have been given considerable attention. The converter's reference voltage is derived from, and is in phase with, the LVDT output signal. Therefore, any errors due to the transducer's phase shift are virtually eliminated.

Programmability of DTC-19300 is used to accomodate the broadest range of LVDTs available. An analog velocity voltage (VEL) is a standard output from the DTC-19300. VEL is a DC level proportional to the core's linear rate of change, and can be used for velocity feedback.

APPLICATIONS

The DTC-19300 provides many features previously supplied by individual system components. Because of its internal AC source, programmable features, fault indicator (BIT), and velocity output (VEL), the need for other system circuits is minimized. The DTC-19300 is an excellent choice for applications using the LVDT transducer for position feedback, such as military/commercial aerospace and industrial control systems.

FEATURES

- *INTERNAL OSCILLATOR PROGRAMMABLE FOR VOLTAGE AND FREQUENCY*
- *PROGRAMMABLE SIGNAL GAIN*
- *PROGRAMMABLE RESOLUTION 12 BIT OR 14 BIT*
- *VELOCITY OUTPUT*
- *BUILT-IN-TEST OUTPUT*
- *THREE-STATE, TWO-BYTE DIGITAL OUTPUT*

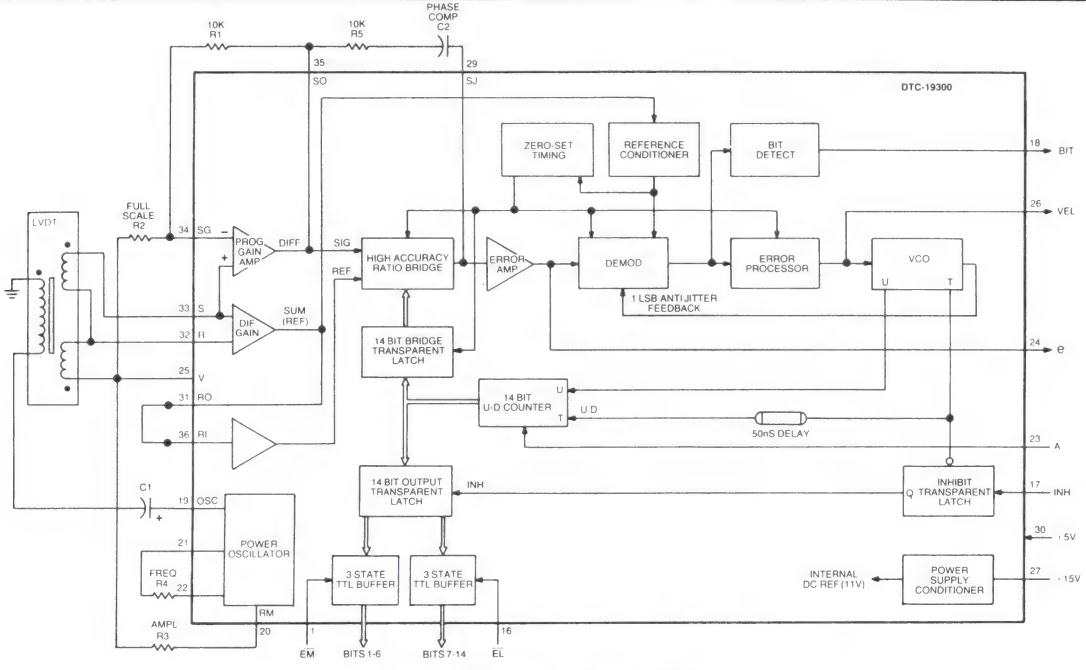


FIGURE 1. DTC-19300 BLOCK DIAGRAM

TABLE 1. DTC-19300 SPECIFICATIONS

PARAMETER	VALUE	DESCRIPTION
RESOLUTION	12 or 14 bits	Programmable.
ACCURACY AT ROOM TEMP.	0.25, 0.05% of Reading	Tempco = 0.001% / °C max. See Ordering Information.
REPEATABILITY	1 LSB max	
DIFFERENTIAL LINEARITY	1 LSB max	
FREQUENCY OUT (OSC, Pin 19)		
Frequency	4.7kHz ±10%	Tunable down to 1kHz; disable with R4 = ∞ (see description).
Voltage	2.7V rms ±20%	20% at room temp, add 0.3% / °C. Scalable down (see description).
Current Drive	20mA rms min	
Protection		Short circuit, overcurrent, and voltage transient protected.
REFERENCE IN (RI)		
Full Scale Voltage	2V rms ±10%	
Input Impedance	20M Ohms min	Transient protected voltage follower.
REFERENCE (R)		
Voltage	1V rms ±10%	
Input Impedance	20M Ohms min	Transient protected voltage follower.
SIGNAL IN (S)		
Full Scale Voltage	2 Vrms	
Input Impedance	20M Ohms min	Transient protected voltage follower.
DIGITAL INPUTS/OUTPUTS		
Logic Type		TTL/CMOS compatible.
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Loading	10 μA max	Pull-up current source to +5V//5pF, CMOS transient protected.
$\overline{\text{INH}}$ (Inhibit)		Logic 0 inhibits, data valid within 0.5μs Logic 1 enables.
$\overline{\text{EM}}$ (Enable Bits 1-6)		Logic 0 enables, data valid within 150 ns.
$\overline{\text{EL}}$ (Enable Bits 7-14)		Logic 1 = high impedance, data high Z within 100 ns.
A (Resolution Control)		Logic 1 = 14 bit resolution. Logic 0 = 12 bit resolution.
OUTPUTS		
Parallel Data	12 or 14 bits	Bipolar two's complement. Bit 1 = MSB, bit 14 or bit 12 = LSB.
$\overline{\text{BIT}}$ (Built in Test)		Logic 0 for BIT condition (converter malfunction).
Drive Capability	Logic 0 = 1 TTL load Logic 1 = 10 TTL loads High Z = 10μA//5pF max	1.6mA at 0.4V max +50pf. −0.4mA at 2.8V min +50pf. When in the third state.
ANALOG OUTPUTS		
V (Analog Ground)	5.5VDC nom	
VEL (Velocity)		VEL is with respect to V.
Scaling	±4V±15%	1 (14 bit) or 4 (12 bit) ranges per second.
Scaling TC	200 PPM/°C max	
Reversal Error	2% max	
Linearity	2% of output max	
Zero Offset	10mV max	
Noise & Ripple	50mV rms	
AC peak/DC avg	0.5% max	
Load	40K Ohms min	
DYNAMIC CHARACTERISTICS		
Tracking Rate	1 full range per sec, min	
Bandwidth, Closed Loop	18 Hz	
Ka	1600 1/sec^2	
A1	0.4 1/sec	
A2	4000 1/sec	
A	40 1/sec	
B	20 1/sec	
acc for 1 LSB lag	0.1 full ranges per sec^2	
Settling time – half scale step	150 ms	

POWER SUPPLIES			
Nominal Voltage and Range		+5VDC±10%	+15VDC±5%
Max Voltage w/o Damage		+8VDC	+18VDC
Current, Peak		10mA max	25mA max, + $\sqrt{2}$ I_{osc} rms.
Current, Average		10mA max	35mA max, + 0.9 x 0.5 x I_{osc} rms.

TABLE 1. DTC-19300 SPECIFICATIONS (Continued) – Specifications apply over temperature and power supply ranges.

PARAMETER	VALUE	DESCRIPTION
TEMPERATURE RANGES		
Operating, Ambient		
−3XX	0°C to +70°C	
−1XX	−55°C to +125°C	
Storage	−65°C to +150°C	
PHYSICAL CHARACTERISTICS		
Size	0.78 x 1.9 x 0.21 inches (20 x 48 x 5.3 mm)	36 pin DDIP
Weight	1 oz (28 gm)	

TECHNICAL INFORMATION

INTRODUCTION

The circuit shown in Figure 1, DTC-19300 Block Diagram, consists of four main parts: signal input conditioning, a feedback loop (whose elements are the high accuracy ratio bridge, demodulator, error processor, VCO and up-down counter), a power oscillator to excite the LVDT, and digital interface circuitry (including various latches and buffers).

In the LVDT, position output is transmitted as a differential voltage that varies linearly with changes in the core position. The DTC-19300 receives the differential and sum voltage at its inputs and internally produces a digital position δ which tracks the differential position λ to within the specified accuracy of the converter.

A high accuracy ratio bridge is used to compute $(\lambda - \delta)$, where:

λ = the LVDT's core position

δ = the digital position contained in the converter's up-down counter.

The tracking process consists of continually adjusting δ to make $(\lambda - \delta) \blacklozenge 0$, so that δ will represent the core's position, λ.

The ratios bridge output is fed to a demodulator whose output is an analog DC level proportional to $(\lambda - \delta)$. The error processor receives its input from the demodulator and integrates the $(\lambda - \delta)$ error signal which then drives a Voltage Controlled Oscillator (VCO).

Functionally, the up-down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a Type II tracking servo. In a type II servo, the VCO always settles to the counting rate which makes the $d\delta/dt$ equal to $d\lambda/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

POWER OSCILLATOR

The DTC-19300 contains an internal power oscillator. The OSC output (pin 19), can be programmed for voltage and frequency. The output voltage is 2.7V rms, scalable down with an external resistor R3 connected between RM (pin 20) and V (pin 25). The frequency is 5K Hz, tunable to 400 Hz with an external resistor R4 connected between RF1 (pin 21) and RF2 (pin 22). If desired, an external oscillator can be used in place of the internal oscillator.

SOLID STATE BUFFERED INPUTS

The signal and reference inputs are voltage follower inputs with high impedance that do not load the LVDT. The maximum transient peak voltage should not exceed 100V.

DIGITAL INTERFACE

The digital interface circuitry has three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the DTC-19300.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the DTC-19300, applying an INHIBIT ($\overline{INH}$) command will lock the data in the **Output Transparent Latch** without interfering with the continuous tracking of the feedback loop. Therefore, the digital position always updates, and the INHIBIT can be applied for an arbitrary amount of time. The **Inhibit Transparent Latch** and the **50 ns delay** are part of the Inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 17) paragraph.

LOGIC OUTPUT

Logic outputs from the DTC-19300 consist of the LVDT core's digital position in 12 or 14 parallel data bits. All logic outputs are short-circuit proof to ground and +5V. The internal T signal is a positive, 0.4 to 0.7μs pulse. Data changes about 50ns after the leading edge of T, and the position is determined by the sum of the bits at logic 1. Digital outputs are three-state and are provided in two bytes: bits 1 through 6 (MSBs) which are enabled by the signal $\overline{EM}$, and bits 7 through 14 (LSBs) which are enabled by the signal $\overline{EL}$. Outputs are valid (logic 1 or 0) 150ns max after setting $\overline{EM}$ or $\overline{EL}$ low, and are high impedance within 100ns max of setting $\overline{EM}$ or $\overline{EL}$ high. Both $\overline{EM}$ and $\overline{EL}$ are internally pulled-up to +5V at 100nA max.

INHIBIT ($\overline{INH}$, PIN 17)

The $\overline{INH}$ input locks the Output Transparent Latch (figure 1) so the bits will remain stable while data is being transferred. The output is stable 0.5μs after $\overline{INH}$ is driven to logic 0.

A logic 0 applied to the T input latches data, and a logic 1 applied to T allows the bits to change. The Inhibit Transparent Latch prevents the transmission of invalid data when there is an overlap between T (VCO clock to up-down counter) and $\overline{INH}$. While the counter is not being updated, T is at a logic 0 and the Inhibit

Latch is transparent. When T goes to a logic 1, the Inhibit Latch is locked. If T occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until T returns to logic 0; if $\overline{INH}$ is applied during T, the latch will not lock until the T pulse is over. The purpose of the 50ns delay is to prevent a race condition between T and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied.

Figure 2 illustrates the Inhibit Timing. Whenever an input position change occurs, the converter changes the digital position in 1 LSB steps and generates a T pulse, delayed by 50ns, nom. Valid data is available at the outputs 0.2μs after the leading edge of T. An $\overline{INH}$ input, regardless of its duration, does not affect the converter update.

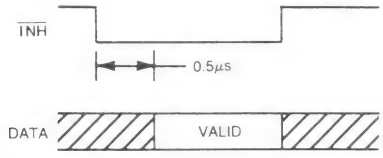


FIGURE 2. INHIBIT TIMING

A simple method of interfacing to a computer is:

1. apply $\overline{INH}$,
2. wait 0.5μs min.,
3. transfer data and release $\overline{INH}$.

As long as the converter's maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as when power is initially applied, the response will be critically damped. Figure 3 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to final value is a function of the small signal settling to final value.

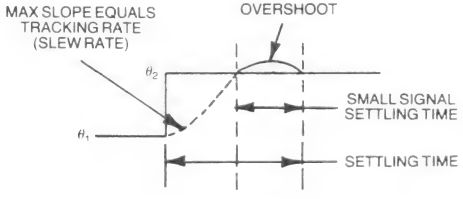


FIGURE 3. RESPONSE TO A STEP INPUT

BUILT-IN-TEST ($\overline{BIT}$, PIN 18)

The BIT output monitors the level of the demodulator and if it exceeds approximately 65 bits, the logic level at $\overline{BIT}$ will change from logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also be set for an over-velocity condition because the converter loop cannot maintain input-output sync, and if the converter malfunctions where it cannot maintain the loop at a null.

VELOCITY (VEL, PIN 26)

The Velocity output (VEL) from the DTC-19300 is a DC voltage proportional to the angular velocity $d\lambda/dt = d\delta/dt$. The velocity is input to the second integrator, as shown in figure 4. Its linearity is dependent solely on the linearity of the voltage controlled oscillator (VCO). An open loop Bode plot is shown in figure 5.

Bandwidth (BW) and the acceleration constant (Ka) can be determined by the following formula:

$$\text{Closed Loop Bandwidth (Hz)} = \frac{\sqrt{2} \cdot A}{\pi}$$

Output VEL is not required for normal operation of the converter; V is used as an internal DC reference. Maximum loading on V and VEL is 40K.

The simple filter shown in figure 6 will, for the Velocity output, eliminate the one overshoot for a step velocity input and will filter the carrier frequency ripple.

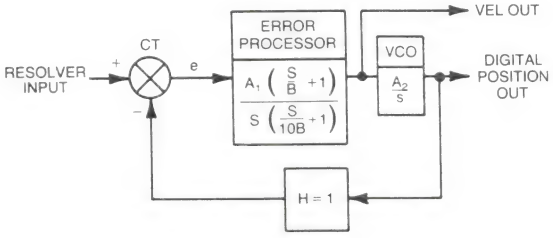


FIGURE 4. CONTROL LOOP BLOCK DIAGRAM

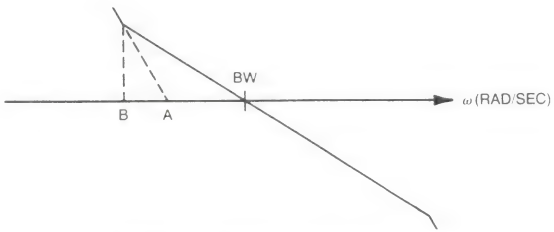


FIGURE 5. OPEN LOOP BODE PLOT

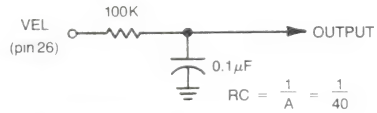


FIGURE 6. VELOCITY FILTER

ELECTRONIC LIMIT STOPS

The DTC-19300 incorporates electronic limit stops and will not count up past +FS−1 LSB or down past −FS.

OUTPUT CODING

Table 2 lists the DTC-19300 full scale (FS) and half scale (HS) digital output codes. Table 3 lists the weight of each bit with respect to the full scale output.

TABLE 2. DIGITAL OUTPUT CODES

SCALE	(MSB)				DIGITAL OUTPUT									(LSB)
+FS – 1 LSB	0	1	1	1	1	1	1	1	1	1	1	1	1	1
+HS	0	1	0	0	0	0	0	0	0	0	0	0	0	0
+1 LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	1
ZERO	0	0	0	0	0	0	0	0	0	0	0	0	0	0
– LSB	1	1	1	1	1	1	1	1	1	1	1	1	1	1
–HS	1	1	0	0	0	0	0	0	0	0	0	0	0	0
–FS	1	0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 3. BIT WEIGHTS

BIT		WEIGHT
1	(MSB)	0.5 full range = FS
2		0.25 full range = HS
3		0.125 full range
4		0.0625 full range
5		0.03125 full range
6		0.015625 full range
7		0.0078125 full range
8		0.0039063 full range
9		0.0019531 full range
10		0.0009766 full range
11		0.0004833 full range
12		0.0002441 full range
13		0.0001221 full range
14	(LSB)	0.0000611 full range

SETTING UP AND PROGRAMMING THE DTC-19300

To set up and operate the DTC-19300, refer to figure 7 and proceed as follows:

INTERNAL OSCILLATOR

1. Select the LVDT's operating frequency.
2. Calculate the value of R4 (the oscillator frequency setting resistor) by using the LVDT frequency in the equation below.

$$R4\,(\text{in Ohms}) = \frac{1 \times 10^{12}}{(\text{Frequency Hz})^2} - 45.6\text{K}$$

3. Calculate the value of R3 (the oscillator amplitude setting resistor), which results in a 0.8V rms between pin 32 (R) and pin 25 (V), when the LVDT is at its null position (core in the center). This usually requires a 0.8V rms input to the LVDT primary. Proceed as follows:
   a. Use the LVDT turns ratio (usually 1:1) to calculate the oscillator output with the equation below:

$$\text{Vosc} = 0.8 \text{ volts} \times \text{turns ratio}$$

   b. Calculate the value of R3 with the equation below:

$$R3 = \frac{\text{Vosc} \times 100\text{K}}{2.7 - \text{Vosc}}$$

   c. Calculate the value of the coupling capacitor C1 so that its impedance will be less than 1/10 the impedance of the LVDT at the operating frequency.

CONVERTER FULL SCALE

4. Calculate the value of R2 (full scale setting resistor) with the LVDT at full travel. This results in 1.6V rms between pin 35 (SO) and pin 25 (V). Use the following equation:

$$R2 = \frac{10\text{K} \times \text{pin 33 (S) voltage}}{1.6 - \text{pin 33 (S) voltage}}$$

PHASE COMPENSATION

5. At full travel, monitor pin 24 (e) voltage with an oscilloscope and determine the value for C2 that gives minimum output. This value (of C2) can be used for all applications which use the same LVDT.

CONVERTER RESOLUTION

6. Select 12 bit or 14 bit operating mode. The 12 bit mode provides faster response to input variations and is set by grounding pin 23 (A). The 14 bit mode provides higher resolution and is set by connecting pin 18 ($\overline{\text{BIT}}$ output) to pin 23 (A).

In both modes, if the $\overline{\text{BIT}}$ line goes low indicating an error condition (the error signal to error processor and VCO is too large), the DTC-19300 is set to 8 bit mode so that the error can be driven to null faster. Once this happens, the converter returns to the original setting.

Note

Consult with the factory for use of the converter with 2-wire LVDTs.

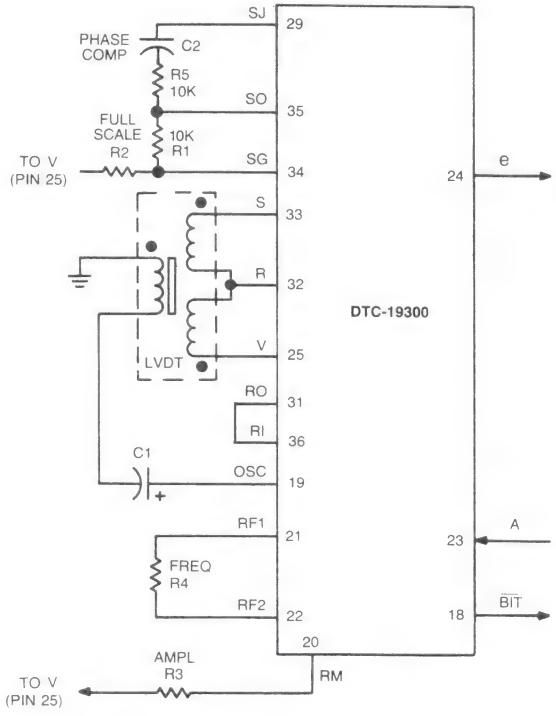
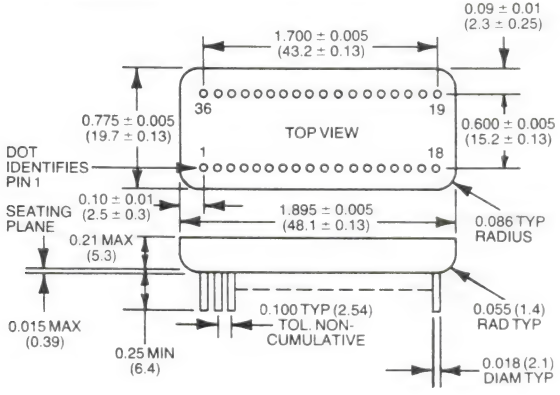


FIGURE 7. DTC-19300 SET-UP

TABLE 4. DTC-19300 PIN FUNCTIONS

PIN NO.	TITLE	I/O	FUNCTION
1	$\overline{EM}$	I	Enable MSBs. Logic 0 enables digital output bits 1-6. Logic 1 disables these bits.
2	1	O	Digital Output Bit 1 (MSB all modes).
3	2	O	Digital Output Bit 2.
4	3	O	Digital Output Bit 3.
5	4	O	Digital Output Bit 4.
6	5	O	Digital Output Bit 5.
7	6	O	Digital Output Bit 6.
8	7	O	Digital Output Bit 7.
9	8	O	Digital Output Bit 8.
10	9	O	Digital Output Bit 9.
11	10	O	Digital Output Bit 10.
12	11	O	Digital Output Bit 11.
13	12	O	Digital Output Bit 12 (LSB 12 Bit Mode).
14	13	O	Digital Output Bit 13.
15	14	O	Digital Output Bit 14 (LSB 14 Bit Mode).
16	$\overline{EL}$	I	Enable LSBs. Logic 0 enables digital output bits 7-14. Logic 1 disables these bits.
17	$\overline{INH}$	I	Inhibit. Output valid 0.5μs after $\overline{INH}$ is logic 0.
18	$\overline{BIT}$	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds approximately 65 bits.
19	OSC	O	Power oscillator output.
20	RM	I	Reference Magnitude. Power amplifier amplitude adjust.
21	RF1	I	Reference Frequency. Power amplifier frequency adjust.
22	RF2	I	Reference Frequency. Power amplifier frequency adjust.
23	A	I	Resolution Control. Sets resolution to 12 or 14 bits. Set for 14 bit mode by connecting the $\overline{BIT}$ (pin 18) to A (pin 23). Set for 12 bit mode by grounding A.
24	e	O	AC Error.
25	V	O	Internal DC reference voltage, +5.5V.
26	VEL	O	Velocity.
27	+15V	I	Supply Voltage.
28	GND	–	Ground.
29	SJ	I	Summing Junction.
30	+5V	I	Supply Voltage.
31	RO	O	Reference Out.
32	R	I	LVDT Reference input.
33	S	I	LVDT Signal input.
34	SG	I	Signal Amplifier Gain Point.
35	SO	O	Signal Amplifier Output.
36	RI	I	Full Scale Reference Input.



Notes:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is electrically floating.

G **FIGURE 8. DTC-19300 MECHANICAL OUTLINE**

ORDERING INFORMATION

DTC-19300-X X X

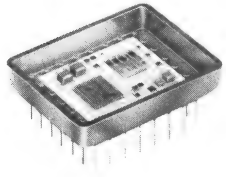
Accuracy:
1 = 0.25% of reading +3 LSB (at room temp.)
2 = 0.05% of reading +3 LSB (at room temp.)

Reliability Grade:
0 = Standard DDC procedures.
1 = Fully compliant with MIL-STD 883.
2 = Screened to MIL-STD-883 but without QCI testing.

Temperature Range:
1 = −55°C to +125°C
3 = 0°C to +70°C

DTC-19305 SERIES

12 BIT LVDT/RVDT TO DIGITAL CONVERTER



PRELIMINARY

DESCRIPTION

The DTC-19305 series are 12-bit tracking LVDT (Linear Variable Differential Transformer) or RVDT (Rotary Variable Differential Transformer) to digital converters. The DTC-19305, packaged in a small 26 pin plug-in (0.8" x 1.0") hybrid features: resistor programmable sum and difference input range, low power: ±5v dc at 10 ma=100 mw typ, 12-bit ratiometric tracking converter, convenient microprocessor digital interface, high reliability and low cost- single monolithic chip, $\overline{BIT}$ output for converter malfunction, and under and over-range indication. An analog velocity voltage (VEL) is a standard output for the DTC-19305.

APPLICATIONS

The DTC-19305 provides many features previously supplied by individual system components. The need for other system circuits is minimized because of the fault indicator ($\overline{BIT}$) and velocity output (VEL). The DTC-19305 is an excellent choice for applications using the LDVT transducer for position feedback, such as military/commercial aerospace and industrial control systems.

FEATURES

- *SMALL SIZE: 0.8" X 1.0" HYBRID PACKAGE*
- *RESISTOR PROGRAMMABLE SUM AND DIFFERENCE INPUT RANGE*
- *LOW POWER: ±5V DC AT 10 MA 100 MW TYP*
- *12-BIT RATIOMETRIC TRACKING CONVERTER*
- *HIGH RELIABILITY AND LOW COST-SINGLE MONOLITHIC CHIP*
- *$\overline{BIT}$ OUTPUT FOR CONVERTER MALFUNCTION*
- *UNDER AND OVER-RANGE INDICATION*

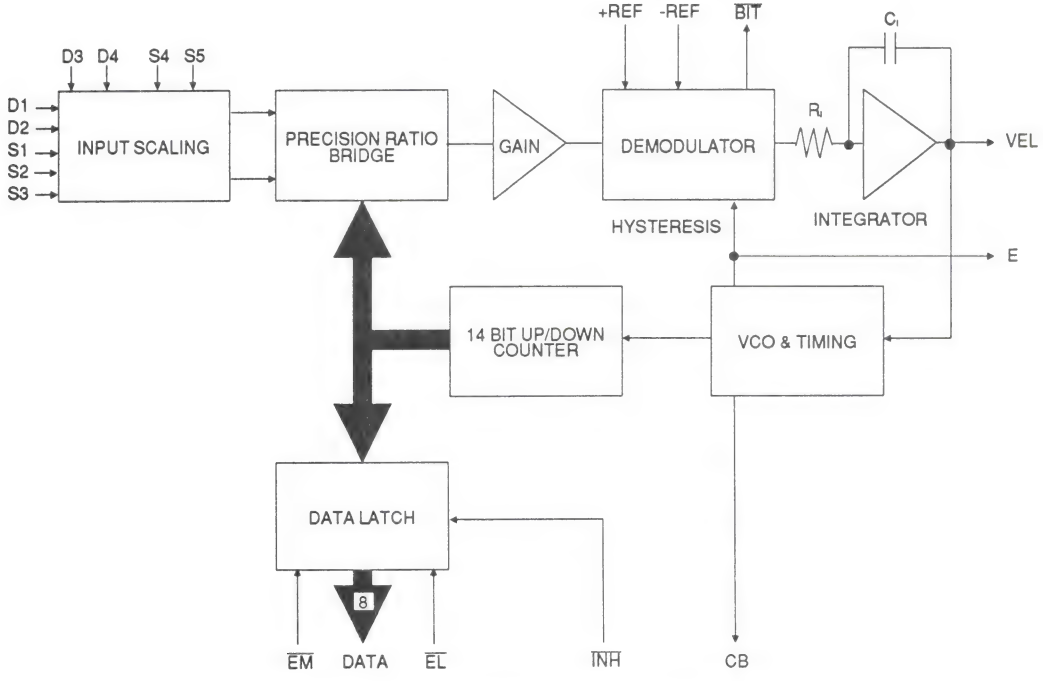


FIGURE 1. DTC-19305 BLOCK DIAGRAM

TABLE 1. DTC-19305 SPECIFICATIONS		
PARAMETER	**UNIT**	**VALUE**
RESOLUTION	Bits	12
ACCURACY	%	0.15 + 3 LSB (see note)
REPEATABILITY	LSB	1 max
DIFFERENTIAL LINEARITY	LSB	0.5 max
DIFFERENCE INPUT		
Frequency	Hz	360 - 5000
Voltage Range	Vrms	2 nom, for no scaling resistor to 20 with scaling resistor
Input Impedance		
single ended	Ohm	40k ±1%
differential	Ohm	80k ±1%
Common Mode Range	V	20 peak max, 100 pk transient
SUM INPUT		
Frequency	Hz	360 - 5000
Voltage Range	Vrms	2 nom, for no scaling resistor to 20 with scaling resistor
Input Impedance		
single ended	Ohm	40k split ±1%
differential	Ohm	80k split ±1%
Common Mode Range	V	20 peak max, 100 pk transient
DC ERROR OUTPUT (E)		
Gradient	Vdc	-1.25 per +1 LSB of error, nom
Range	LSBs	±3 min
Load	mA	±0.5 max
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pf max. CMOS transient protected
Inhibit ($\overline{INH}$)		Logic 0 inhibits; Data stable within 0.3µS
Enable Bits 1 to 6 ($\overline{EM}$)		Logic 0 enables; Data stable within 150 nS
Enable Bits 7 to 12 ($\overline{EL}$)		Logic 1 = High Impedance Data High Z within 100 nS
Outputs		
Parallel Data (1-12)	bits	12, 2 bytes, 8 parallel lines; offset binary , positive logic
Built-In-Test ($\overline{BIT}$)		Logic 0 for BIT condition. ±100 LSBs of error with a filter of 2.5 mS
OR1, OR2		Over Range; enable with $\overline{EM}$
Drive Capability		50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, -0.4 mA at 2.8V min High Z; 10 µA //5 pF max

TABLE 1. DTC-19305 SPECIFICATIONS (continued)		
PARAMETER	**UNIT**	**VALUE**
DYNAMIC CHARACTERISTICS		
Tracking Rate	FRPS	20 min
Bandwidth(Closed Loop)	Hz	47
Ka	$1/s^2$	11k
A	1/sec	105
B	1/sec	56
Settling Time (half scale step)	msec	120 max
POWER SUPPLIES		
Nominal Voltage	V	+5 -5
Voltage Range	±%	5 10
Max Volt. w/o Damage	V	+7 -7
Current	mA	10 typ,15 max
TEMPERATURE RANGE		
Operating		
-30X	°C	0 to +70
-10X	°C	-55 to +125
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in	1.0 x 0.8 x 0.2; 26 pins
Weight	oz	0.66 max

NOTE: % of Reading

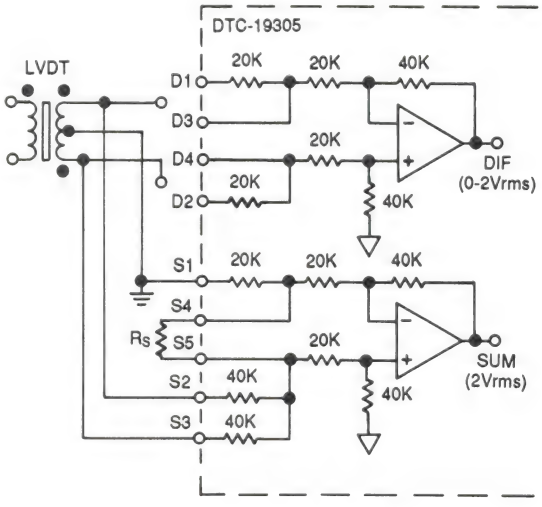


FIGURE 2. 3-WIRE LVDT HOOKUP DIAGRAM

$$\text{Open Loop Transfer Function} = \frac{A^2 (S/B + 1)}{S^2 (S/10B + 1)}$$

TABLE 2. OUTPUT CODING				
LVDT Output	MSB 1			12 LSB
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1LSB	00	1111	1111	1111
+0.5 travel	00	1100	0000	0000
+ 1 LSB	00	1000	0000	0001
null	00	1000	0000	0000
- 1 LSB	00	0111	1111	1111
-0.5 travel	00	0100	0000	0000
-full travel	00	0000	0000	0000
-over full travel	11	xxxx	xxxx	xxxx

TABLE 3. PIN OUT			
PIN#	NAME	PIN#	NAME
1	$\overline{ENM}$	14	E
2	N.C.	15	GND
3	OR 1/7	16	-5V
4	OR 2/8	17	S1
5	1/9	18	S2
6	2/10	19	S3
7	3/11	20	S4
8	4/12	21	S5
9	5	22	D1
10	6	23	D2
11	$\overline{BIT}$	24	D3
12	$\overline{ENL}$	25	D4
13	$\overline{INH}$	26	+5V

Dimensions are in inches (millimeters).

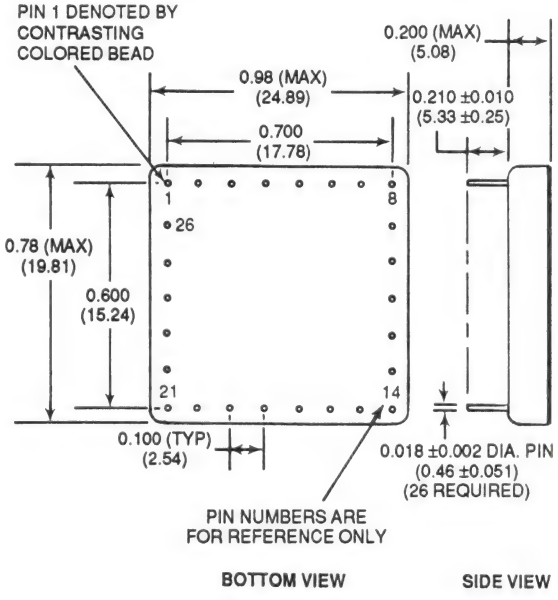


FIGURE 3. DTC-19305 MECHANICAL OUTLINE

ORDERING INFORMATION

DTC-19305-X X X

Accuracy:
1 = 0.15% of reading +3 LSB

Reliability Grade:
0 = Standard DDC procedures.
1 = Fully compliant with MIL-STD 883.
2 = Screened to MIL-STD-883 but without QCI testing.

Temperature Range:
1 = −55°C to +125°C
3 = 0°C to +70°C

SBA SERIES

HIGH POWER SYNCHRO BOOSTER AMPLIFIERS
Also Boosts Output of D/S & D/R Converters

DESCRIPTION

The SBA-Series amplifiers are compact units designed to be bolted to a chassis (see mechanical outline). Both 60 and 400HZ units require signal input levels of 90V synchro or 6.81V resolver. Their signal output is high power 90V L-L synchro. A connection to the signal reference voltage provides the power to drive the amplifier. The only other connections are for logic controls: a Disable input, a BIT output, and +5 V power supply to drive the logic. All signal inputs and outputs are transformer isolated from each other, and logic inputs and outputs are opto-isolated.

The SBA is a high efficiency device. Because power is derived from the reference rather than DC supplies, heat dissipation is reduced by 50% and the unit is smaller in size. Another energy saving feature is the Disable, which allows the output to be turned off when it is not required. The SBA components are mounted on a 1/8 inch thick aluminum plate which conducts heat efficiently to the chassis to which the unit is bolted.

The SBA is fully protected. Current limiting prevents damage from overloads and short circuits. Voltage clamps protect against reference and load transients. A thermal cutout disables the output at 125° C.

In addition to retaining the high efficiency and protection features of previous DDC torque drivers, the SBA has a new feature: a kick circuit. When the rotor in a torque receiver is hung up, the automatic kick circuit in the SBA will shift the synchro output by 120° for 1/2 second to free the hang-up.

APPLICATIONS

SBA amplifiers are rugged units, requiring no calibrations or adjustments, that can be used wherever high power synchro output is required. They can drive large passive loads such as multiple CTs and CDXs, or active loads such as torque receivers. The SBA can be used to amplify the output of a synchro transmitter directly, but its most common useage is for D/S conversion. Only two modules are required for high power D/S conversion: a standard, low power hybrid or discrete D/S or D/R converter, and the SBA.

High power synchro drive capability is often required in training simulators, remote indicators, gun fire control, and Navy retransmission systems. The DISABLE and BIT control lines are designed for computer supervision. The power conserving features and small size of the SBA amplifiers make them an excellent choice for installations requiring multiple units.

FEATURES

- *MOST COMPACT, EASY TO USE SYSTEM FOR HIGH POWER SYNCHRO OUTPUT*
  - *ONLY ONE MODULE NEEDED TO BOOST SYNCHRO SIGNALS.*
  - *POWERED FROM REFERENCE ±15V POWER SUPPLIES NOT REQUIRED.*
  - *PROVIDES HIGH POWER D/C CONVERSION WHEN USED WITH LOW POWER D/S OR D/R CONVERTER.*
- *90V, 60 OR 400 Hz SYNCHRO OUTPUTS:*
  - *DRIVES MULTIPLE CT AND CDX LOADS UP TO 25VA.*
  - *DRIVES TORQUE RECEIVER LOADS UP TO Zss = 6Ω.*
- *KICK CIRCUIT FREES TORQUE RECEIVER ROTOR TO PREVENT HANGUPS.*
- *VERY HIGH EFFICIENCY:*
  - *DERIVING POWER FROM REFERENCE REDUCES HEAT DISSIPATION BY 50%.*
- *VIRTUALLY INDESTRUCTIBLE:*
  - *PROTECTED AGAINST SHORT CIRCUITS, OVERLOADING, TRANSIENTS, TEMPERATURE, AND REFERENCE SUPPLY SHUT DOWN.*

SPECIFICATIONS

Apply over temperature range, ± 10% reference voltage and frequency variation, and ± 10% harmonic distortion in the reference.

PARAMETER	VALUE
ACCURACY	
Passive Loads (CT and CDX)	±3.0 arc-minutes
Active Loads (torque receiver)	± 10 arc-minutes
SIGNAL INPUT	
Input Isolation	Transformer Isolation, 500V rms min. breakdown to ground
Synchro Input	Frequency / L-L Voltage / Impedance
SBA-25001	400 Hz ± 10% / 90V / 400 KΩ min, balanced
SBA-25003	60 Hz ± 5% / 90V / 100 KΩ min, balanced
Resolver Input	
SBA-25002	400 Hz ± 10% / 6.81V / 4 KΩ min, balanced
SBA-25004	60 Hz ± 5% / 6.81V / 4 KΩ min, balanced
	Other frequencies line-to-line voltages and output power levels are available. Please consult factory.
SYNCHRO OUTPUT	
L-L Voltage for Nominal Input Voltage	90V ±1%
Minimum Load Impedance of Passive Loads	Z_{so} = 243Ω
Minimum Load Impedance of Active Loads	Z_{ss} = 6Ω
CONTROL LINES	
Disable (DIS)	TTL compatible Logic 0 enables power amplifier output if internal temperature does not exceed 125°C Loading is 2.5mA max. at logic 0 Opto-isolated, 1000V peak min. breakdown to ground.
Overload Indicator (BIT)	TTL compatible Logic 1 indicates that normal output is not being provided for either of two reasons. 1. A thermal overload prevents the disable from turning the output on. 2. A current overload condition exists and output is reduced by internal current limiting. Drive capability is 2 Std. TTL loads Opto-isolated, 1000V peak min. breakdown to ground.
Kick Circuit (K and CO)	Jumper connection in mating connector. Normally connected for torque receiver loads (not for passive CT and CDX loads). Shifts output by 120° for 1/2 sec. to unjam rotor if output is hung up by an overcurrent condition. Repeat every 4-1/2 seconds so long as overcurrent condition persists. Cannot cause damage to SBA or to torque receiver.
POWER SUPPLIES	
Reference Input (Must Be Same As Signal Reference)	
Reference Signal Isolation	Transformer isolated, 500V rms min. breakdown to ground.
Frequency:	400 Hz / 60 Hz
Nominal Value	400 Hz / 60 Hz
Range	360-440 Hz / 57-63 Hz
Voltage:	
Nominal Value	115V rms
Range	± 10%
Max. Value Without Damage	130V rms
Current:	
No-load	50 mA max / 100 mA max
Additional With Load	1 mA per mA of output load
Logic Voltage Supply (+5V)	
Voltage Level	+ 5V DC ±10%
Max. Voltage Without Damage	+ 10V
Current	10 mA max.
THERMAL CHARACTERISTICS	
Temperature Ranges: (Case Temperature)	
Operating	−25°C to +85°C
Storage	−55°C to +125°C
Heat to be Dissipated	1.5 Watts max. per VA delivered
Thermal Resistance at Junction of Power Transistor to Heat Sink	1.5°C/Watt, conduction cooling
Thermal Cutoff	Amplifier output is disabled whenever internal temperature exceeds 125°C.
PHYSICAL CHARACTERISTICS	400 Hz / 60 Hz
Size (Bolts to Chassis)	7.4 x 5.1 x 1.8 inches (188 x 130 x 46 mm) / 7.4 x 5.1 x 2.6 inches (188 x 130 x 66 mm)
Weight	4 lb (1.82 Kg) max / 7 lb (3.1 Kg) max

TECHNICAL INFORMATION

Figure 1 shows that the SBA consists of three main parts: a power amplifier with a transformer isolated signal input, an internal power supply which is transformer isolated from the reference power source, and digital controls with opto-isolation.

SIGNAL INPUT

90V L-L synchro input passes through an isolation transformer. 6.81V L-L resolver input passes through a Scott-T transformer which changes it to S1, S2, S3, synchro format as well as providing signal isolation. If frequencies or voltage levels, other than those specified are required, please consult the factory.

POWER AMPLIFIER

The triple power amplifier accepts synchro input and produces high power, 90V L-L synchro output. The output is current limited with a sharp limit transition at 1.0A peak. The current limiting prevents damage from output overloads or short circuits, and voltage clamping prevents damage from load transients.

If the reference input is lost, the amplifier output shuts down. In a shut down condition, the SBA presents a safe, open circuit configuration to the load.

The amplifier is thermally protected by a cutout which disables the output when the internal temperature reaches 125°C. The output is automatically restored when the temperature drops below 125°C.

The kick circuit in the amplifier is described in a separate section.

POWER SUPPLY

The high efficiency, low heat dissipation characteristics of the SBA are made possible by the pulsating power supply. This supply produces two unfiltered, full-wave rectified positive and negative voltages as shown in the diagram. These voltages are always in phase with the amplifier output voltage because the power is derived from the reference input. The amplitude of the two voltages need only be a few volts greater than the power amplifier output voltage, since both will change together if the reference level changes. As indicated in Figure 2, the positive and negative pulsating power supply voltage levels will be consistently lower than the constant DC levels of any DC supplies. Because the voltage levels are lower, the power consumed will be much less. The power dissipated as heat is equal to the amplifier current times the difference in voltage between the power supply and the output. For the SBA, the power dissipated is reduced by approximately 50% for reactive loads.

DIGITAL CONTROLS

Two logic lines emerge from the power amplifier, one indicating whether a current overload condition exists (current overload indicator) and one indicating when the internal temperature exceeds 125°C (thermal overload indicator). Logic 1 signifies overload. The Overload Indicator (BIT) will be at logic 1 when either or both of the indicator lines are at logic 1. To prevent nuisance signals in the BIT, the current overload logic line has a 4 second delay before responding to an actual overload condition.

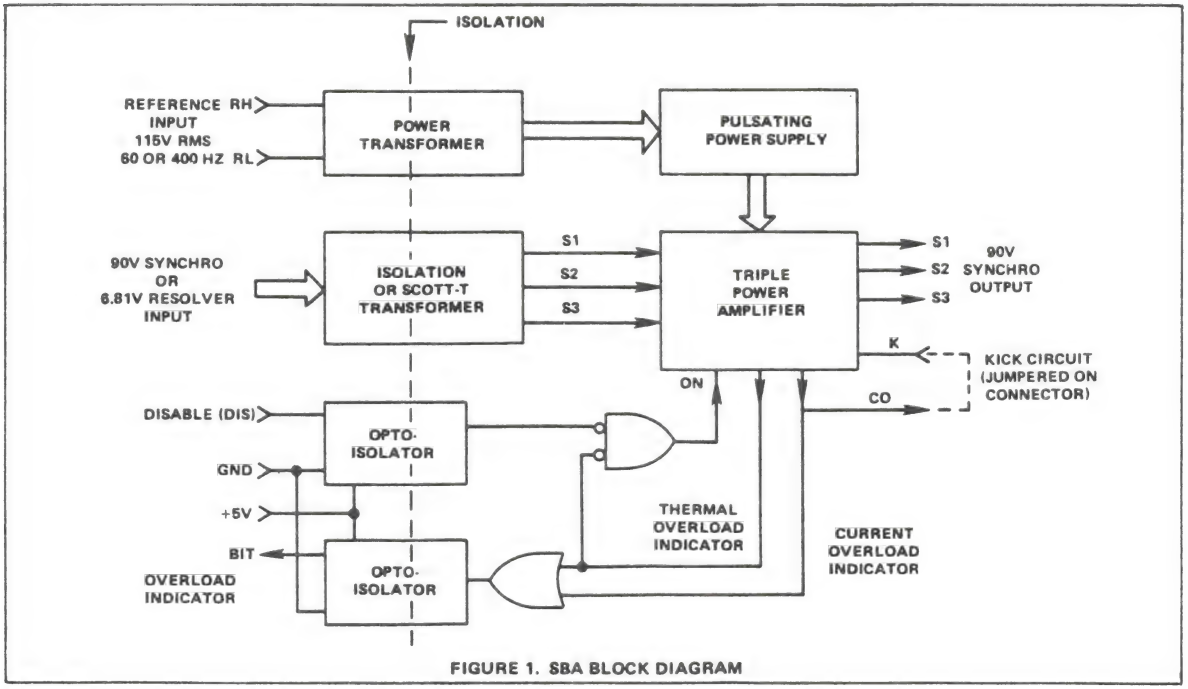


FIGURE 1. SBA BLOCK DIAGRAM

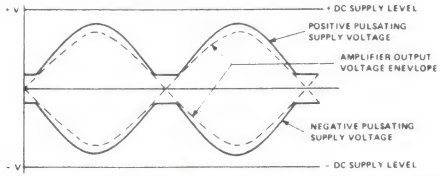


FIGURE 2. PULSATING POWER SUPPLY VOLTAGE WAVEFORMS

The Disable (DIS) makes it possible to switch the power amplifier output on or off. The reference input current drain, as indicated in the specifications, is much smaller if the output is off. If several SBA amplifiers are connected to the same reference, their disable lines can be used to sequence the SBA turn on. This reduces the transient reference power requirement because torque receivers generally draw the maximum limiting current at turn on when the rotors are off null.

The Disable can turn the output on only if two conditions are satisfied. One condition, indicated by the AND gate in the block diagram, is that no thermal overload exists (temperature above 125°C). The other condition is that the reference input must be supplied, since the output shuts down if the amplifier loses power.

KICK CIRCUIT

A hang-up condition can occur in a torque receiver in which the rotor is not driven back to null but stalls at some other angle. The function of the kick circuit in the SBA is to free the hang-up so that the rotor can return to null.

The kick circuit frees rotor hang-ups by shifting the synchro output angle by 120° for a period of 1/2 second. As shown in the block diagram, the kick circuit is activated by connecting the kick input K to the current overload indicator logic line CO. Because the driving current supplied by the SBA is limited to 1 ampere, a current overload condition will usually exist except around null. Such current overloading, if it persists longer than the 4 second delay in the CO response time, will drive the CO line to logic 1, and activate the kick circuit.

Usually one kick is enough to free a rotor hang-up. However, the kick circuit will repeat its 1/2 second, 120° angle shift every 4.5 seconds so long as the current overload condition persists. Repeated cycling cannot harm the torque receiver or the SBA.

The output currents in the SBA are limited to 1A. Without the kick circuit, larger drive currents would be required to reduce the probability of rotor hang-ups. A kick circuit is therefore an important asset in reducing the size and cost of a torque driver.

The kick circuit pin K should be left unconnected for passive loads such as CTs and CDXs.

DRIVING CT AND CDX LOADS

When driving CT and CDX loads the SBA must have enough steady state power capability to drive the Z_{so} of the load. Z_{so} (stator impedance with rotor open-circuited) is measured as shown in the Figure 3:

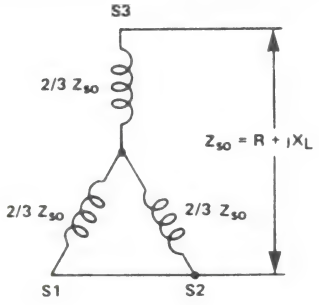


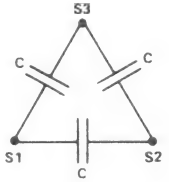
FIGURE 3. Z_{so} MEASUREMENT

The SBA can drive CT and CDX loads whose Z_{so} has a magnitude $(R^2 + X_L^2)^{1/2}$ which is at least as great as the minimum load impedance of $Z_{so} = 243\Omega$ listed in the specifications table. The following table shows the load impedance of some typical control transformers and control differential transmitters.

SOME COMMON CT AND CDX LOAD IMPEDANCES

Military Type Number	Size	Z_{so} (Nominal)
CONTROL TRANSFORMERS:		
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1420 + j13260
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980
CONTROL DIFFERENTIAL TRANSMITTERS:		
11CDX4b	11	253 + j1802
15CDX4d	15	140 + j1000
15CDX6c	15	404 + j2290
18CDX4c	18	63 + j 695
18CDX6d	18	521 + j1605
23CDX4c	23	32 + j 306
23CDX6c	23	221 + j 958

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Figure 4 illustrates three capacitors placed across the legs of the synchro stator in a delta configuration:



DELTA TUNING CONFIGURATION

FIGURE 4. CT LOAD TUNING

The correct value of the capacitance C in Farads is given by:

$$C = \frac{X_L}{4\pi f\,(R^2 + X_L^2)}$$

where f is the carrier frequency and R and X are the series real and reactive components of Z_{so}. Good grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel, because the load impedance Z is increased to:

$$Z = \frac{R^2 + X_L^2}{R}$$

DRIVING TORQUE RECEIVER LOADS

In addition to having enough steady state power capability to maintain a torque receiver at null, a torque driver must have a peak transient power sufficient to drive the torque receiver back to null. This transient power capability is indicated by the maximum torque receiver load capability Z_{ss} which can be driven. For the SBA, the maximum load Z_{ss} is 6Ω.

Some common torque receivers and their load impedances Z_{ss} (stator input impedance with rotor shorted) are listed in the following table:

SOME COMMON TORQUE RECEIVERS AND THEIR LOAD IMPEDANCES

Synchro	V_{L-L}/freq. (Hz)	Z_{ss}(Ω)
11TR4c	90V/400	180 to 250
15TRx4a	90V/400	50 to 82
15TRx6a	90V/60	920
18TRx4a	90V/400	16 to 21
18TRx6b	90V/60	350 to 430
23TR6	90V/60	110 to 145
23TR6a	90V/60	110 to 145
23TRx4a	90V/400	6.5 to 8.1
23TRx6b	90V/60	110 to 145

The SBA-25002 and 25004 Synchro Booster Amplifiers are directly compatible with our MDCR-H or HDSC-14 Digital to Resolver/Synchro Converters. Figure 5 illustrates the connection procedure for this application.

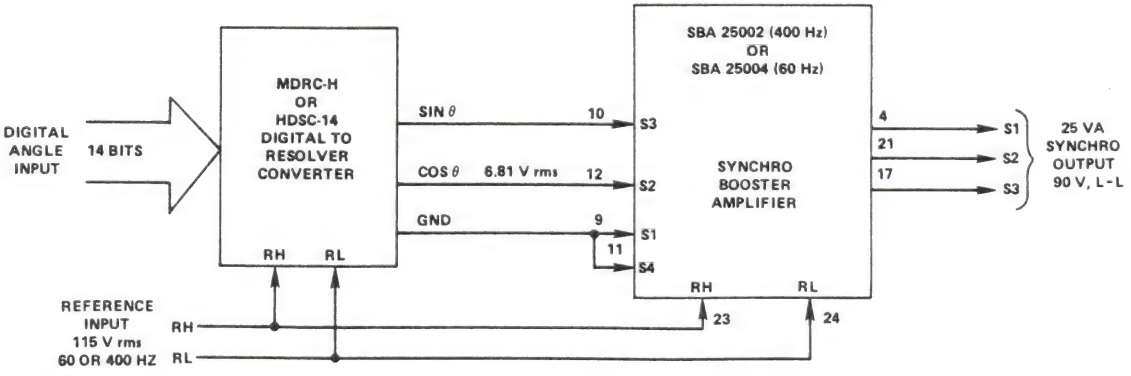
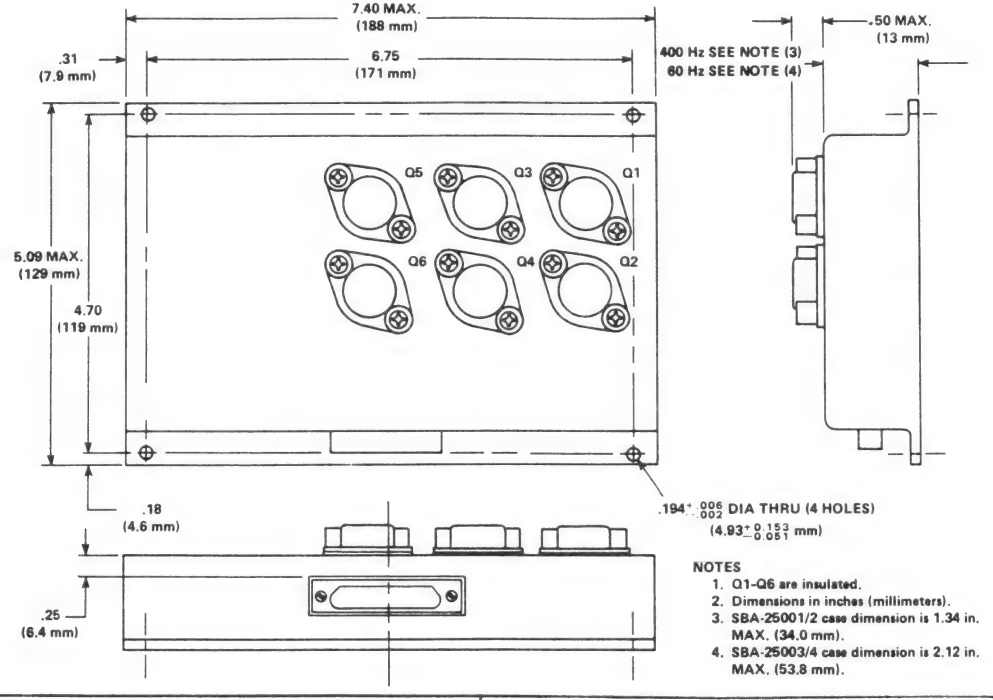


FIGURE 5. MDRC/SBA CONNECTION DIAGRAM

MECHANICAL OUTLINE

Metal case bolts to chassis for heat-sinking.
Mating connector and locking hardware supplied.



NOTES
1. Q1-Q6 are insulated.
2. Dimensions in inches (millimeters).
3. SBA-25001/2 case dimension is 1.34 in. MAX. (34.0 mm).
4. SBA-25003/4 case dimension is 2.12 in. MAX. (53.8 mm).

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	+5V	14	DIS INPUT
2	BIT OUTPUT	15	NC
3	NC	16	GND
4	S1 OUT	17	S3 OUT
5	TP	18	CO
6	K	19	NC
7	TP	20	TP
8	TP	21	S2 OUT
9	S1 IN	22	NC
10	S3 IN	23	RH
11	S4 IN	24	RL
12	S2 IN	25	NC
13	TP		

NOTES:
1. Pin S4 is for resolver input versions only.
2. To enable the kick circuit for torque receivers, connect pin 6 to pin 18.
3. NC means no connection is made to this pin internally.
4. TP are test points intended for factory use only.

ORDERING INFORMATION

SBA-25001

1 = 400 Hz, 90V L-L synchro input
2 = 400 Hz, 6.81V L-L resolver input
3 = 60 Hz, 90V L-L synchro input
4 = 60 Hz, 6.81V L-L resolver input
All units provide 25VA synchro output

NOTE: The following hardware is supplied with each order:
Mating Connector AMP 205207-1
One set Male Retainer Screws AMP 205980-1
15 Sockets AMP 205090-1

C

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SECTION J
MIL-STD-1553 DATA BUS PRODUCTS

PRODUCT SUMMARY TABLE

MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES	PAGE
• *TRANSCEIVERS — Single*				
BUS-8553	Transceiver	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.20"	Featuring low power dissipation and improved filtering to enhance bit error rate of system. Directly interfaces to Harris 15530 Encoder/ Decoder. DESC #5962-86049-05XC Uses BUS-25679 XFMR.	J-87
BUS-63102 II	Universal Transceiver	1.26 x 1.26 x 0.17" Hybrid	Universal transceiver conforms to MIL-STD-1553 A/B and McDonnell Douglas A-3818, A-5232, A-4905, and A-5690. Use BUS-27765 XFMR.	
BUS-63104 II	Transceiver	1.26 x 1.26 x 0.17" Hybrid	Conforms to MIL-STD-1553 A/B. Improved filtering to enhance bit error rate. Use BUS-27765 XFMR.	
BUS-63105II(-15V) **BUS-63107II(-12V)**	Transceiver	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.20"	Monolithic Transceiver.Listed on MIL.DWG.No.5962-86049-02ZC. Conforms to MIL-STD-1553 A/B. High S/N ratio, internal filtering. Drives Harris 15530 directly. SEAFAC tested. Eliminates non-standard part approval when specified by the Military Drawing number. Uses BUS-25679(-15V) and BUS-29854(-12V) XFMR	J-26
BUS-63115 II			Same as BUS-63105 II but has inverted RX and $\overline{RX}$ outputs.	
BUS-63117 II			Same as BUS-63107 II but has inverted RX and $\overline{RX}$ outputs.	
• *TRANSCEIVERS — Dual*				
BUS-63125II(-15V) **BUS-63127II(-12V)**	Dual Transceiver	36 Pin DDIP Hybrid 1.9 x 0.78 x 0.2"	Dual redundant monolithic transceivers in a single hybrid. Conforms to MIL-STD-1553 A/B. High S/N ratio, internal filtering. Drives Harris 15530 directly. Complete isolation, including separate power and signal connections. SEAFAC tested. Eliminates non-standard part approval when specified by the MIL. DWG. No. 5962-87579-02XC. Uses BUS-25679(-15V) and BUS-29854(-12V) XFMR	J-26
BUS-63135 II			Same as BUS-63125 II but has inverted RX and $\overline{RX}$ outputs.	
BUS-63137 II			Same as BUS-63127 II but has inverted RX and $\overline{RX}$ outputs.	
BUS-63147 **BUS-63148**	Dual 5V Transceiver	36 Pin DDIP Hybrid 1.9 x 7.6 x 0.210"	Complete transmitter and receiver pair conforming fully to MIL-STD-1553 A/B. Features +5V power supply, Dual Redundant packaging, and Harris I/O compatibility. BUS-63148 is BUS-65612 compatible. Uses BUS-41429 XFMR.	J-28
• *COMPLETE TERMINALS*				
BUS-61553(-15V) SERIES **BUS-61554(-12V)** **BUS-61555(+5V)**	Advanced Integrated MUX (AIM) Hybrid AIM-HY	2.1 x 1.9 x 0.25" (DDIP)	Complete MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT) device. Contains dual low power MKII transceivers, complete BC/RT/MT protocol logic, MIL-STD-1553-to-host interface unit, and an 8K x 16 shared RAM. Provides memory mapped 1553 interface, on-line and off-line Self Test, and is SEAFAC Tested.Eliminate non-standard part approval when specifiied by the MIL. DWG No. 5962-88692-01XC. Uses BUS-25679(-15V), BUS-29854(-12V), and BUS-41429(5V) XFMR	J-20 J-22
BUS-61556(-15V)		2.2 x 1.6 x 0.17" (Flatpack)	Same as above but it is transceiverless and is used with BUS-63102 II.	
BUS-61563(-15V)			Flatpack version of BUS-61553.	
BUS-61564(-12V)			Flatpack version of BUS-61554.	
BUS-61565(+5V)			Flatpack version of BUS-61555.	
BUS-61559(-15V) **BUS-61560(-12V)** **BUS-61561(+5V)**	Enhanced Advanced Integrated MUX (AIM) Hybrid AIM-HY'ER	2.1 x 1.9 x 0.25" (DDIP)	Complete MIL-STD-1553B Notice 2 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT) device. Supports STANAG 3910 as it directly interfaces to the BUS-63910 high-speed protocol unit. Pin, functional, and software compatible to BUS-61553 Series including data and address buffers selection, Enhanced RT Subaddress Memory Management, and additional interrupts, internal illegalization, and Time Tag.	J-28
BUS-61569(-15V) **BUS-61570(-12V)** **BUS-61571(+5V)**		2.2 x 1.6 x 0.17" (Flatpack)		
BUS-65112 **BUS-65117**	Dual Redundant RT	2..1 x 1.9 x 0.25" (DDIP) 2.2 x 1.6 x 0.17" (Flatpack) Hybrid	MIL-STD-1553 dual redundant RT includes transceivers, encoder/decoder and protocol. Supports 13 mode codes and has DMA type interface handshake. SEAFAC tested. Eliminated non-standard part approval when specified by the Military Drawing number (DESC) 5962-87535-01XC. Uses BUS-25679 XFMR.	J-39
BUS-65142	Dual Redundant RT	1.9 x 2.1 x 0.25" (DDIP)	Complete dual redundant RT package in either DDIP or Flatpack hybrid packages. Includes CMOS-SOS Monolithic RT protocol and BiPolar low power Mark II transceivers, data buffers, timing control logic, supports mode codes, 16MHz decoders that offer improved noise rejection and zero crossing detection, and has SEAFAC tested components. Uses BUS-25679 XFMR.	J-41
BUS-65144		1.6 x 2.2 x 0.17" (Flatpack)		

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

Data Bus Products continued.

PRODUCT SUMMARY TABLE (continued)

MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES	PAGE
• *COMPLETE TERMINALS — continued*				
BUS-65149	Universal multi-protocol Remote Terminal	2.1 x 1.9 x 0.25" (90 Pin DIP)	The BUS-65149 is the world's first dual redundant universal MIL-STD-1553 Remote Terminal (RT) hybrid. The BUS-65149 features a universal sinusoidal transceiver and pin selectable options providing for support of MIL-STD-1553A; MIL-STD-1553B; McAIR A3818, A5232, and A5690; the various G.D. F16 protocols; and GRUMMAN SPG151A. The BUS-65149 provides all of the functions required to interface between a MIL-STD-1553 dual redundant serial data bus and a subsystem parallel three-state data bus. A pair of BUS-27765 transformers are required to interface between the BUS-65149 and the 1553 bus.	J-43
BUS-65153 **BUS-65163**	Complete, dual redundant MIL-STD-1553B Remote Terminal **"STIC"**	1.90 x 1.0 x 0.240" 70-pin DIP ceramic package 70-pin Flatpack	Provides the output voltage level required for MIL-STD-1760. Contains two (2) low power transceivers and a DDC custom designed chip. This chip includes dual encoder/decoder, RT protocol logic, 3-state data buffers, and DMA transfer control logic. Supports all 13 dual redundant mode codes, programmable. Parallel data transfers (8-bit or 16-bit) are accomplished via a DMA type handshake. Programmable 16 or 12MHz clock.	J-45
BUS-65612	Bus Controller, Remote Terminal, or Bus Monitor	1.32 x 1.32 x 0.125" (PGA)	Pin grid array (BUS-65612). Dual redundant CMOS SOS MIL-STD-1553 Bus Controller, Monitor or RT with error detection and complete mode code capability. Includes 16MHz dual encoder/decoder, dual bit processor, RT protocol, BC protocol, and DMA subsystem interface.	J-69
BUS-66312	1750 or STD CPU Memory Mangement Interface	1.32 x 1.32 x 0.125" (PGA)	Interfaces STD or 1750 CPUs (F9450 or PACE 1750A) and 1553 BC/RTs (BUS-65600 and BUS-65612) for minimum CPU overhead; internal microcode controller; buffer controls for 1750 address bus and data bus; registers for command, interrupt, and mode control words.	J-71
• *CARD ASSEMBLIES*				
BUS-65505 (-12V) **BUS-65506 (-15V)**	Unibus Bus Controller, Remote Terminal, or Bus Monitor	15.6 x 8.4" Unibus Hex Card	Dual redundant Bus Controller Remote Terminal Unit, or Bus Monitor with Unibus ® interface. Supports all MIL-STD-1553 message formats, 12 Mode Codes, and provides Built-in-test capability. Its 4K x 16 bit dual access RAM and command registers minimize CPU overhead.	J-47
BUS-65508 (-15V) **BUS-65509 (-12V)**	Multibus I Bus Controller, Remote Terminal, or Bus Monitor	6.75 x 12" Multibus ® Card	Dual redundant Bus Controller, Remote Terminal, or Bus Monitor with Multibus ® interface. Supports all MIL-STD-1553 message formats, 12 Mode Codes, and provides built-in-test capability. Its 4K x 16 bit dual access RAM and command registers minimize CPU overhead.	J-49
BUS-65515	IBM PC ® Bus Controller or Remote Terminal	13.125 x 4.9" IBM PC Card	Dual redundant Bus Controller, Remote Terminal, or Bus Monitor with IBM PC interface. Supports all MIL-STD-1553 message formats, 13 mode codes, and provides built-in-test capability. Its 4K x 16 bit dual access RAM and command registers minimize CPU overhead.	J-51
BUS-65517 II	IBM PC Card for Test and Simulation	13.125 x 4.6" IBM PC Card	Simultaneously simulates a Bus Controller, and active Monitor and up to 31 Remote Terminals. Provides comprehensive Error injection with Bit/Word resolution. Fully dual redundant. Includes user friendly menu driven software.	J-53
BUS-65519	IBM PC Card Mil-Std-1553 RT Production Test Plan protocol Testing Software & Hardware Run time routine library	13.125 x 4.6" IBM PC Card	The BUS-65519 is a turnkey system used to automate the protocol tests of the SAE RT Production Test Plan. A number of military contracts are imposing this test plan on MIL-STD-1553 suppliers.With the BUS-65519, the test engineer characterizes the Unit Under Test (UUT) via the user friendly, menu driven software. Once this is done, the configuration can be saved to disk. The BUS-65519 can execute the ENTIRE protocol tests in under 20 seconds. A report detailing the results of the test is automatically generated.	J-55
BUS-65522 II **BUS-65523 II** **BUS-65524**	VME/VXI Bus Controller, Remote Terminal, or Bus Monitor	9.2 x 6.3 x 0.4" VME Eurocard Ruggedized	Dual redundant Bus Controller, Remote Terminal, or Bus Monitor with VME/VXI interface. Supports all MIL-STD-1553 message formats, mode codes, and provides built-in-test capability. Its 8K x 16 dual access RAM and four types of interrupts minimize CPU overhead. BUS-65523II is McAir option. The BUS-65524 is Ruggedized.	J-57
BUS-65525	VMEbus-to-STANAG 3838 /3910, BC, RT, and MT for Test& Simulation	9.2 x 6.3 x 0.4" VME Eurocard	Complete interface between a VMEbus backplane and a dual redundant STANAG 3838/3910 low-speed/high-speed (LS/HS) bus. Consists of a intelligent VME slave device and an external fiber optic transceiver. Provides capability for operating as a STANAG 3838 (low-speed) BC, RT, or MT. Capability to operate as a 20 Mbps STANAG 3910 (high-speed) RT.	J-59

NOTES: Most hybrid products are available with Military Processing (Contact Factory).
® Unibus is a registered trademark of Digital Equipment Corporation.
® Multibus is a registered trademark of Intel Corporation.
® IBM XT/AT is a registered trademark of International Business Machines.

Data Bus Products continued.

PRODUCT SUMMARY TABLE (continued)

MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES	PAGE
● *CARD ASSEMBLIES — continued*				
BUS-65526	VMEbus-to-MIL-STD-1553B, BC, RT, and MT for Test& Simulation	9.2 x 6.3 x 0.4" VME Eurocard	Complete interface between a VMEbus backplane and a dual redundant MIL-STD-1553B Notice 2 bus. The board comprises a double height (6.3" X 9.2") intelligent VME slave device, operating in 1553 Bus Controller (BC), Remote Terminal (RT), or Monitor (MT) modes.	J-61
BUS-65529	IBM AT ® BC, RT, MT	6.5 x 4.9" IBM AT half-slot	Dual redundant BC,RT, or MT on a half-slot IBM AT interface card. Supports all MIL-STD-1553 Message formats, 13 mode codes, and built-in-test capability. It's AIM-HY'er features and 4K x 16 shared RAM interface minimizes CPU overhead.	J-63
BUS-65535	VME/VXI BC, Multi RT, MT for Test& Simulation	9.2 x 6.3 x 0.4" VME Eurocard	Simultaneously simulates a Bus Controller, and active Monitor and up to 31 Remote Terminals. Provides comprehensive Error injection with Bit/Word resolution. Fully dual redundant. Includes user friendly menu driven software.	J-65
BUS-65555	MIL-STD-1553 RT/BC/MT interface unit for GRiD © laptop	GRiD internal battery cartridge 2.9 x 1.45 x 5.5" Module	Full, intelligent interfacing between MIL-STD-1553B Data Bus and the rugged GRiD 1520,1530, and 1535 series laptop XT/AT ® compatible computers. Software controls operation as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT). It offers the dual 1553 ports through standard 1553 triaxial connectors. Validated by SEAFAC.	J-67
● *TERMINAL BIT PROCESSORS and DUMB RTs*				
BUS-64100II	Bit Processor	1.15 x 2.15 x 0.2" Hybrid	LSI based Manchester II encoder/decoder. Wrap-around self-test, 16 bit parallel tri-state output, mode codes, address recognition, time out.	J-36
BUS-65101II(-12V) **BUS-65102II(-15V)** **BUS-65201II(Univ)**	Dumb RT (1553 and MACAIR)	1.8 x 1.6 x 0.2" Hybrid	MIL-STD-1553 dumb RT with transceiver, encoder/decoder, control logic dual rank I/O registers, and internal clock oscillator. Provides all interface functions between the Data Bus and a subsystem parallel data highway. May operate as an RT, BC, or Bus Monitor, in either single or dual redundant configurations. SEAFAC tested.	J-37
● *TESTERS*				
BUS-68005	Data Bus Exerciser	17 x 14.5 x 3.5" Instrument	Full function simulation of RTU and BC operation; implements protocol test of SAE AE-9 (see BUS-69005) proposed production test plan; has 1553 A/B System Tests; Real-Time Monitor output; programmable transmitter output level and channel A/B selection; can do superceding command test; error generation/detection; RS-232 and GPIB-488 external control.	J-75
BUS-68010	Data Bus Tester	8.5 x 3.5 x 9.3" Instrument	Low cost, bench top error generating and detecting instrument for functional testing of MIL-STD-1553 Data Bus systems. Operational as Bus Controller, Remote Terminal, and Bus Monitor.	J-77
BUS-68015	Noise Tester	8.25 x 14.5 x 3.5"	Programmable bit error rate tester; self contained Bus Controller and noise source which correlates with SEAFAC; auto self test & diagnostics. Programmable via IEEE 488; pass/fail or continuous run.	J-79
BUS-69005	MIL-STD-1553 Test Software	Flexible Disk	Used with the BUS-68005 Data Bus Tester, BUS-68015 Noise Tester and an IBM PC/XT/AT to perform all protocol tests specified in the SAE AE-9 RT Production Test Plan. Menu-driven complete/partial PTP execution; disk storage of PTP-subset and RT configurations; single, continuous and Halt-on-Error execution. Selectable test data printout.	J-81
BUS-69006	MIL-STD-1553 Test Software	Flexible Disk	Provides a menu-driver ATE environment using an IBM PC/XT/AT host along with two of DDC's BUS-68005 Data Bus Exerciser to perform all protocol tests specified in the SAE RT Production Test.	J-83
BUS-69050	1553 Software Library	Flexible Disk	Consists of a library of run-time routines to perform common MIL-STD-1553 functions. Supports the BUS-61553), BUS-61559, BUS-65515, BUS-65522II, BUS-65529, BUS-65531, and BUS-65555.	J-85
● *SPECIAL TEST EQUIPMENT*				
BUS-8559	Var. Output Transceiver	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.20"	Conforms to MIL-STD-1553 A/B. Has variable output level for use in test applications. Receiver has internal filtering for high S/N ratio. Uses BUS-25679 XFMR.	J-89
BUS-1555	Manchester II decoder	Encapsulated Module 3.1 x 2.6 x 0.8"	Decodes serial Manchester II into 16 bit parallel and NRZ serial data output. Error detection capability.(16MHz clock operation)	J-16
BUS-1556	MIL-STD-1553 Encoder	Encapsulated Module 3.1 x 2.6 x 0.8"	Encodes parallel data into Manchester II. Errors include: Manchester coding, parity, high and low bit count, and sync field.(2MHz clock operation)	J-18

NOTES: Most hybrid products are available with Military Processing (Contact Factory).
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® IBM XT/AT is a registered trademark of International Business Machines.

Data Bus Products continued.

PRODUCT SUMMARY TABLE (continued)

MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES	PAGE
• SEMS				
BUS-67001(UKT) **BUS-67002(UKU)** **BUS-67003(UKS)**	SEM Family	ISEM 2A Format B	Family of SEM modules to configure dumb RT, complete RT, or Bus Controller.	D-3
BUS-67007		Format E	A complete MIL-STD-1553 & 1750A computer I/O, RT/BC/MT mode selectable, with on board shared ram support. L.E.D.'s indicate the board activity and status.	D-3 J-73
• TRANSFORMERS				
BUS-25679 **BUS-27765** **BUS-29854** **BUS-41429** **B-2396**	Bus Isolation Transformers	0.63 x 0.63 x 0.3" Module	Provides all of the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553 A/B. Low profile, modular units that are multitapped to accommodate existing system configurations.	J-14
B-2200/2300 Series*	Interface Transformers (BETA) *see footnote	0.63 x 0.63 x 0.3" or 0.5 x 0.35 x 0.25" Modules	Interface transformers listed on DESC Spec. No. M21038/27. Designed to couple MIL-STD-1553 A/B compatible drivers to the bus. Low profile devices multi-tapped to accommodate existing system configurations. Eliminates non-standard part approval when specified by the Military Drawing number. Listed on QPL-21032-31 from BETA transformers.	J-10
HLP-6000 Series*	Interface Transformers (BETA) *see footnote	0.63 x 0.63 x 0.175" Modules	Provides the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B. These transformers are **hermetically sealed**, **low profile**, modular units that are multi-tapped to accommodate existing system configurations.	J-91
LPB-5000 Series*	Interface Transformers (BETA) *see footnote	0.63 x 0.63 x 0.150" Modules	Provides the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B. These transformers are **low profile**, modular units that are multi-tapped to accommodate existing system configurations.	J-93
• STANAG-3910				
BUS-63910	Dual Redundant Fiber Optic Transceiver	3.35 x 2.76 x 0.71" Metal Cased Module	The BUS-63910 20 MHz fiber optic transceiver provides a complete electrical to optical front end interface to a dual redundant EFA/STANAG 3910 fiber optic bus. The BUS-63910's intended use is to interface between a star-coupled STANAG 3910 bus, a BUS-63920 Data Retiming Unit, and a BUS-63930 STANAG 3910 Remote Terminal Unit. For each redundant channel, the BUS-63910 includes a transmitter, receiver, fiber optic Y-coupler, and optical connector. The BUS-63910 operates at an optical wavelength of 810±40 nm and provdes a minimum optical power output of -4dBm. The receiver provides a minimum sensitivity level of -35dBm and a dynamic operating range of 23dB.	J-30
BUS-63920	Data Retiming Unit	1.38 x 1.18 x 0.33" 22 pin hybrid	The BUS-63920 Data Retiming Unit recovers clock and serial data from the outputs of a dual redundant STANAG-3910 transceiver. It interfaces directly with a BUS-63910 Fiber Optic Transceiver. The BUS-63920 may be used for STANAG 3910 clock recoveryfor both fiber and wire applications. In operation, it extracts 40MHz clock and retimed data from a transceiver's raw serial data output. The BUS-63920 features a fast maximum aquisition time of 1µs, as required for the burst transmission mode of STANAG 3910. Other features include a provision to ensure no clock or data outputs during bus idle periods and an input multiplexer to accommodate dual transceiver outputs.	J-32
BUS-63930	High-speed Remote Terminal Protocol Unit	1.52 x 1.52 x 0.125" 180 pin PGA	The BUS-63930 provides a full implementation of STANAG 3910 RT protocol, including encoder/decoder /FCS logic, mode codes, and error handling. Internal registers are included for control of the 3838/3910 interface, interrupts, time tagging, and self-test. Also provided is a buffered processor to HS shared RAM interface (2M x 16 max), arbitration logic, and a printer-oriented memory mangement structure.The BUS-63930 interfaces between a host processor, a STANAG 3838 Terminal such as DDC's BUS-61559 AIM HY'ER, high-speed message RAM, a data retiming unit (DRU), and a 20 MHz fiber optic transceiver. Packaged in a 180-pin PGA, the BUS-63930 incorporates Frame Logic, Monitor Logic, Arbiter Logic, and Control Logic.	J-34

NOTES: Most hybrid products are available with Military Processing (Contact Factory).
* Order directly from Beta Transformers Technology Corporation
40 Orville Drive Bohemia, NY 11716 (516) 244-7393 FAX: 516-244-8893

Data Bus Products continued.

MIL-STD-1553
BACKGROUND INFORMATION

During the 1950s, military aircraft mission requirements reached such a level of complexity that they could no longer be satisfied with independent and self-sufficient electronics (avionics) subsystems. There was a recognized need for these subsystems to be integrated so they could share information and resources. By the mid 60s, avionics integration had caused a dramatic increase in the complexity of subsystem interfaces and in the size and weight of interconnecting cable bundles. Wiring is now so complex that modification and system testing are difficult and costly. Digital technology offers an obvious solution—time division multiplexing on a serial data bus (see Fig. 1).

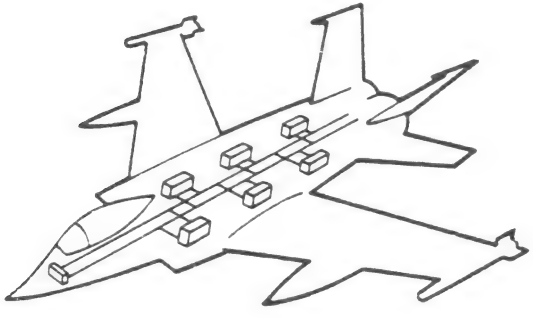

Fig. 1. Point-to-point wiring once used to integrate aircraft avionics, resulted in heavy cables and system complexity (above). The multiplexed data bus now being used to integrate avionics results in simplicity and flexibility.

In 1968, the SAE A2K Committee, with Tri-Service and other industry representation, was formed to generate a military standard for multiplexing. MIL-STD-1553—Military Standard Aircraft Internal Time Division Command/Response Multiplex Data Bus—was issued in 1973. The current revision, MIL-STD-1553B, came out in 1978. A tribute to its success is its widespread application in military programs—and the ready availability of interfacing components. Avionics integration in these applications is flexible, lightweight, and easily tested and modified.

MIL-STD-1553B characterizes all aspects of the data bus network—media, transmission technique, protocol, and terminal interface. The standard provides specifications detailed enough to ensure the interchangeability of equipment from numerous suppliers but flexible enough to allow multiple supplier designs.

TOPOLOGY AND MEDIA

A 1553B data network requires a bus topology that allows all subsystems coupled to the data bus to have access to all transmissions (see Fig. 2). Dual redundant data bus media provide fault tolerance with no single point failure mechanism. Short stub and long stub terminal coupling to the 1553B data bus is transformer-coupled for signal common mode rejection and uses isolation resistors for fault protection (see Fig. 3). Up to 31 terminals can be placed on a 1553B data bus, and each terminal can service up to 30 subsystems.

The data bus travels a shielded twisted pair cable. Its characteristic impedance (70 Ω), attenuation (1.5 dB/100 ft), and capacitance (30 pF/ft) are specified in 1553B along with numerous other parameters. Coupling characteristics are also specified—transformer turns ratio (1:1.4), input impedance (3k Ω), common mode rejection (45 dB), and data bus voltage (1 to 20 V pk-to-pk).

MIL-STD-1553B data bus transmissions are serial time division multiplex messages in pulse code modulation form. Bus traffic is half duplex, hence it travels in one direction at a time over one of the dual redundant cables. Either cable may be used for any message. Coded information samples are transmitted one bit at a time over the data bus.

The 1553B data bus network functions in a command/response sequence. Access to the data bus is provided only when a command is received by a terminal, at which time the terminal may respond—but only with the action the command requests. Central control of media access is the primary operating mode of the 1553B data bus, although a form of distributed control, called dynamic bus control, is possible. Essentially, dynamic bus control allows central control to pass from one terminal to another. Transmissions continue in a command/response fashion, after bus control has passed.

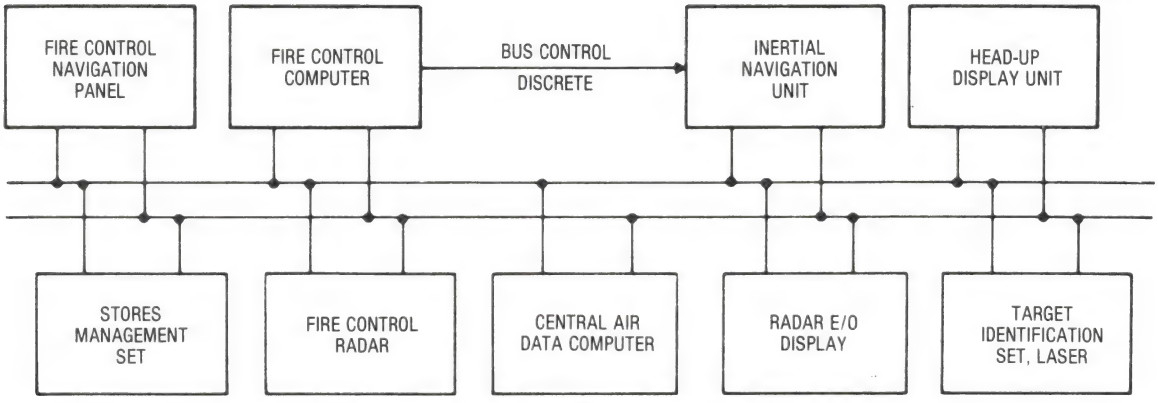

Fig. 2. The MIL-STD-1553B data network requires all data bus subsystems to have access to all transmissions.

TERMINALS

Three types of interfaces between subsystems and the data bus are provided—a bus controller, bus monitor, and remote terminal unit (RTU). A bus controller initiates message transfers on the data bus. A bus monitor receives bus traffic and extracts selected information to be used at a later time. Any terminal not operating as a bus controller or bus monitor is a remote terminal unit.

Terminal interface characteristics detailed in MIL-STD-1553 include limits for input and output voltage levels, input impedance, waveform fidelity, noise parameters, as well as short and long stub coupling conditions.

CODING METHOD

Transmissions on the 1553B data bus are coded in Manchester II biphase level form (see Fig. 4). Manchester coding is self-clocking with a zero crossing during each bit time. Having no DC voltage component, Manchester coding is ideal for the transformer coupling requirement of 1553B. Its noise rejection properties are superior to voltage level coding, since each bit requires a voltage transition. Manchester II biphase level coding also offers good error detection properties.

MIL-STD-1553B specifies a transmission bit rate on the data bus of 1 Mbit per second with a combined accuracy and long-term stability of ±0.1%. The short-term (1-s) stability is specified as ±0.01%.

Each word of a 1553B message requires an initial sync pattern, which is an invalid Manchester waveform 3 bits long. The sync pattern has a voltage transition at 1½-bit times. The phase of this sync pattern determines whether the waveform is a command and status waveform or a data waveform (see Fig. 5). If the first 1½-bit times are positive, it is a command and status type; if the first 1½-bit times are negative, it is a data type. This 3-bit sync pattern provides good noise immunity with a small message overhead.

The last bit of a 1553B word is an odd parity bit. Use of a single parity bit per word is compatible with undetected terminal bit error rate of 10^{-12} bps. Odd parity therefore provides good error detection with a minimum message overhead and is easy to implement.

MIL-STD-1553B requires a 4-μs gap between sequential messages. This intermessage gap time is measured between the mid-bit crossing of the RTU parity bit and the mid-sync crossing of the bus controller command sync (see Fig. 5).

Each bus controller command requires an RTU response of 4 to 12 μs. The RTU response time is measured between the mid-bit crossing of the bus controller parity bit and the mid-sync crossing of the RTU status sync. A terminal must wait 14 μs before considering that a no-response condition exists.

MIL-STD-1553B allows three word formats—command words, data words, and status words. Each consists of a 3-bit sync, 16 bits of data, and a parity bit (see Fig. 6).

Since 1553B uses a central control (command/response) protocol, only the bus controller can transmit a command word. The command word defines the format of the subsequent data bus message and contains the 5-bit address of the receiving or transmitting terminal, a transmit or receive command bit, a 5-bit subaddress/mode field, and a 5-bit word count/mode code field. the subaddress/mode field identifies 30 unique subsystem or memory locations. If the field contains 00000 to 11111, then a terminal management mode command has been received, and the subsequent word count/mode code field is interpreted not as a word count but as a mode code.

The data word's 3-bit sync pattern distinguishes it from command and status words. Following the sync field are a

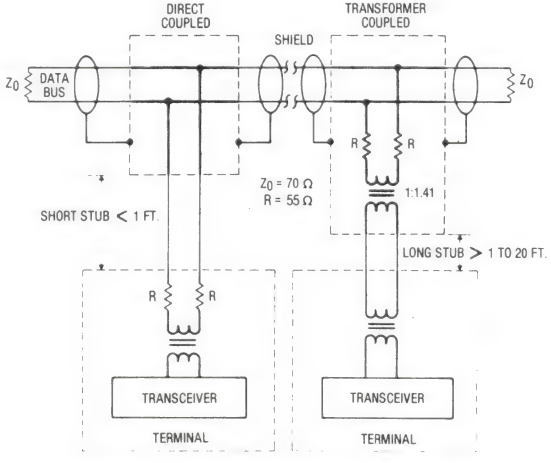

Fig. 3. The 1553B specs for data bus coupling require the data bus to be terminated at both ends, and the terminals to be transformer-coupled to the bus through isolation resistors.

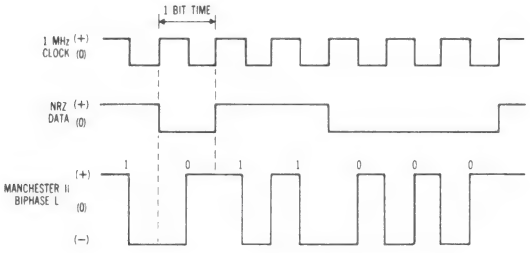

Fig. 4. Manchester II encoding provides the noise immunity benefits of a self-clocking code, with zero transitions during each bit time, and is ideal for transformer coupling.

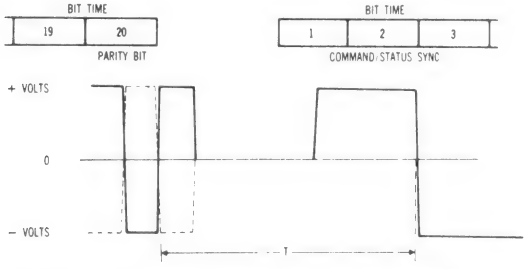

Fig. 5. The bus controller must provide a 4-us min gap between messages, and the remote terminal status response must be 4 to 12 μs.

16-bit data field and 1 parity bit. There are no restrictions on the data field, except that the most significant bit must be transmitted first.

A terminal transmits the status word acknowledgement during each message, except a broadcast message. The word acknowledgement contains a 3-bit sync field, the 5-bit address of the transmitting terminal, and numerous status bits. Remote terminal status is conveyed with message error, instrumentation, broadcast received, and terminal flag bits. Subsystem status is conveyed with service request, busy subsystem flag, and dynamic bus control acceptance flag bits.

MESSAGE FORMATS

MIL-STD-1553B provides for three categories of message formats—message transfers between two terminals, mode commands for terminal management, and broadcasts to all remote terminals. Figure 7 illustrates 5 of the 10 possible message formats. Each message may contain as many as 32 data words.

In bus-controller-to-remote-terminal transfers, the bus controller transmits the receive command and data words contiguously (no gap). After the elapsed response time, the remote terminal acknowledges the status word. Before the next command can be executed, there must be an intermessage gap.

In remote-terminal-to-bus-controller transfers, the bus controller sends the transmit command. After the elapsed response time, the remote terminal transmits the status word and data words contiguously.

Receive and transmit mode commands may contain up to one data word. Broadcast commands require all remote terminals to receive the message. The data may originate from the bus controller or any remote terminal.

MIL-STD-1553B specifies that the transfer of data bus messages be transparent to the user subsystem. Management of data bus traffic is the responsibility of the bus controller and remote terminals. Mode commands are used by the bus controller as a tool for data bus management and may contain any of the 15 assigned mode codes (see Table on page 316). Mode codes are divided into data-word and no-data-word categories.

A number of mode codes are assigned for terminal testing and error recovery routines. If the bus controller receives a status word response with the message error bit set, it can branch to an error handling sequence. Error handling sequences may contain mode codes such as transmit status word, transmit last command, initiate self-test, transmit bit word, or shut down transmitter. If the fault condition has been eliminated, normal message transfers resume.

TERMINAL OPERATION

Each type of terminal provides an interface between the serial data bus and the subsystem. Terminal operation can be partitioned into functional blocks of transceiver, encoder/decoder, protocol, and subsystem interface (see Fig. 8).

The transceiver contains the analog transmitter and receiver functions required to interface directly to the data bus, and the receiver portion contains the signal limiting, filtering, and threshold detection circuits that meet the data bus error rate requirements. The transceiver receives an analog signal from the transformer and outputs a serial digital Manchester coded signal to the decoder. The transmitter portion contains the circuits required to drive the data bus load with a trapezoidal waveform, as well as a timer to prevent "chattering" on the data bus.

The digital encoder and decoder functions required to translate messages to and from Manchester II format reside in the encoder/decoder. The decoder also provides word error checking on each 20-bit word received. It must flag invalid conditions of sync, Manchester coding, bit count, and parity. After the decoder validates the word, it flags the command/status or data word received and outputs the 16-bit digital word. The encoder controls the transmitter and generates the parity bit and command/status or data sync required for the 20-bit word.

The protocol circuits provide the terminal intelligence that manages the data bus transfers. In the receive mode, the circuits decode and validate the received address, then decode and act upon the received command or status word. If the command word is a mode command, the protocol circuit initiates appropriate action. Invalid word count and message errors are flagged in the protocol circuits. In the transmit mode, the protocol circuit formats the message, including status and data words. The circuit also controls the built-in test function and subsystem interface.

The subsystem interface contains the circuits required to transfer messages between the 1553B terminal and the subsystem. Typical functions are buffer storage, interrupt generation, and timing and control of subsystem handshaking.

The MIL-STD-1553B is a mature standard that has been imposed on various military programs. Therefore, numer-

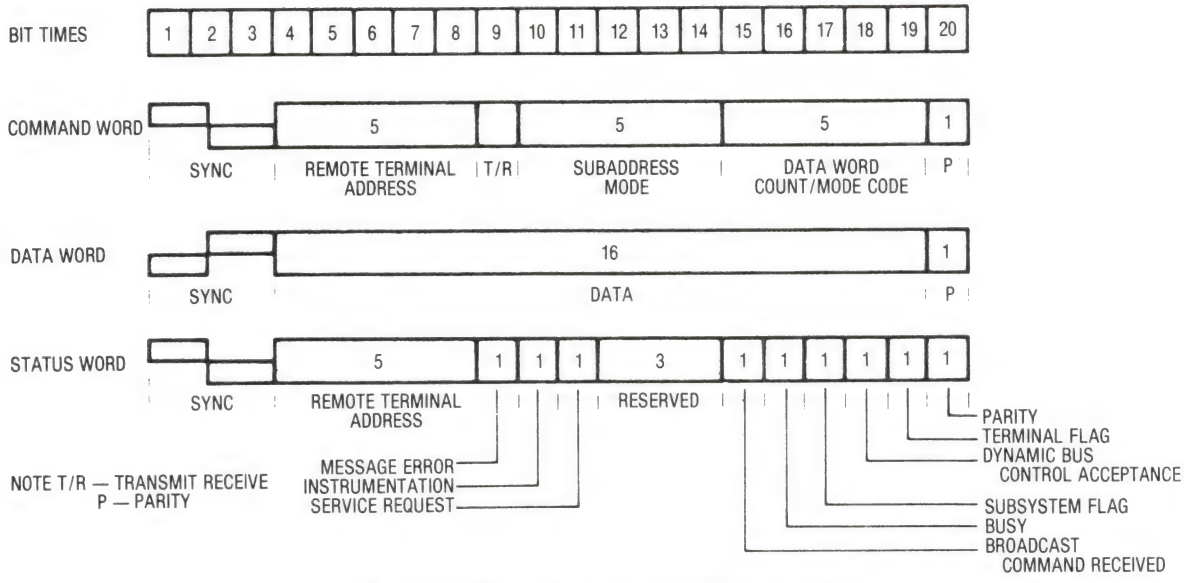

Fig. 6. Word formats allowed by 1553B include command words from bus controllers, status words from remote terminals, and data words from both.

ous suppliers have introduced components that can be used to implement bus controller, RTU, and bus monitor functions. The transceiver, encoder/decoder, protocol, and subsystem interface functional blocks have been implemented with sets of monolithic ICs and hybrid circuits.

Power requirements and circuit complexity have created a need for multiple chip 1553B terminals. The requirement to drive a 100-mA load at 30 V pk-to-pk has made it necessary for bipolar technology to be incorporated into 1553B transceivers. (By comparison, encoder/decoder and protocol circuits have been implemented in low power CMOS ICs. The protocol circuit, due to its complexity, has thus far warranted a separate IC.)

These multiple IC designs are often packaged in a single hybrid circuit—the ILC Data Device remote terminal components, for instance—to meet the small-size requirements of airborne military equipment.

Summarizing, the success of MIL-STD-1553B as a widely used local network standard for the military can be attributed to a number of important factors. First off, Triservice as well as industry participation in creating 1553B resulted in a consensus of requirements. Secondly, detailed specifications for the data bus media and terminal interface resulted in the interchangeability of suppliers' hardware. And last but certainly not least, imposition of the 1553B standard on a number of military programs resulted in multiple suppliers.

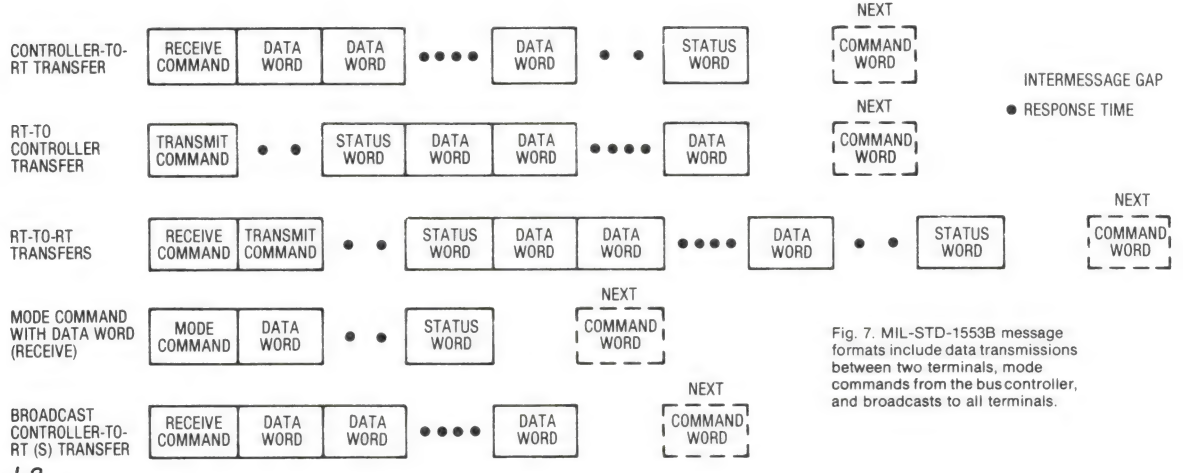

Fig. 7. MIL-STD-1553B message formats include data transmissions between two terminals, mode commands from the bus controller, and broadcasts to all terminals.

Mode Codes for MIL-STD-1553B

Transmit-receive bit	Mode code	Function	Associated data word	Broadcast command allowed
1	00000	Dynamic bus control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit data word	No	No
1	00011	Initiate self-test	No	Yes
1	00100	Transmitter shutdown	No	Yes
1	00101	Override transmitter shutdown	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes
1	00111	Override inhibit terminal flag bit	No	Yes
1	01000	Reset remote terminal	No	Yes
1	01001	Reserved	No	TBD
1	01111	Reserved	No	TBD
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit last command	Yes	No
1	10011	Transmit bit word	Yes	No
0	10100	Selected transmitter shutdown	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
1 or 0	11111	Reserved	Yes	TBD

Note: TBD — to be determined

Assigned mode codes help the terminals manage data bus message traffic.

IEEE-488 DATA BUS STANDARD

INTRODUCTION

In an attempt to standardize instrumentation interfaces, used in Automatic Test Equipment, the Institute of Electrical and Electronic Engineers has advocated the adoption of the IEEE-488-1975 Digital Interface for Programmable Instrumentation.

THEORY OF OPERATION

Generally, the IEEE-488 Standard is described as a method to interface many instruments of various designs and data formats to a single predetermined data bus configuration; thus facilitating instrument hardware compatibility. This is accomplished through 16 hard wire lines and a standard connector. Eight lines are used for handling bi-directional data transmissions. Three handshake control lines handle the required timing of transmissions on the bus. The data transfer rate is mandated by the slowest listener in the system. Five interface management lines handle the remaining functions, such as type and condition of information (command or data) being transferred on the bus.

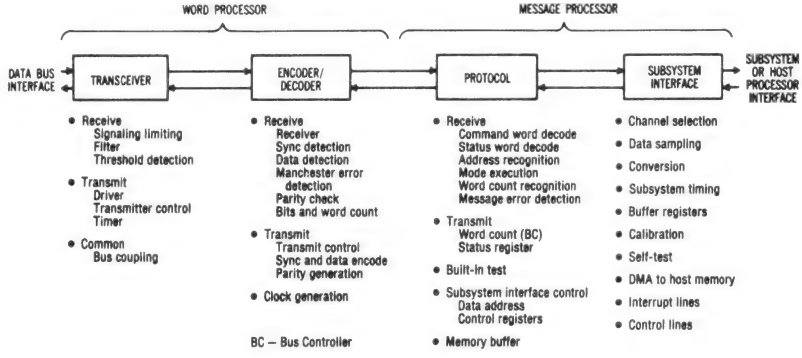

Fig. 8. The terminal functional elements that perform data bus interface, word processing, and message processing are the transceiver, encoder/decoder, protocol, and subsystem interface components.

See page N-19 for a list of Application Notes available from DDC.

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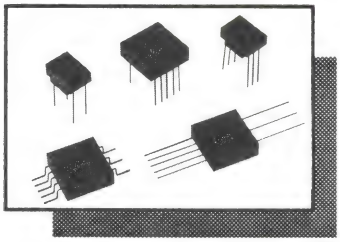


MIL-STD-1553 TRANSFORMERS TO DESC SPECIFICATION NO. 21038/27

DESCRIPTION AND APPLICATIONS

The military data bus specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The B-2200/2300 series of transformers provide the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B compliance.

The step up and down ratios that are available with the B-2200/2300 series complement DDC's entire MIL-STD-1553 product line and are compatible with competitor's drivers, receivers, and transceivers. These transformers are low profile, modular units that are multi-tapped to accommodate existing system configurations. Encapsulated in accordance with MIL-T-21038, their tin coated steel leads conveniently accommodate printed circuit board mounting. Sinusoidal or trapezoidal waveforms are accurately processed, making the B-2200/2300 series of transformers an excellent choice for any MIL-STD-1553A or B application.

FEATURES

- *FULLY QUALIFIED TO DESC SPECIFICATION NO. 21038/27*
- *FOR USE WITH MIL-STD-1553A AND B, MACAIR A-3818, A-5690, A-5232, AND A-4905*
- *LOW PROFILE*
- *-55°C TO +130°C OPERATING TEMPERATURE RANGE*
- *BUILT AND TESTED TO MIL-T-21038 AND MIL-STD-202*
- *LISTED ON QPL-21038-31*
- *QUALIFICATION VALIDATED ANNUALLY*

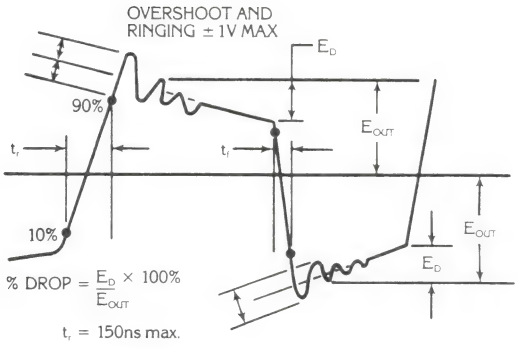


FIGURE 1. WAVEFORM INTEGRITY

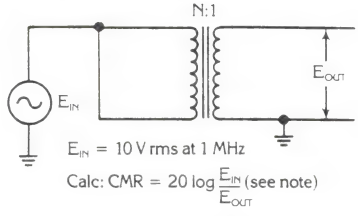


FIGURE 2. CIRCUIT FOR COMMON MODE REJECTION

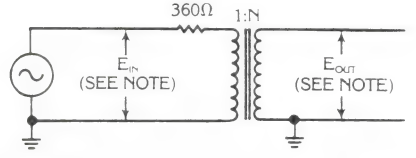
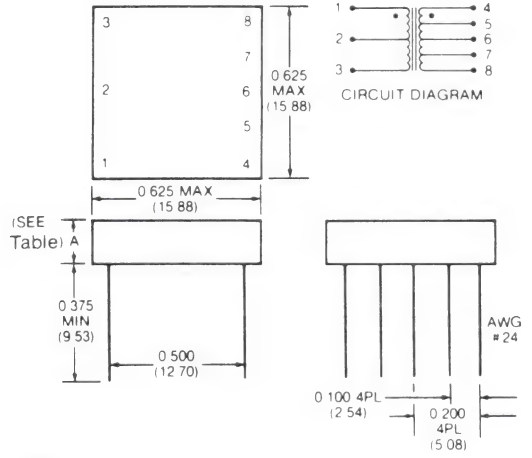

360Ω
1:N
E_{IN}
(SEE NOTE)
E_{OUT}
(SEE NOTE)
E_{IN} = 250 kHz square wave, 27.0 volts peak-to-peak with a rise and fall time no greater than 100 ns.
Calc: Droop = $\frac{E_D}{E_{OUT}} \times 100\%$. (See figure 4 for E_D)

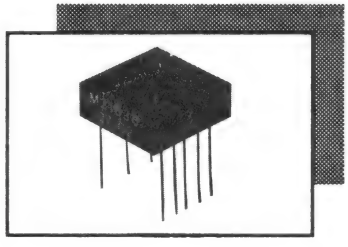
FIGURE 3. CIRCUIT FOR WAVEFORM INTEGRITY

Note: Input to be applied and output to be measured for all dash numbers as shown. N represents highest turn winding in each test.

TABLE 1. B-2200/2300 SERIES SPECIFICATIONS			
PARAMETER	UNIT	VALUE	REMARK
Case			Flame Resistant, DIALLYL PHTHALATE
Terminals			Copper Clad Steel (soft tinned)
Weight	Oz (gm)	0.175(5) max	
Terminal Strength	lbs	2	2 pounds applied force, Method 211, MIL-STD-202, Test condition A
Dielectric Withstanding Voltage	Vrms	100	Method 301, MIL-STD-202
Life (expectancy "X")	Hrs	10,000 min	In accordance with MIL-T-21038
Insulation Resistance	M Ohm	1,000 min	At 250Vdc using method 302, test condition B, MIL-STD-202
Pulse Width (of Output Pulse)	µs	2	Tested using figure 3 with resulting figure 1 waveform.
Overshoot	V	< 1	Tested using figure 3 with resulting figure 1 waveform.
Rise Time (of Output Pulse)	ns	< 150	Tested using figure 3 with resulting figure 1 waveform.
Common Mode Rejection	db	45 min	Tested using figure 2
Operating Temperature Range	°C	-55 to +130	
Droop	%	20 max	Tested using figure 3 with resulting figure 1 waveform.
DC Resistance	Ohm		See respective Electrical Characteristics Table
Input Impedance	Ohm		See respective Electrical Characteristics Table

CONFIGURATION A



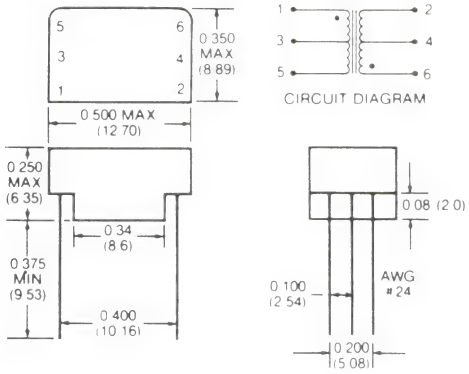


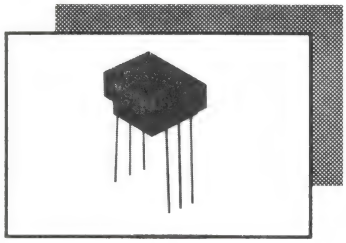
Notes
(1) Dimensions are in inches (mm)
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25 mm)

TABLE 2. ELECTRICAL CHARACTERISTICS – CONFIGURATION A							
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	"A" (max)	DC RESISTANCE Ω(max)	IMPEDANCE Ω (min)
B-2202	M-21038/27-01	1:1 ±3%	1-3	4-8		1-3 3.0	(1-3)
		1:0.707 ±3%	1-3	5-7	0.300	4-8 3.0	4,000
B-2203	M-21038/27-02	1.4:1 ±3%	1-3	4-8		1-3 3.5	(1-3)
		2:1 ±3%	1-3	5-7	0.250	4-8 3.0	7,200
B-2204	M-21038/27-03	1.25:1 ±3%	1-3	4-8		1-3 3.2	(1-3)
		1.66:1 ±3%	1-3	5-7	0.250	4-8 3.0	4,000
B-2205	M-21038/27-04	2.3:1 ±3%	1-3	4-8		1-3 1.2	(5-7)
		3.2:1 ±3%	1-3	5-7	0.300	4-8 3.0	3,000
B-2385	M-21038/27-10	2.12:1 ±3%	4-8	1-3		1-3 1.0	(4-8)
		1.5:1 ±3%	5-7	1-3	0.250	4-8 3.0	4,000

J

CONFIGURATION B

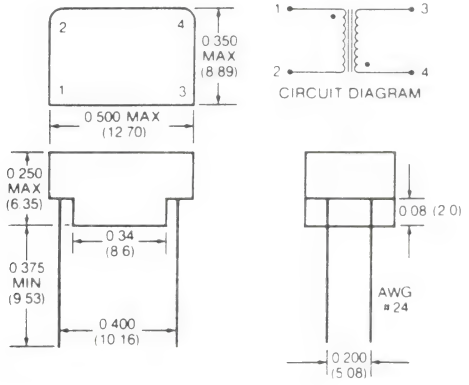


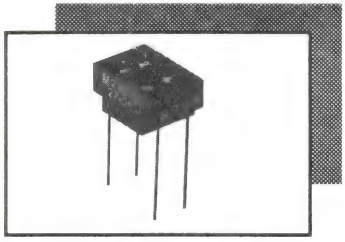


Notes
(1) Dimensions are in inches (mm)
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25 mm

TABLE 3. ELECTRICAL CHARACTERISTICS - CONFIGURATION B						
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω(max)	IMPEDANCE Ω (min)
B-2207	M-21038/27-06	1:1 ±3%	1-5	2-6	1-5 2.5	(1-5)
					2-6 2.8	3,000
B-2208	M-21038/27-07	1:1.41 ±3%	1-5	2-6	1-5 2.2	(2-6)
					2-6 2.7	3,000
B-2209	M-21038/27-08	1:1.66 ±3%	1-5	2-6	1-5 1.5	(2-6)
					2-6 2.4	3,000
B-2210	M-21038/27-09	1:2 ±3%	1-5	2-6	1-5 1.3	(2-6)
					2-6 2.6	3,000

CONFIGURATION C

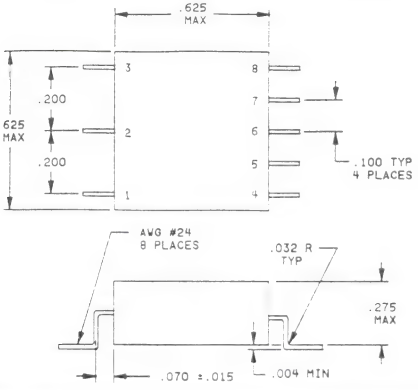


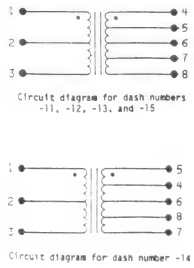


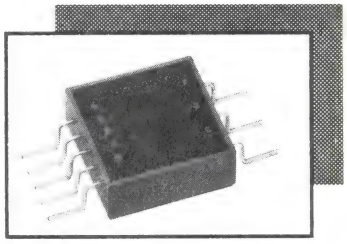
Notes
(1) Dimensions are in inches (mm)
(2) Unless otherwise specified, tolerance is ±0.010 inches (0.25 mm)

TABLE 4. ELECTRICAL CHARACTERISTICS - CONFIGURATION C						
BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω(max)	IMPEDANCE Ω (min)
B-2206	M-21038/27-05	1:1.41 ±3%	1-2	3-4	1-2 2.2	(3-4)
					3-4 2.7	3,000

CONFIGURATION D





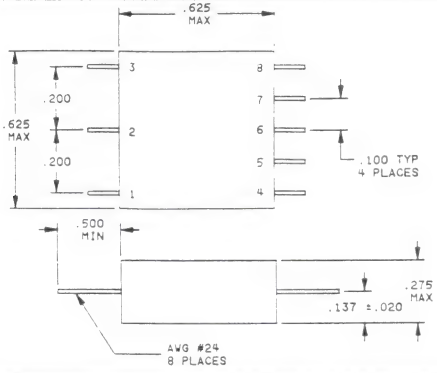


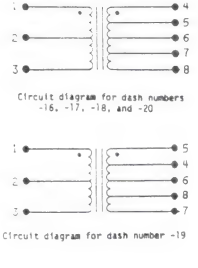
Notes
(1) Dimensions are in inches
(2) Unless otherwise specified, tolerance is ±0.010 inches

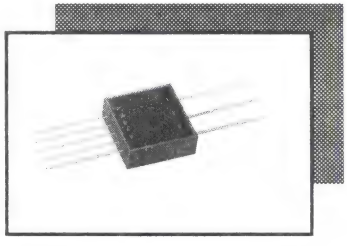
TABLE 5. ELECTRICAL CHARACTERISTICS – CONFIGURATION D

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω(max)	IMPEDANCE Ω (min)
B-2386	M-21038/27-11	1:1 ±3%	1-3	4-8	1-3 3.0	(1-3)
		1:0.707 ±3%	1-3	5-7	4-8 3.0	4,000
B-2387	M-21038/27-12	1.4:1 ±3%	1-3	4-8	1-3 3.5	(1-3)
		2:1 ±3%	1-3	5-7	4-8 3.0	7,200
B-2388	M-21038/27-13	1.25:1 ±3%	1-3	4-8	1-3 3.2	(1-3)
		1.66:1 ±3%	1-3	5-7	4-8 3.0	4,000
B-2389	M-21038/27-14	2.3:1 ±3%	4-8	1-3	1-3 1.2	(5-7)
		3.2:1 ±3%	5-7	1-3	4-8 3.0	3,000
B-2390	M-21038/27-15	2.12:1 ±3%	4-8	1-3	1-3 1.0	(4-8)
		1.5:1 ±3%	5-7	1-3	4-8 3.0	4,000

CONFIGURATION E







Notes
(1) Dimensions are in inches
(2) Unless otherwise specified, tolerance is ±0.010 inches

TABLE 6. ELECTRICAL CHARACTERISTICS – CONFIGURATION E

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω(max)	IMPEDANCE Ω (min)
B-2342	M-21038/27-16	1:1 ±3%	1-3	4-8	1-3 3.0	(1-3)
		1:0.707 ±3%	1-3	5-7	4-8 3.0	4,000
B-2343	M-21038/27-17	1.4:1 ±3%	1-3	4-8	1-3 3.5	(1-3)
		2:1 ±3%	1-3	5-7	4-8 3.0	7,200
B-2344	M-21038/27-18	1.25:1 ±3%	1-3	4-8	1-3 3.2	(1-3)
		1.66:1 ±3%	1-3	5-7	4-8 3.0	4,000
B-2345	M-21038/27-19	2.3:1 ±3%	4-8	1-3	1-3 1.2	(5-7)
		3.2:1 ±3%	5-7	1-3	4-8 3.0	3,000
B-2391	M-21038/27-20	2.12:1 ±3%	4-8	1-3	1-3 1.0	(4-8)
		1.5:1 ±3%	5-7	1-3	4-8 3.0	4,000

A

J

BUS TRANSFORMERS

MIL-STD-1553 DATA BUS ISOLATION TRANSFORMERS

FULL DATA SHEET AVAILABLE

DESCRIPTION AND APPLICATIONS

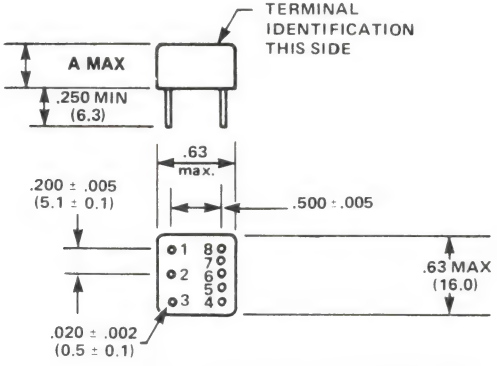
The military Data Bus Specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The BUS-25679, BUS-27765 and BUS-29854 provide all of the turns ratio configurations, component isolation and common mode rejection ratio characteristics necessary for MIL-STD-1553 A and B.

The step up and down ratios, available with these transformers, complement our entire product line and are compatible with competitive drivers, receivers and transceivers (contact the factory for details). The transformers are low profile, modular units that are multi-tapped to accommodate existing system configurations. They are encapsulated in accordance with MIL-T-21038. Their tin coated steel leads conveniently accommodate printed circuit board mounting. They accurately process sinusoidal or trapezoidal waveforms, in accordance with MIL-STD-1553 A and B and McDonnell Douglas specifications A-3818, A-5690, A-5232 and A-4905.

FEATURES

- *MANCHESTER II, BI-PHASE, 1MHz OPERATION*
- *FOR USE WITH MIL-STD-1553 A AND B AND MACAIR SPECIFICATIONS A-3818, A-5690, A-5232 AND A-4905*
- *8 PIN, LOW PROFILE PACKAGE*
- *OPERATING TEMPERATURE: -55° C to +125° C*

MECHANICAL OUTLINE (BUS-25679, BUS-27765 & BUS-29854)



DIMENSION TABLE		
BUS-25679	BUS-27765	BUS-29854
A = 0.275 in. (7mm)	A = 0.300 in. (7.6mm)	A = 0.275 in. (7mm)

Notes
1. Dimensions are maximums unless otherwise noted.
2. All dimensions are in inches (millimeters).
3. Pin callouts on bottom view are for reference only.

TURNS RATIO TABLE				
		TURNS RATIO		
PRIMARY	SECONDARY	BUS-25679	BUS-27765	BUS-29854
1, 3	4, 8	1.4 : 1	1 : 1	1 : 0.83
1, 3	5, 7	2 : 1	1 : .707 (1.4 : 1)	1 : 0.60

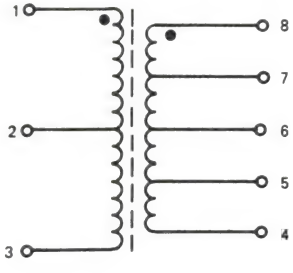


FIGURE 1. TURNS RATIO DIAGRAM

BUS TRANSFORMERS

SPECIFICATIONS

PARAMETER	UNITS	VALUE		
		BUS-25679	BUS-27765	BUS-29854
FREQUENCY RESPONSE				
Operating Range	KHz	250 to 3000	10 to 3000	250 to 3000
Self Resonance	MHz	40 min	40 min	40 min
COMMON MODE REJECTION (CMR)	dB	50 min	45 min	50 min
ELECTRICAL REQUIREMENTS				
Terminals 1, 3 & 4, 8				
Winding Resistance (RDC)	Ω	1.5 max	3 max	1.9 max
Interwinding Capacitance	pF	70 max	30 max	70 max
Winding Inductance				
(LM)	mH	7.5 min	7.5 min	7.5 min
(LL)	uH	6.0 max	6.0 max	6.0 max
PEAK TO PEAK VOLTAGE				
Terminals 1, 3	Vpp	60 max	39.2 max	60 max
PEAK PULSE CURRENTS (AC)				
Terminals 1, 3 (primary)	mA	180 max	140 max	180 max
DROOP				
3 us Pulse Duration				
140Ω Load Across				
Terminals 4-8	%	10 max	10 max	10 max
DECAY TIME				
140Ω Load Across				
Terminals 4-8	ns	25 max	25 max	25 max
BACKSWING				
Across 140Ω Load				
Terminals 4-8		none	none	none
TURNS RATIOS				
Terminals				
1, 3 : 4, 8		1.4 : 1	1 : 1	1 : 0.83
1, 3 : 5, 7		2 : 1	1 : .707	1 : 0.60
2 : 6		CT	CT	CT
Winding Tolerance	± %	5	3	5
TEMPERATURE REQUIREMENTS				
Operating (ambient)	°C	-55 to +125	-55 to +125	-55 to +125
Storage	°C	-55 to +130	-55 to +130	-55 to +130
PHYSICAL CHARACTERISTICS				
Size	in	0.63 x 0.63 x 0.275 (16 x 16 x 7 mm)	0.63 x 0.63 x 0.300 (16 x 16 x7.6 mm)	0.63 x 0.63 x 0.275 (16 x 16 x 7 mm)
Weight	oz	0.1 (3g)	0.1 (3g)	0.1 (3g)

J

TECHNICAL INFORMATION

For the purpose of illustration, pins 1-3 represent the primary winding for each transformer (See Figure 1). In all applications the BUS-25679 may be used for long stub connections as illustrated in Figure 2. The secondary winding is connected to the Data Bus through two fault isolation resistors for direct, or to another transformer for long stub connections as shown. Please note that the transformers connected to the BUS-8553, BUS-8559 and BUS-63105 series transceivers require that their primary center tap winding be grounded.

G-ABR

ORDERING INFORMATION

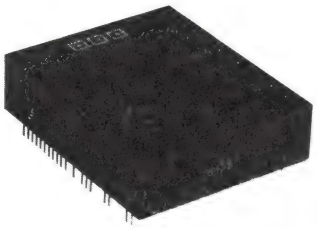
ORDER: BUS-25679, BUS-27765 or BUS-29854

NOTES: 1. Consult Figure 2 for correct unit for application.
2. Consult factory for competitor cross reference information.

Transformers fully qualified to DESC Drawing No. 82030 are available. Consult factory for data sheet B-2200 SERIES.

Specifications are subject to change without notice.

MIL-STD-1553 MANCHESTER II DECODER FOR TEST EQUIPMENT



FULL DATA SHEET AVAILABLE

DESCRIPTION AND APPLICATIONS

Providing enhanced bit error capability and precise message error detection, the BUS-1555 Manchester II Decoder Module avails itself to a wide range of applications. The decoder is encapsulated in a 3.1 x 2.6 x 0.8 inch module and is compatible with receivers designed to meet MIL-STD-1553 A/B, DDC Models BUS-63105 and BUS-8559 are directly compatible with this decoder.

The BUS-1555 will sample Manchester II input data at 16 MHz, which improves bit recognition and overall system capability. Error flags are provided for low and high bit count, odd parity and Manchester II phasing errors. Control logic outputs include Line Active, Frame, Sync Detector, Sync Type and Load Data Pulses. Internal logic may be initialized by means of the Reset Input function (see figure 1). The power supply input range is +4.5V to +5.5V and nominal power dissipation is 2.5 watts. The input is biphase TTL complementary serial data, which is decoded and output as both 16 bit TTL parallel and NRZ serial data.

The BUS-1555 is well suited for use in MIL-STD-1553 test equipment and as a data bus monitor terminal where subsystem listening devices are used. Applications include both ground and on board avionics system.

FEATURES

- *16 MHz CLOCK RATE*
- *ERROR FLAGS FOR SYNC MANCHESTER II ERROR HIGH AND LOW BIT COUNT*
- *CONFORMS TO MIL-STD-1553 A & B*
- *16 BIT PARALLEL AND NRZ SERIAL OUTPUTS*

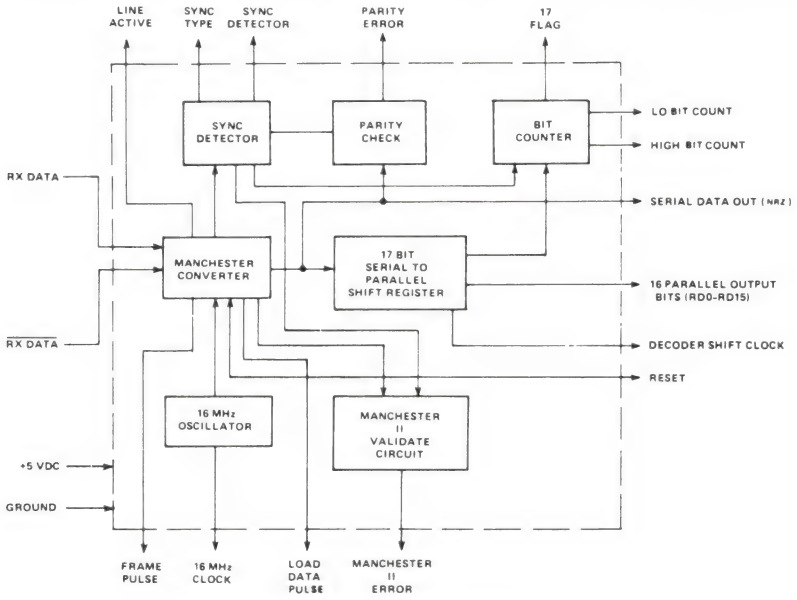


FIGURE 1. BLOCK DIAGRAM

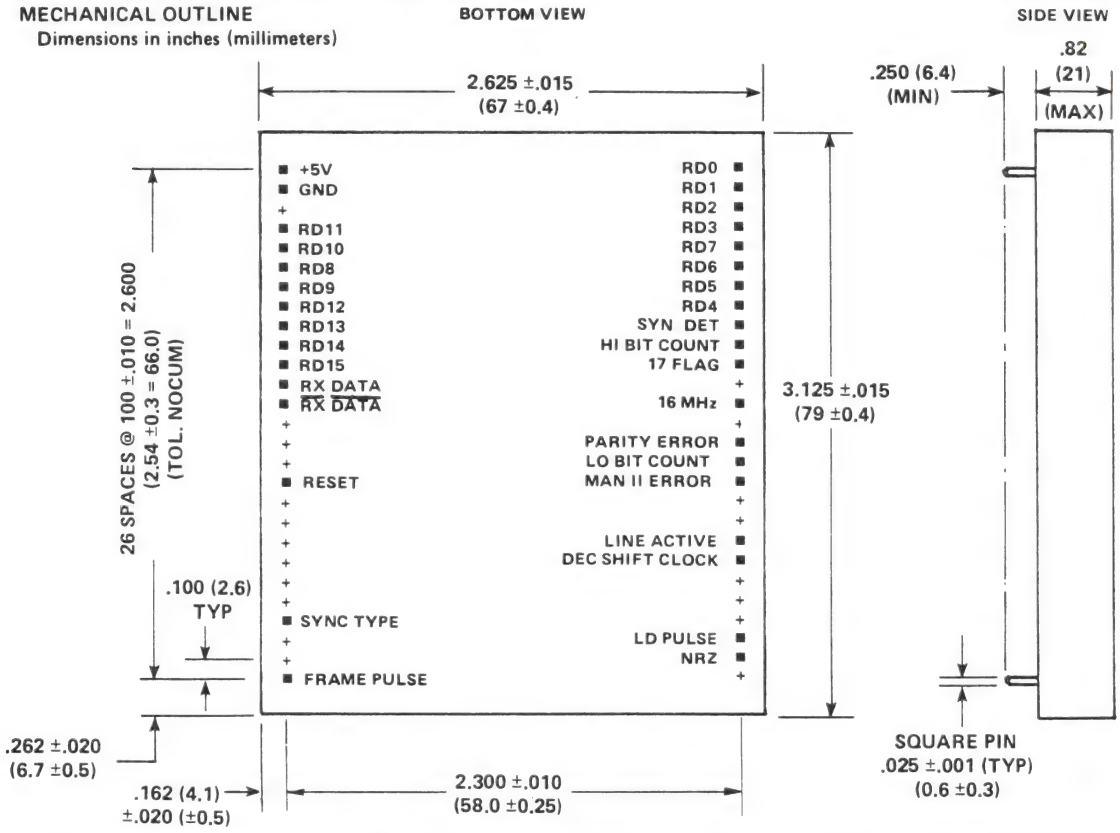
A Manchester error at any bit time takes highest priority. It causes the low bit count error flag to be inhibited, the Manchester error flag to be activated, and a Load Data pulse to appear at the end of the frame.

It is to be noted that the BUS-1555 continues to monitor the input for valid sync after the error checking sequence has begun. As a result of this this, a bit time ending with no Manchester transition present, and 1.5 μsec elapsed since the last Manchester transition, will be interpreted as half of a sync field. Under these conditions the bit counter will not be incremented, and if the second half of the sync field doesn't occur, a low bit count error flag will result. If a bit time ends with no Manchester transition present, and 1.0 μsec elapsed since the last Manchester transition, a Manchester error flag will result.

The valid word indicator is referred to as the 17 flag. This flag is activated when there are 16 data bits plus 1 parity bit valid Manchester transitions. The Parity Error flag is only valid when the 17 flag has been activated.

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



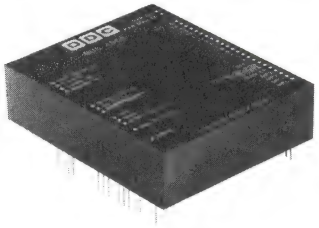
ORDERING INFORMATION

BUS-1555

B-ABR

BUS-1556

MIL-STD-1553 ENCODER Generates Errors For Test Equipment



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-1556 MIL-STD-1553 Encoder is a versatile building block, featuring capability for generating a number of different error types. The Manchester encoder is encapsulated in a 3.1 x 2.6 x 0.8 inch module and is compatible with transmitters designed to meet MIL-STD-1553 A/B. (DDC models BUS-63105 and BUS-8559).

The BUS-1556 converts 16-bit parallel input data to a Manchester II encoded serial output. All timing is derived from an externally supplied 2 MHz clock. The encoder outputs error-free data words or it may be pin programmed to output words containing one or more encoding errors. The errors generated by the BUS-1556 include Manchester II error in any of the 16 data bits, and parity bit positions; parity error, long word (one extra bit) error, short word (one missing bit) error, and two different forms of sync field errors.

A Master Reset pin for initialization, an Encoder Enable input, an Encoder Active and T Load outputs are provided for handshaking with a parallel subsystem. Complementary bi-phase serial data output is provided via the TX DATA and $\overline{\text{TX DATA}}$ pins. The power supply input range is +4.5 V to +5.5 V and nominal power dissipation is 2.5 watts.

APPLICATIONS

The BUS-1556 is intended for use in test fixtures as well as in Automatic Test Equipment (ATE) for testing MIL-STD-1553 A/B monitors, bus controllers and remote terminals. Applications include both ground support and on-board avionics systems.

FEATURES

- *ENCODES PARALLEL DATA INTO SERIAL MANCHESTER*
- *ERROR GENERATION CAPABILITY:*
  - *MANCHESTER CODING ERROR*
  - *PARITY ERROR*
  - *HIGH BIT COUNT ERROR*
  - *LOW BIT COUNT ERROR*
  - *SYNC FIELD ERROR*
- *CONFORMS TO MIL-STD-1553 A AND B*
- *USED IN TEST SYSTEMS WITH BUS-1555 DECODER*

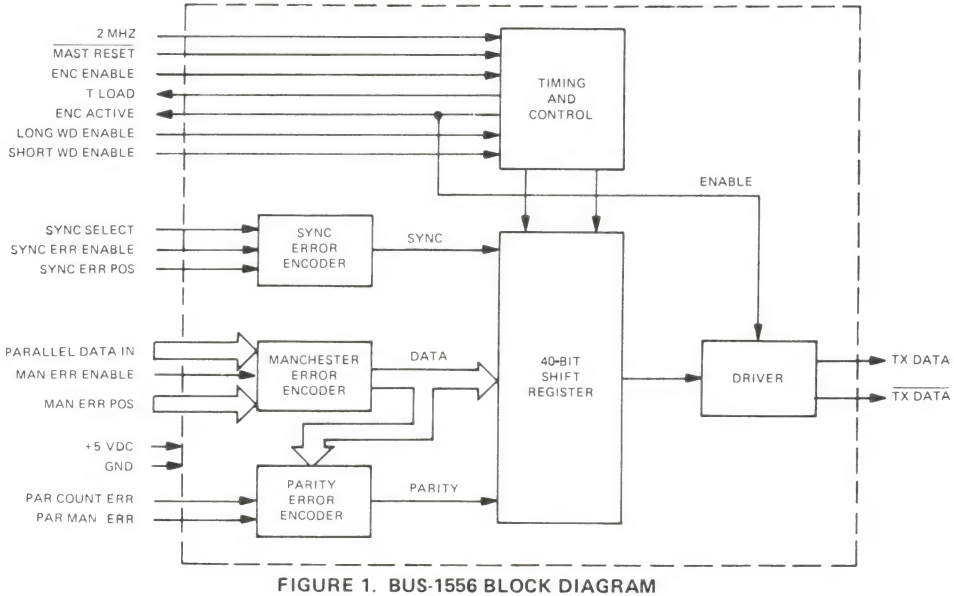


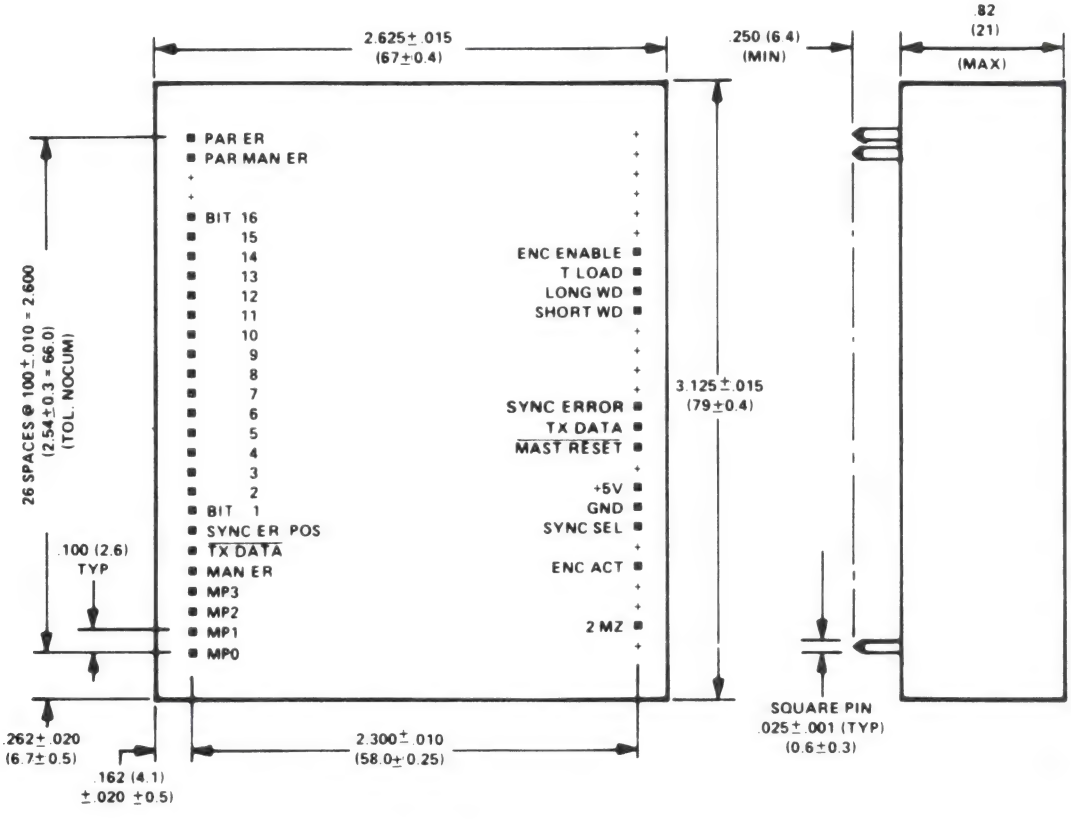
FIGURE 1. BUS-1556 BLOCK DIAGRAM

TEST METHODS

BUS-1556 converter modules are high quality products whose semiconductor components are hermetically sealed. These modules will meet the specific test methods and conditions of MIL-STD-202E shown unless alternative methods are specified by the customer in his procurement documentation.

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



BOTTOM VIEW

ORDERING INFORMATION

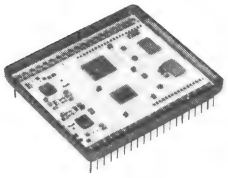
BUS-1556

C-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-61553

MIL-STD-1553 ADVANCED INTEGRATED MUX (AIM) HYBRID



SEE ALSO USER'S GUIDE

FULL DATA SHEET AVAILABLE

DESCRIPTION

DDC's BUS-61553 Advanced Integrated Mux (AIM) Hybrid is a complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT) device. Packaged in a single 78 pin DIP package, the BUS-61553 contains dual low-power transceivers, complete BC/RTU/MT protocol logic, a MIL-STD-1553-to-host interface unit and an 8K x 16 RAM.

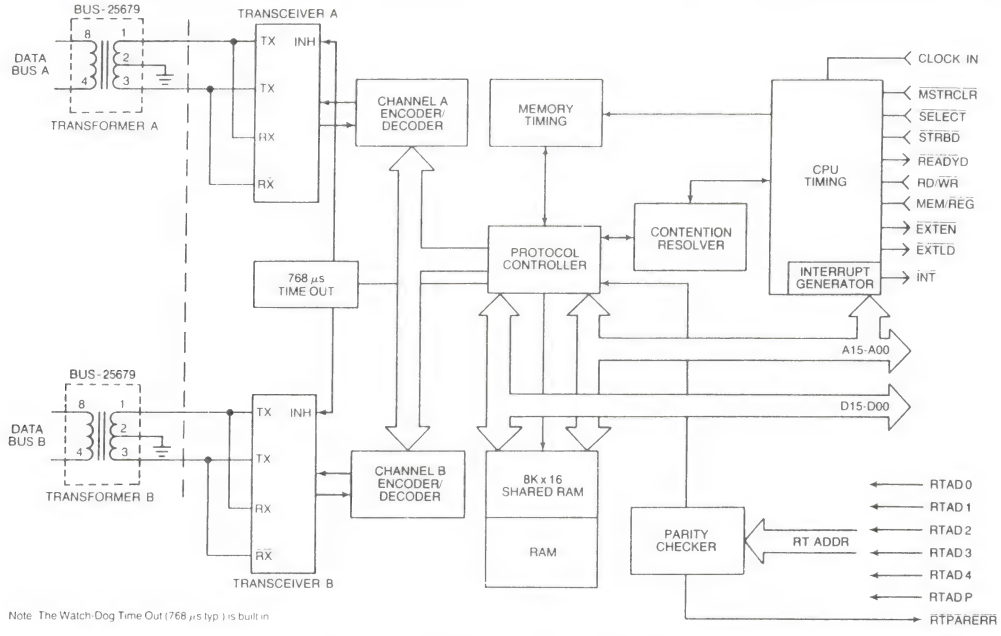
Using an industry standard dual transceiver and standard status and control signals, the BUS-61553 simplifies system integration at both the MIL-STD-1553 and host processor interface levels.

All 1553 operations are controlled through the CPU access to the shared 8K x 16 RAM. To ensure maximum design flexibility, memory control lines are provided for attaching external RAM to the BUS-61553 Address and Data Buses and for disabling internal memory; the total combined memory space can be expanded to 64K x 16. All 1553 transfers are entirely memory-mapped; thus the CPU interface requires minimal hardware and/or software support.

The BUS-61553 operates over the full military −55°C to +125°C temperature range. Available screened to MIL-STD-883, the BUS-61553 is ideal for demanding military and industrial microprocessor to 1553 interface applications.

FEATURES

- *COMPLETE INTEGRATED MUX INCLUDING:*
  - *LOW POWER DUAL TRANSCEIVER*
  - *BC/RTU/MT PROTOCOL*
  - *8K x 16 SHARED RAM*
  - *INTERRUPT LOGIC*
- *COMPATIBLE WITH MIL-STD-1750 AND OTHER STANDARD CPUs*
- *DIP OR FLATPACK HYBRID*
- *MINIMIZES CPU OVERHEAD*
- *PROVIDES MEMORY MAPPED 1553 INTERFACE*
- *ON-LINE & OFF-LINE SELF-TEST*
- *IBM PC® DEVELOPMENT TOOLS AVAILABLE*
- *SEAFAC TESTED*



Note: The Watch-Dog Time Out (768 µs typ.) is built in.

FIGURE 1. BUS-61553 BLOCK DIAGRAM

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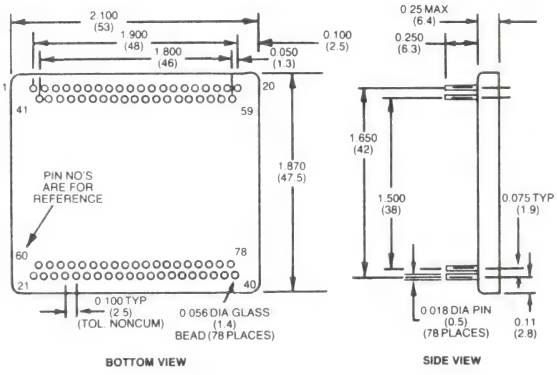
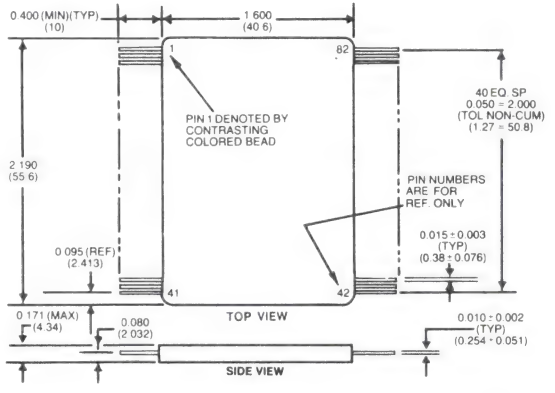
TABLE 8. BUS-61563 FLATPACK PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	NC	42	NC
2	D00	43	TX/RX-A
3	D01	44	$\overline{TX/RX-A}$
4	D02	45	−15VA
5	D03	46	+5V
6	D04	47	GNDA
7	D05	48	$\overline{TAGEN}$
8	D06	49	$\overline{EXTLD}$
9	D07	50	$\overline{READYD}$
10	D08	51	$\overline{RD/WR}$
11	D09	52	$\overline{SELECT}$
12	D10	53	$\overline{EXTEN}$
13	D11	54	$\overline{IOEN}$
14	D12	55	$\overline{STRBD}$
15	D13	56	$\overline{INT}$
16	D14	57	$\overline{MEM/REG}$
17	D15	58	$\overline{MSTRCLR}$
18	RTAD1	59	CLOCK IN
19	RTAD3	60	$\overline{INCMD}$
20	RTAD0	61	$\overline{MEMENA-OUT}$
21	RTAD2	62	$\overline{MEMENA-IN}$
22	RTAD4	63	$\overline{MEMOE}$
23	RTADP	64	$\overline{MEMWR}$
24	$\overline{ILLCMD}$	65	A15
25	SA/MC-2	66	A14
26	SA/MC-0	67	A13
27	SA/MC-4	68	A12
28	LOGIC +5V	69	A11
29	SA/MC-3	70	A10
30	SA/MC-1	71	A09
31	$\overline{THIS-RT}$	72	A08
32	$\overline{BCSTRCV}$	73	A07
33	$\overline{RTPARERR}$	74	A06
34	LMC	75	A05
35	$\overline{T/R}$	76	A04
36	−15VB	77	A03
37	+5VB	78	A02
38	$\overline{GNDB}$	79	A01
39	$\overline{TX/RX-B}$	80	A00
40	TX/RX-B	81	LOGIC GND
41	NC	82	NC



Note: Dimensions are in inches (millimeters).

FIGURE 34. MECHANICAL OUTLINE (DDIP)



Note: Dimensions are in inches (millimeters).

FIGURE 35. MECHANICAL OUTLINE (FLATPACK)

J

ORDERING INFORMATION

BUS-61553-883B

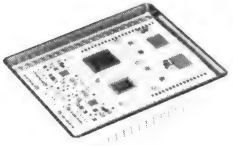
Reliability Grade:
- 883B = Fully compliant with MIL-STD-883.
- B = Screened to MIL-STD-883 but without QCI testing.
- Blank = 0° to 70° C

Power Supply:
- 3 = −15V Transceivers
- 4 = −12V Transceivers
- 5 = +5V Transceivers – Call Factory
- 6 = Transceiverless – use with BUS-63102 II – Call Factory

Packaging:
- 5 = DDIP
- 6 = Flatpack

BUS-61555

MIL-STD-1553 ADVANCED INTEGRATED MUX (AIM) HYBRID



PLEASE REFERENCE BUS-61553 DATA SHEET FOR TIMING SPECIFICATIONS

DESCRIPTION

DDC's BUS-61555 Advanced Integrated Mux (AIM) Hybrid is a complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT) device requiring only a +5 volt power supply. Packaged in a single 78 pin DIP package, the BUS-61555 contains dual low-power transceivers, complete BC/RTU/MT protocol logic, a MIL-STD-1553-to-host interface unit and an 8K x 16 RAM.

Using an industry standard dual transceiver and standard status and control signals, the BUS-61555 simplifies system integration at both the MIL-STD-1553 and host processor interface levels.

The CPU controls all 1553 operations by accessing the shared 8K x 16 RAM. To ensure maximum design flexibility, memory control lines are provided for attaching external RAM to the BUS-61555 Address and Data Buses and for disabling internal memory; the total combined memory space can be expanded to 64K x 16. All 1553 transfers are entirely memory-mapped; thus the CPU interface requires minimal hardware and/or software support.

The BUS-61555 operates over the full military -55°C to +125°C temperature range. Available screened to MIL-STD-883, the BUS-61555 is ideal for demanding military and industrial microprocessor to 1553 interface applications.

FEATURES

- *+5 VOLT ONLY*
- *VERY LOW POWER*
- *COMPLETE INTEGRATED MUX INCLUDING:*
  - *-LOW POWER DUAL TRANSCEIVER*
  - *-BC/RTU/MT PROTOCOL*
  - *-8K x 16 SHARED RAM*
  - *-INTERRUPT LOGIC*
- *COMPATIBLE WITH MIL-STD-1750 AND OTHER STANDARD CPUs*
- *MINIMIZES CPU OVERHEAD*
- *PROVIDES MEMORY MAPPED 1553 INTERFACE*
- *ON-LINE AND OFF-LINE SELF-TEST*
- *IBM PC ® DEVELOPMENT TOOLS AVAILABLE*

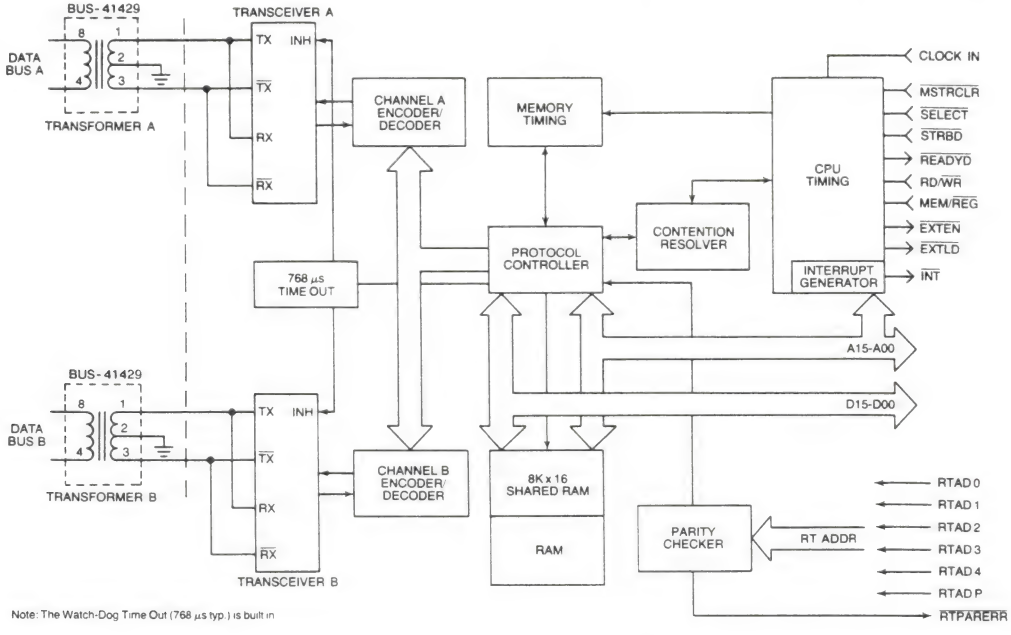


FIGURE 1. BUS-61555 BLOCK DIAGRAM

®IBM PC is a registered trademark of International Business Machines Corporation.

TABLE 1. BUS-61555 SPECIFICATIONS		
Specifications at nominal power supply voltages.		
PARAMETER	**VALUE**	**NOTES**
RECEIVER		
Differential Input Voltage	V_{p-p}	40 max
Differential Input Impedance	K Ohms	7 min
CMRR	dB	40 min
TRANSMITTER (Direct Coupled)*		
Differential Output Voltage	V_{p-p}	6.0 min, 9.0 max
Output Rise and Fall Times	n sec	100 min, 300 max
Output Offset Voltage	mV	±90 max
LOGIC		
V_{IH}	V	2.2 min
V_{IL}	V	0.8 max
CLOCK	MHz	16
POWER SUPPLIES		
+5V (Logic)	V	+5±10%
+5VA (Chan A)	V	+5±10%
+5VB (Chan B)	V	+5±10%
Current Drain (Total Package)		(Typ)/max
Idle	mA	(70)/160
25% Duty Cycle	mA	(205)/310
50% Duty Cycle	mA	(340)/460
100% Duty Cycle	mA	(610)/760
TEMPERATURE RANGE		
Operating (Case)	°C	−55 to +125
Storage	°C	−65 to +150
PHYSICAL CHARACTERISTICS		
Size		
78 pin DIP	in (mm)	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)
82 pin Flatpack	in (mm)	2.19 x 1.6 x 1.7 (55.6 x 40.6 x 4.34)
Weight	oz (g)	1.0 (29)

*Given for direct coupled output across 35 ohms.

TABLE 2. BUS-61555 PIN OUTS			
PIN	**NAME**	**PIN**	**NAME**
1	D00	40	TX/RX-A
2	D02	41	D01
3	D04	42	D03
4	D06	43	D05
5	D08	44	D07
6	D10	45	D09
7	D12	46	D11
8	D14	47	D13
9	RTAD1	48	D15
10	RTAD0	49	RTAD3
11	RTAD4	50	RTAD2
12	ILLCMD	51	RTADP
13	SA/MC-0	52	SA/MC-2
14	LOGIC +5V	53	SA/MC-4
15	SA/MC-1	54	SA/MC-3
16	BCSTRCV	55	THIS-RT
17	LMC	56	RTPARERR
18	NC	57	T/R
19	GNDB	58	+5VB
20	TX/RX-B	59	TX/RX-B
21	LOGIC GND	60	A00
22	A01	61	A02
23	A03	62	A04
24	A05	63	A06
25	A07	64	A08
26	A09	65	A10
27	A11	66	A12
28	A13	67	A14
29	A15	68	MEMWR
30	MEMOE	69	MEMENA-IN
31	MEMENA-OUT	70	INCMD
32	CLOCK IN	71	MSTRCLR
33	MEM/REG	72	INT
34	STRBD	73	IOEN
35	EXTEN	74	SELECT
36	RD/WR	75	READYD
37	EXTLD	76	TAGEN
38	GNDA	77	+5VA
39	NC	78	TX/RX-A

ORDERING INFORMATION

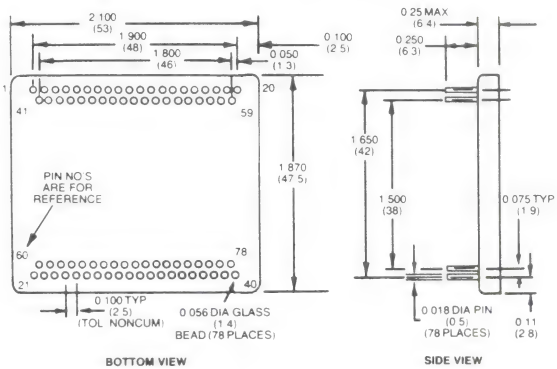
BUS-61555-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

Blank = 0° to 70° C

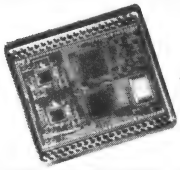


Note: Dimensions are in inches (millimeters).

FIGURE 2. MECHANICAL OUTLINE (DDIP)

DDC
ILC DATA DEVICE CORPORATION

BUS-61559 SERIES



FULL DATA SHEET AVAILABLE

MIL-STD-1553B NOTICE 2 ADVANCED INTEGRATED MUX HYBRIDS with ENHANCED RT FEATURES (AIM-HY'er)

DESCRIPTION

DDC's BUS-61559 series of Advanced Integrated Mux Hybrids with enhanced RT Features (AIM-HY'er) comprise a complete interface between a microprocessor and a MIL-STD-1553B Notice 2 bus, implementing Bus Controller (BC), Remote Terminal (RT), and Monitor Terminal (MT) modes. Packaged in a single 78-pin DIP or 82-pin flat package, the BUS-61559 series contains dual low-power transceivers and encoder/decoders, complete BC/RT/MT protocol logic, memory management and interrupt logic, 8K x 16 of shared static RAM, and a direct, buffered interface to a host processor bus.

The BUS-61559 includes a number of advanced features in support of MIL-STD-1553B Notice 2 and STANAG 3838. Other salient features of the BUS-61559 serve to provide the benefits of reduced board space requirements, enhanced software flexibility, and reduced host processor overhead.

The BUS-61559 contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. Alternatively, the buffers may be operated in a fully transparent mode in order to interface to up to 64K words of external shared RAM and/or connect directly to DDC's component set supporting the 20 MHz STANAG-3910 bus.

The memory management scheme for RT mode provides an option for separation of broadcast data, in compliance with 1553B Notice 2. A circular buffer option for RT message data blocks offloads the host processor for bulk data transfer applications.

Another feature, besides those listed to the right, is a transmitter inhibit control for the individual bus channels.

The BUS-61559 series hybrids operate over the full military temperature range of -55 to +125°C and 883B processing is available. The hybrids are ideal for demanding military and industrial microprocessor-to-1553 applications.

FEATURES

- ***Complete Integrated 1553B Notice 2 Interface Terminal***
- ***Functional Superset of BUS-61553 AIM-HY Series***
- ***Internal Address and Data Buffers for Direct Interface to Processor Bus***
- ***RT Subaddress Circular Buffers to Support Bulk Data Transfers***
- ***Optional Separation of RT Broadcast Data***
- ***Internal Interrupt Status and Time Tag Registers***
- ***Internal RT Command Illegalization***
- ***883B Processing Available***

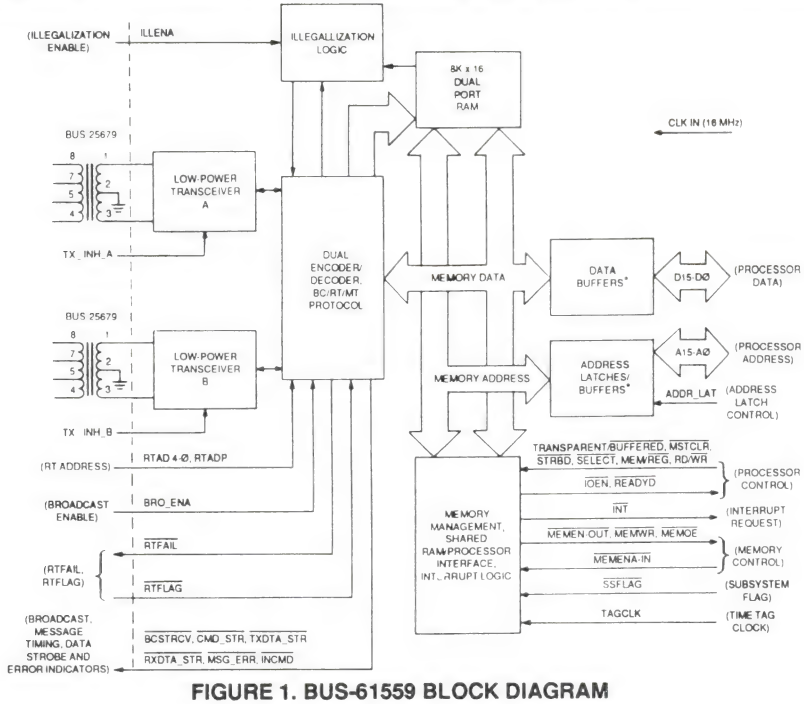
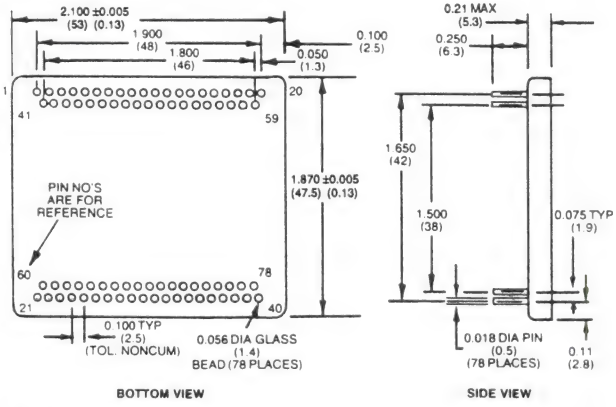


FIGURE 1. BUS-61559 BLOCK DIAGRAM

TABLE 4.
PIN ASSIGNMENTS (DDIP)BUS-61559

PIN	NAME	PIN	NAME
1	D00	40	TX/RX-A
2	D02	41	D01
3	D04	42	D03
4	D06	43	D05
5	D08	44	D07
6	D10	45	D09
7	D12	46	D11
8	D14	47	D13
9	RTAD1	48	D15
10	RTAD0	49	RTAD3
11	RTAD4	50	RTAD2
12	MSG_ERROR	51	RTADP
13	CMD_STR	52	RXDTA_STR
14	LOGIC +5V	53	TXDTA_STR
15	TAGCLK	54	BRO_ENA
16	BCSTRCV	55	RTFAIL
17	ILLENA	56	RTFLAG
18	-15V B	57	TX_INH_B
19	GND B	58	+5V B
20	TX/RX-B	59	TX/RX-B
21	LOGIC GND	60	A00
22	A01	61	A02
23	A03	62	A04
24	A05	63	A06
25	A07	64	A08
26	A09	65	A10
27	A11	66	A12
28	A13	67	A14
29	A15	68	MEMWR
30	MEMOE /ADDR_LAT	69	MEMENA-IN
31	MEMENA-OUT	70	INCMD
32	CLOCK IN	71	MSTCLR
33	MEM/REG	72	INT
34	STRBD	73	IOEN
35	TRANSP/BUFF	74	SELECT
36	RD/WR	75	READYD
37	SSFLAG	76	TX_INH_A
38	GND A	77	+5V A
39	-15V A	78	TR/RX A



NOTES:
1. Dimensions are in inches (millimeters).
2. Leads = KOVAR, plated by 150µ inches minimum nickel, plated by 50µ inches minimum gold.

FIGURE 25. MECHANICAL OUTLINE, DIP (BUS-61559/60)

ORDERING INFORMATION

BUS-61559 - X

Reliability Grade:
- 883B = Fully compliant 883B Processing Available.
- B = 883B Processing Available but without QCI Testing .
- Blank = 0° to 70° C operation.
- 601 = MIL-STD-1760A compatible, with fully compliant 883B Processing Available.

Power Supply and Packaging*:
- 59 = +5V/-15V DDIP
- 60 = +5V/-12V DIP
- 61 = +5V DIP
- 69 = +5V/-15V Flatpack
- 70 = +5V/-12V Flatpack
- 71 = +5V Flatpack

* Consult factory for other voltage and packaging options.

For additional information, please contact the Data Bus Applications Group at 1-800-DDC-1772 x234. In New York State, (516) 567-5600 x234.

D-ABR

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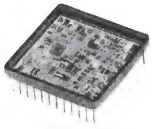
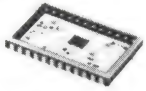
BUS-63100II SERIES

MIL-STD-1553 DATA BUS SINGLE AND DUAL TRANSCEIVERS

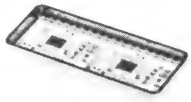
FULL DATA SHEET AVAILABLE



BUS-63102 II



BUS-63105 II



BUS-63125 II

DESCRIPTION

The BUS-63100 II transceivers are complete transmitter and receiver pairs conforming fully to MIL-STD-1553A and 1553B. Features available with selected models of this high reliability series include: Smiths and Harris interface type choices, ±12V/±15V power supply voltage range, variable threshold levels, and single (24 pin DDIP or square) and completely independent dual redundant (36 pin DDIP) packaging configurations. All models are also available in flatpacks.

The receiver section of the BUS-63100 II series accepts phase-modulated bipolar data from a MIL-STD-1553 Data Bus and produces TTL signal data at its outputs: RX Data Out and RX $\overline{\text{Data}}$ Out. These outputs represent positive and negative variations of the input data signals beyond an internally fixed or externally set threshold level. An external STROBE input enables or disables the receiver outputs.

The transmitter section accepts bipolar TTL signal data at its TX Data and TX $\overline{\text{Data}}$ input lines and produces phase-modulated bipolar data at the TX Data and TX $\overline{\text{Data}}$ outputs. The transmitters' output voltage level is typically 28Vpp to 30Vpp. An external input, INHIBIT, takes priority over the transmitter inputs and disables the transmitter when activated with a logic "1".

The small size and different model capabilities available with the BUS-63100 II series simplify engineering design, making it an excellent choice for interfacing with any MIL-STD-1553 system.

FEATURES

- *CONFORMS FULLY TO MIL-STD-1553A AND 1553B*
- *SOME MODELS AVAILABLE TO MILITARY (DESC) DRAWINGS*
- *MODEL CAPABILITIES:*
  SINGLE OR DUAL REDUNDANT PACKAGING
  – 12V/– 15V POWER SUPPLY VOLTAGE RANGE AVAILABLE
  HARRIS OR SMITHS I/O COMPATIBILITY
- *SMALL SIZE:*
  SINGLE – 24 DDIP OR SQUARE
  DUAL – 36 DDIP FLATPACKS
- *LOW POWER*
- *HIGH RELIABILITY – LSI*

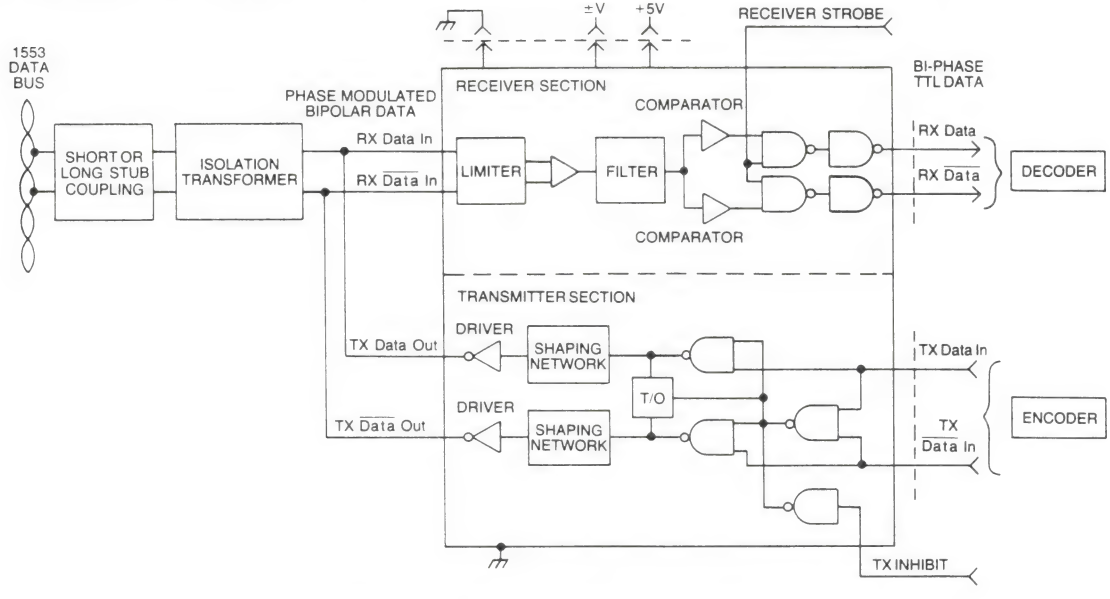


FIGURE 1. BUS-63100 II SERIES BLOCK DIAGRAM

ORDERING INFORMATION

SINGLE TRANSCEIVERS

BUS-63105 II-883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL-STD-883 but without QCI testing
  - Blank = 0° to 70°C
- Power Supply Voltage Range/Package
  - 5 = −15VDC/DDIP
  - 6 = −15VDC/Flatpack
  - 7 = −12VDC/DDIP
  - 8 = −12VDC/Flatpack
- Enc-Dec Compatibility:
  - 0 = Compatible with Harris Encoder/Decoder
  - 1 = Compatible with Smiths Encoder/Decoder

BUS-63105 II available as Military (DESC) drawing 5962-86049-02ZC.

See figure 2 for mating transformer.

BUS-63102 II-883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL-STD-883 but without QCI testing
  - Blank = 0° to 70°C
- 2 = Universal transceiver (MACAIR and 1553) ±12V to ±15V power supply range, compatible with Smiths Encoder/Decoder.
- 4 = 1553, ±12V to ±15V power supply range, compatible with Smiths Encoder/Decoder.
- Packaging:
  - 0 = 24 pin square
  - 1 = 24 pin square flatpack

See figure 2 for mating transformer.

DUAL TRANSCEIVERS

BUS-63125 II-883B

- Reliability Grade: (See note.)
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL-STD-883 but without QCI testing
  - Blank = 0° to 70°C
- Power Supply Voltage Range/Package
  - 5 = −15VDC/DDIP
  - 6 = −15VDC/Flatpack
  - 7 = −12VDC/DDIP
  - 8 = −12VDC/Flatpack
- Enc-Dec Compatibility:
  - 2 = Compatible with Harris Encoder/Decoder
  - 3 = Compatible with Smiths Encoder/Decoder

BUS-63125 II and BUS-63126 II available as Military (DESC) drawing 5962-87579.

See figure 2 for mating transformer.

Note: Available as BUS-63125 II-641 (BUS-65612 compatible Transceiver).

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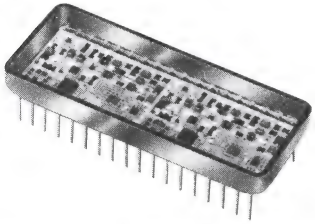


FULL DATA SHEET AVAILABLE

MIL-STD-1553 DATA BUS +5V DUAL TRANSCEIVER

DESCRIPTION

The BUS-63147 transceiver is a complete transmitter and receiver pair conforming fully to MIL-STD-1553A and 1553B. Features include: +5V power supply voltage, Harris interface type, completely independent dual redundant operation, and small size (36 pin DDIP).

The receiver section of the BUS-63147 series accepts phase-modulated bipolar data from a MIL-STD-1553 Data Bus and produces TTL signal data at its outputs: RX DATA OUT and RX $\overline{\text{DATA}}$ OUT. These outputs represent positive and negative variations of the input data signals beyond an internally fixed threshold level. An external STROBE input enables or disables the receiver's outputs.

The transmitter section accepts biphase TTL signal data at its TX DATA and TX $\overline{\text{DATA}}$ inputs and produces phase-modulated bipolar data at the TX DATA and TX $\overline{\text{DATA}}$ outputs. The transmitter's output voltage level is typically 30Vpp. An external input, INHIBIT, takes priority over the transmitter inputs and disables the transmitter when activated with a logic "1".

The small size, +5V power supply voltage, and compliance with MIL-STD-1553 simplify engineering design, making it an excellent choice for interfacing with any MIL-STD-1553 system.

FEATURES

- *ONLY REQUIRES +5V POWER SUPPLY*
- *SMALL SIZE – 36 PIN DDIP*
- *LOW POWER*
- *MIL-STD-883B SCREENING AVAILABLE*
- *DUAL REDUNDANT PACKAGING*
- *HARRIS I/O COMPATIBILITY*
- *CONFORMS FULLY TO MIL-STD-1553A AND 1553B*

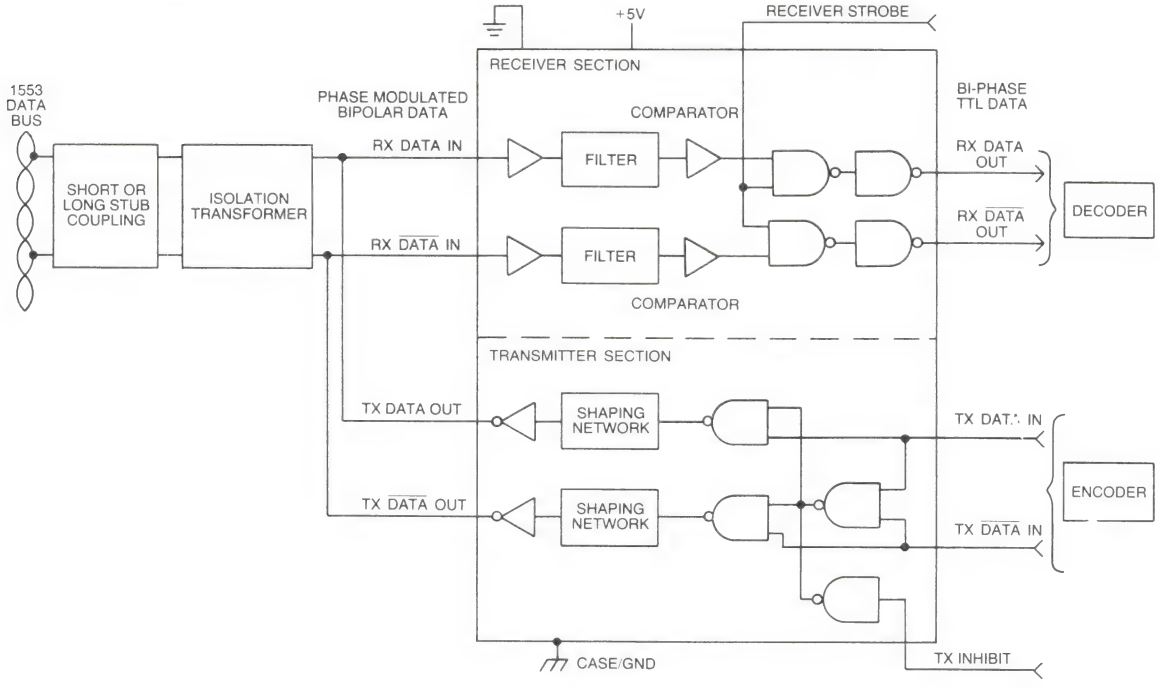
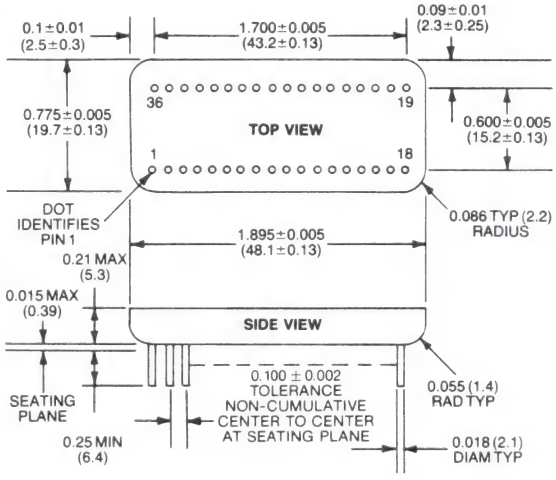


FIGURE 1. BUS-63147 BLOCK DIAGRAM

TABLE 3. BUS-63147 PIN FUNCTIONS

PIN	FUNCTION		PIN	FUNCTION	
1	TX DATA OUT	*	19	NC	
2	TX $\overline{\text{DATA}}$ OUT	*	20	RX DATA IN	**
3	GND	*	21	RX $\overline{\text{DATA}}$ IN	**
4	NC	*	22	GND	**
5	RX DATA OUT	*	23	NC	**
6	STROBE	*	24	+5V	**
7	GND	*	25	INHIBIT	**
8	RX $\overline{\text{DATA}}$ OUT	*	26	TX DATA IN	**
9	GND (CASE)	*	27	TX $\overline{\text{DATA}}$ IN	**
10	TX DATA OUT	**	28	NC	
11	TX $\overline{\text{DATA}}$ OUT	**	29	RX DATA IN	*
12	GND	**	30	RX $\overline{\text{DATA}}$ IN	*
13	NC		31	GND	*
14	RX DATA OUT	**	32	NC	
15	STROBE	**	33	+5V	*
16	GND	**	34	INHIBIT	*
17	RX $\overline{\text{DATA}}$ OUT	**	35	TX DATA IN	*
18	NC		36	TX $\overline{\text{DATA}}$ IN	*

*Channel One
**Channel Two



Dimensions in inches (millimeters).

FIGURE 5. BUS-63147 MECHANICAL OUTLINE

ORDERING INFORMATION

BUS- 63147 - 883B

Reliability Grade:
883B = Fully compliant with MIL-STD-883
B = Screened to MIL-STD-883 but without QCI testing
Blank = 0^{o} to 70^{o} C operation

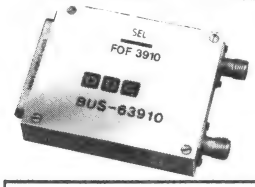
Decoder Compatibility:
7 = Standard Decoder
8 = DDC Bus-65612 PGA

Matching transformer BUS-41429.
SMD Listing: DESC# 5962-89522-01XC

J

DDC
ILC DATA DEVICE CORPORATION

BUS-63910



FULL DATA SHEET AVAILABLE

STANAG 3910 DUAL REDUNDANT FIBER OPTIC TRANSCEIVER

DESCRIPTION

The BUS-63910 40 Mbaud fiber optic transceiver provides a complete electrical to optical front end interface to a dual redundant STANAG 3910/EFABus fiber optic bus. The BUS-63910's intended use is to interface between a reflective star-coupled STANAG 3910 bus, a BUS-63920 Data Retiming Unit, and a BUS-63930 STANAG 3910 Remote Terminal Unit.

For each redundant channel, the BUS-63910 includes a transmitter, receiver, fiber optic Y-coupler, and optical connector.

The transmitter consists of a high-power L.E.D. and temperature compensated driver circuit. The launch power from the transmitter is -2.5 ± 1.5 dBm with a center wavelength of 810 ± 40 nm, in compliance with STANAG 3910/EFABus.

The receiver includes a PIN photodiode transimpedance preamplifier, and custom designed gain stages. The receiver provides a wide dynamic range to accommodate the variations in path attenuation to be found in reflective star-coupled optical systems.

The internal Y-couplers consist of small fused couplers.

The transmitter and receiver sections for the two channels contain individual power control inputs. These inputs allow power consumption to be minimized when the BUS-63910 is idle.

Packaged in a 3.35 x 2.76 x 0.71 inch (85 x 70 x 18 mm) metal case, the BUS-63910 includes a subminiature D electrical connector and a pair of fiber optic connectors that provide compliance to STANAG 3910/EFABus.

FEATURES:

- *20Mbps MANCHESTER II ENCODED DATA (40 Mbaud)*
- *HIGH-POWER L.E.D. TRANSMITTER*
- *PIN DIODE TRANSIMPEDANCE RECEIVER WITH HIGH SENSITIVITY AND WIDE DYNAMIC RANGE*
- *INTERNAL Y-COUPLERS FOR SINGLE FIBER I/O PER PATH*
- *TRANSMITTER AND RECEIVER POWER CONTROL INPUTS*
- *OPTICAL CONNECTORS COMPLIANT TO STANAG 3910/EFABUS SPECIFICATION*

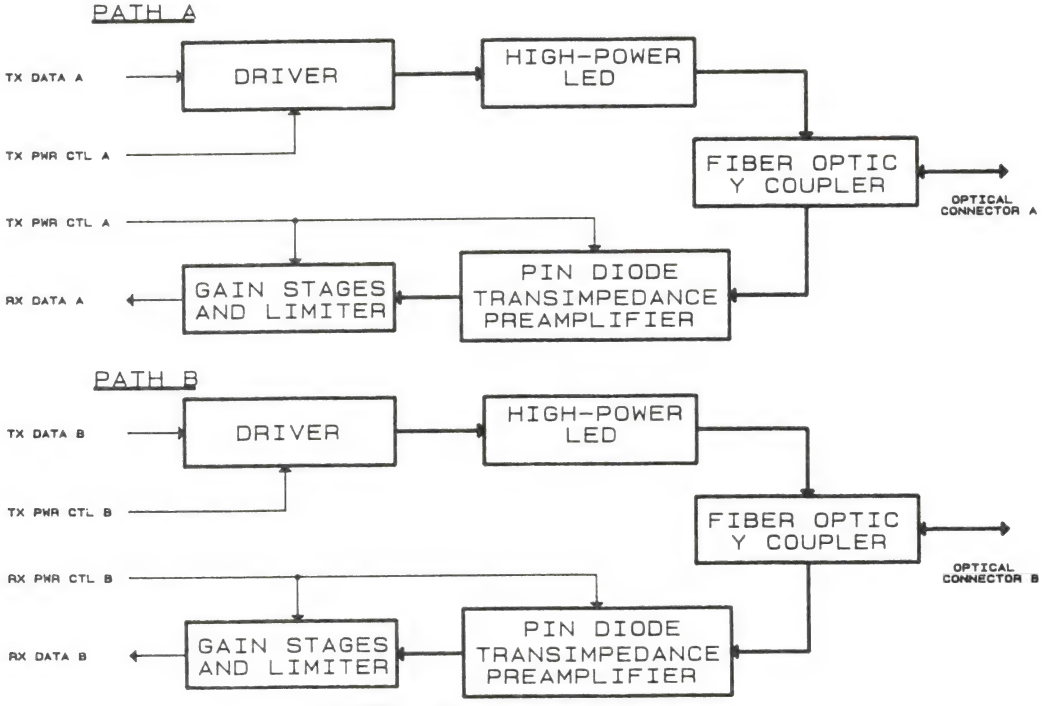


FIGURE 1. BUS-63910 BLOCK DIAGRAM

FIBER OPTIC Y-COUPLER

The Y-couplers join the individual fibers from the respective transmitter and receiver for each path within the BUS-63910. They consist of small fused fiber couplers.

TABLE 2. BUS-63910 SUBMINIATURED CONNECTOR CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V Rx B	12	PWR CTL Tx B
2	+5V Rx B	13	GND
3	-15V Rx B	14	PWR CTL Tx A
4	-15V Tx B	15	N/C
5	-15V Tx A	16	+5V Tx A
6	PWR CTL Rx A	17	GND
7	-15V Rx A	A1	RX B
8	+5V Rx A	A2	TX B
9	+15V Rx A	A3	TX A
10	PWR CTL Rx B	A4	RX A
11	+5V Tx B		

ELECTRICAL CONNECTOR: MS18276-4 PLUG

ELECTRICAL MATING CONNECTOR: MS-18276-4 SOCKET (NOT SUPPLIED)

FIBER OPTIC CONNECTOR: "HA" Receptacle, reference Hellermann-Deutsch drawing number 454092

FIBER OPTIC MATING CONNECTOR: "HA" Plug available from Hellerman-Deutsch, reference drawing number 454093 (NOT SUPPLIED)

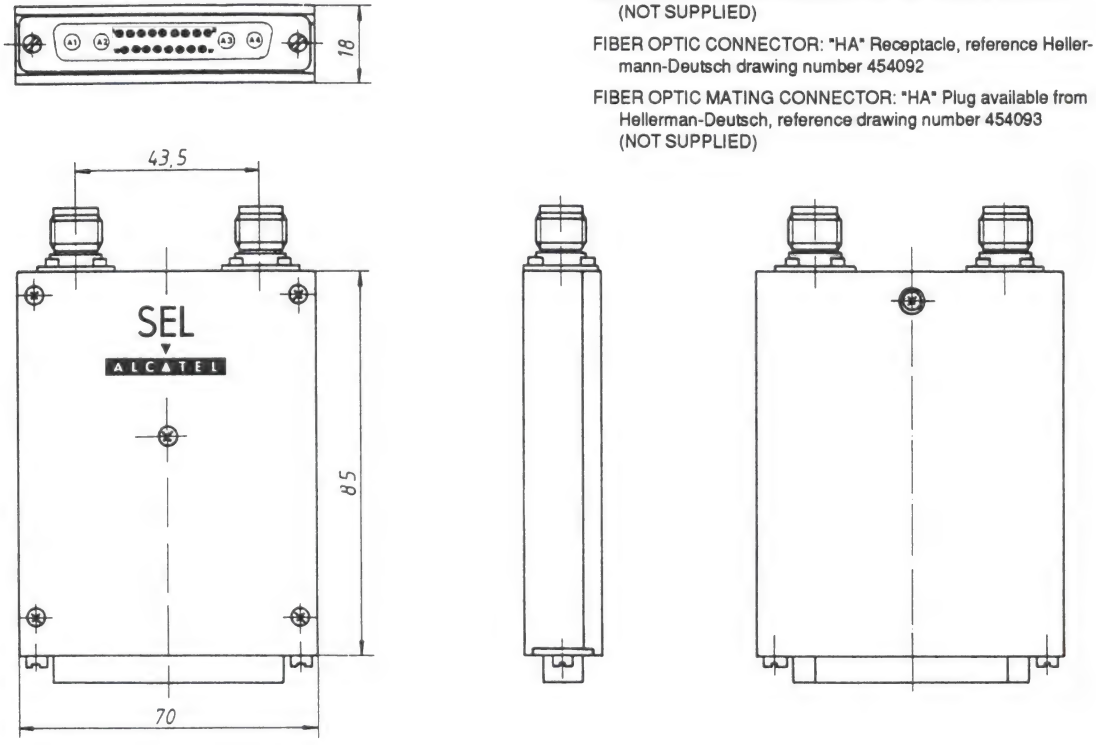


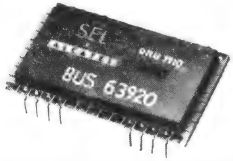
FIGURE 6. BUS-63910 MECHANICAL OUTLINE

ORDERING INFORMATION:

BUS-63910 0° to 70°C

BUS-63910-B -55°C to +95°C

A-ABR



FULL DATA SHEET AVAILABLE

STANAG 3910 DATA RETIMING UNIT

DESCRIPTION

The BUS-63920 Data Retiming Unit extracts clock and serial data from the outputs of a dual redundant STANAG 3910 transceiver. It interfaces directly with the BUS-63910 Fiber Optic Transceiver and the BUS-63930 RT Protocol Unit.

The BUS-63920 accepts raw serial data from the outputs of a STANAG 3910 fiber optic or electrical transceiver. The serial data for STANAG 3910 occurs in a burst mode and is Manchester II encoded at 20 Mbps.

The BUS-63920 includes a multiplexer to select between the two 50 ohm serial inputs. The multiplexer SELECT A/$\overline{B}$ input is provided from a STANAG 3910 protocol device, such as, a BUS-63930 Remote Terminal Unit.

The output of the clock recovery circuit is used to sample the raw data from the selected channel to provide the recovered serial data. Both the 40 MHz recovered clock and the recovered serial data are provided as outputs from the BUS-63920. These two outputs may be connected directly to the BUS-63930 High-Speed RT Protocol Unit.

The BUS-63920 features a fast acquisition time of 1 µs max, as required for the burst data transmission of STANAG 3910. In addition, there is a provision to ensure that there is no clock output or change in the data output during bus idle periods.

The BUS-63920 is packaged in a 16-pin 1.38 x 1.18 x 0.33 inch(35 x 30 x 8.5 mm) hybrid.

FEATURES

- *STANAG 3910 CLOCK RECOVERY*
- *40 MHz CLOCK EXTRACTION*
- *RETIMED DATA OUTPUT*
- *FAST ACQUISITION TIME AS REQUIRED FOR BURST TRANSMISSION*
- *FIBER AND WIRE TRANSCEIVER APPLICATIONS*
- *INPUT MULTIPLEXER TO ACCOMMODATE DUAL REDUNDANT TRANSCEIVER OUTPUTS*

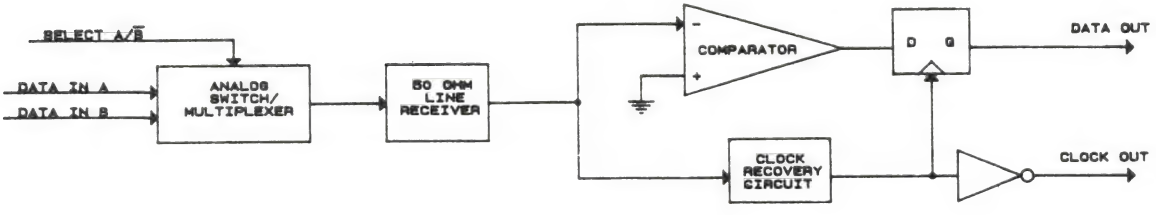


FIGURE 1. BUS-63920 BLOCK DIAGRAM

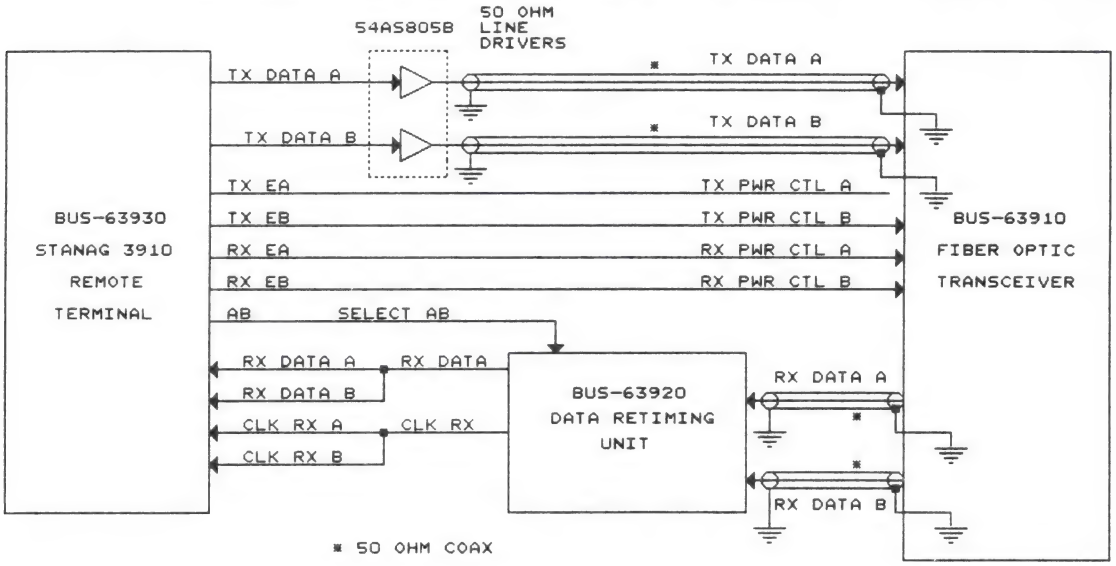


FIGURE 5. INTERCONNECTION DIAGRAM TO BUS-63910 FIBER OPTIC TRANSCEIVER AND BUS-63930 HIGH-SPEED RT PROTOCOL UNIT

TABLE 2. PIN FUNCTIONS			
PIN	FUNCTION	PIN	FUNCTION
1	SELECT	22	NC
2	GND	21	NC
3	DATA IN 1	20	NC
4	GND	19	NC
5	DATA IN 2	18	NC
6	GND	17	NC
7	-5V	16	GND
8	NC	15	+5V
9	GND	14	CLOCK-OUT
10	DATA-OUT	13	GND
11	GND	12	NC

Note: Pins 8 and 12 **must not** be connected to an external signal.

ORDERING INFORMATION

BUS-63920 0°C to 70°C
BUS-63920-B -55°C to +125°C

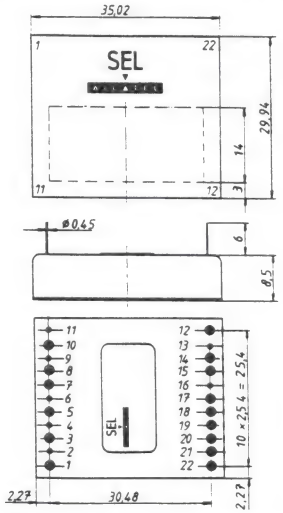
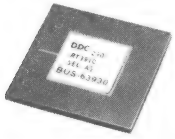


FIGURE 6. BUS-63920 MECHANICAL OUTLINE

A-ABR



STANAG 3910 HIGH-SPEED REMOTE TERMINAL PROTOCOL UNIT

FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-63930 comprises a complete, dual redundant STANAG 3910 high-speed remote terminal protocol device. The BUS-63930 interfaces between a host processor, a STANAG 3838 Terminal such as DDC's BUS-61559 AIM HY'ER, high-speed message RAM, a data retiming unit (DRU), and a 20 Mbps fiber optic transceiver. Packaged in a 180-pin PGA, the BUS-63930 incorporates Frame Logic, Monitor Logic, Arbiter Logic, and Control Logic.

The Frame Logic consists of a 20 Mbps Manchester II encoder/decoder plus Frame Check Sequence (FCS) generator/checking logic. The Monitor Logic interfaces to the STANAG 3838 RT to capture Command Words to the HS subaddress and associated Action Words.

The Arbiter Logic consists of buffers plus contention resolving logic to provide an interface between the host processor, the BUS-63930 registers and up to 2M x 16 of HS RAM. The Control Logic coordinates the activities of the other sections and includes complete state machine logic for STANAG 3910 message processing and error handling.

The BUS-63930 may be interfaced directly to the BUS-61559 STANAG 3838 Advanced Integrated Mux Hybrid (AIM-HY'ER).

The BUS-63930 includes internal registers for overall control, interrupt enabling, programming of transmitter delay timing, self-test, and monitoring of the STANAG 3838 RT's buses. Registers are also provided for the High-Speed Status, Last Action, and BIT words.

The BUS-63930 provides a pointer-driven memory management scheme with double buffering. Other features include interrupts, time tagging, implementation of all STANAG 3910 mode codes and built-in self-test.

The BUS-63930 is fabricated in 0.9 micron HCMOS and operates at a very low standby current of 2 mA max.

FEATURES

- *COMPREHENSIVE IMPLEMENTATION OF STANAG 3910 HIGH-SPEED DUAL REDUNDANT RT PROTOCOL*
- *DIRECT INTERFACE TO BUS-61559 STANAG 3838 HYBRID, BUS-63910 FIBER OPTIC TRANSCEIVER, AND BUS-63920 DATA RETIMING UNIT*
- *REGISTER ORIENTED ARCHITECTURE*
- *SUPPORTS UP TO 2M WORDS OF RAM*
- *BUILT-IN SELF-TEST*
- *LOW POWER HCMOS*
- *180-PIN PGA*

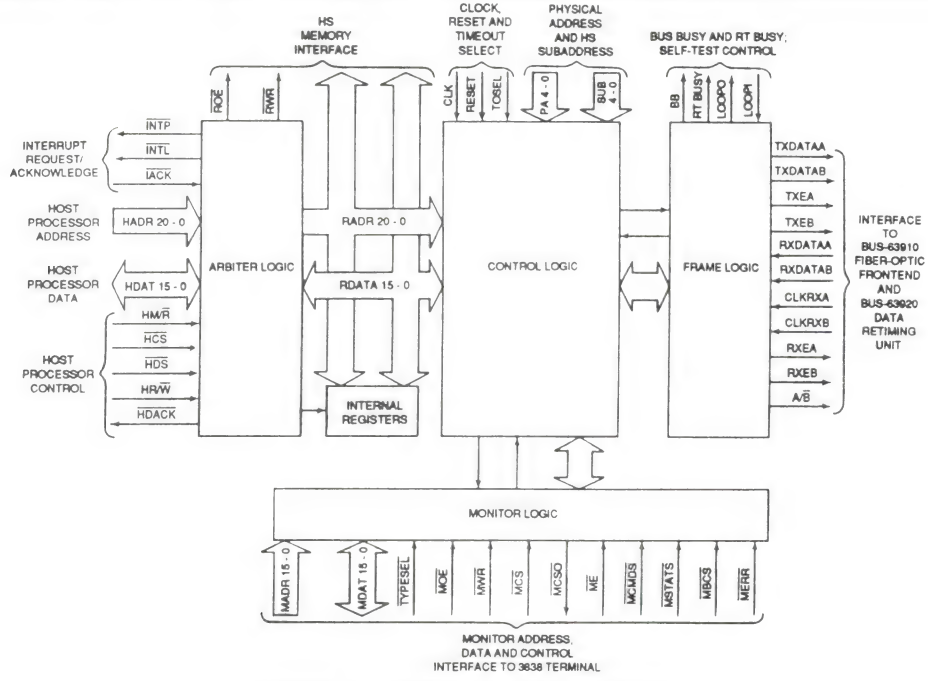

HS MEMORY INTERFACE
CLOCK, RESET AND TIMEOUT SELECT
PHYSICAL ADDRESS AND HS SUBADDRESS
BUS BUSY AND RT BUSY; SELF-TEST CONTROL
INTERRUPT REQUEST/ ACKNOWLEDGE
HOST PROCESSOR ADDRESS
HOST PROCESSOR DATA
HOST PROCESSOR CONTROL
ARBITER LOGIC
CONTROL LOGIC
FRAME LOGIC
INTERNAL REGISTERS
MONITOR LOGIC
INTERFACE TO BUS-63910 FIBER-OPTIC FRONTEND AND BUS-63920 DATA RETIMING UNIT
MONITOR ADDRESS, DATA AND CONTROL INTERFACE TO 3838 TERMINAL

FIGURE 1. BUS-63930 BLOCK DIAGRAM

TABLE 5. PIN FUNCTION TABLE (continued)		
Monitor Interface to STANAG 3838 RT (continued)		
Pin Name	**Pin**	**Function**
$\overline{MBCS}$	L15	Monitor Broadcast Strobe. When using the Type 1 interface configuration to a STANAG 3838 RT, this input strobe indicates that the received LS message was directed to the broadcast address.
$\overline{MERR}$	K15	Monitor Message Error. This signal indicates an error occurred during the current LS message sequence. Not used if bit 7 of the Control Register is logic 1.
Test Pins		
Pin Name	**Pin**	**Function**
TEST1	A3	For normal operation, TEST 1 must be connected to Ground. When set to high, the following signals are put in their high impedance state: RADR20-0, RDAT15-0, $\overline{ROE}$, $\overline{RWR}$, HDAT15-0, $\overline{HDACK}$, and MDAT15-0.
TEST2	E12	Do not connect.
TEST3	G13	Do not connect.
TEST4	D12	Do not connect.
TEST5	F12	Do not connect.
TEST6	A2	Do not connect.

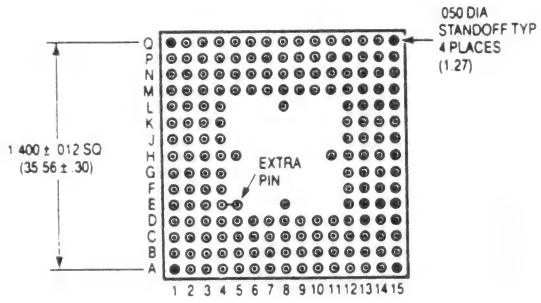


FIGURE 30. MECHANICAL OUTLINE DRAWING

ORDERING INFORMATION

BUS-63930 for 0°C to 70°C operating temperature.

BUS-63930 -B FOR -55°C to +125°C operating temperature.

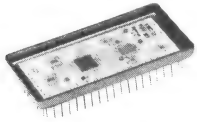
J

A-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-64100II

MIL-STD-1553 TERMINAL BIT PROCESSOR



FULL DATA SHEET AVAILABLE

IMPROVED CONTACT FACTORY

DESCRIPTION

The DDC BUS-64100II is a terminal Bit Processor, which consists of a Manchester II Converter and a DDC advanced custom LSI monolithic chip. Packaged in a single hybrid it has improved reliability and low power dissipation. It is capable of interfacing MIL-STD-1553 transceiver, such as DDC's Monolithic BUS-63115 to an associated subsystem's parallel or serial interface. Its 1 MHz data rate makes it compatible with transceivers that process either McDonnell Douglas MACAIR sinusoidal or trapezoidal waveforms. The BUS-64100II can be used as a common interface for remote terminals, bus monitors or bus controllers.

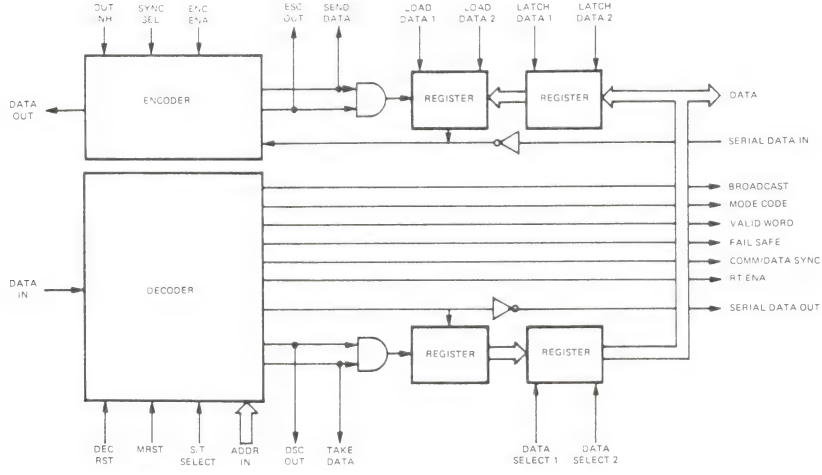
This unit functions as a decoder per MIL-STD-1553 by transferring all command, status and data words to the subsystem, together with error information, BIT status and necessary handshake signals. It flags Address Recognition, Broadcast and Mode Code decoding terminal fail safe signal and contains a built-in Self-test Circuit.

The subsystem can control the transmission of data through positive handshaking of the logic control lines provided. The unit accepts parallel or serial data then transmits the Command, Status or Data words as directed by the subsystem. By virtue of its extensive input/output logic configuration the BUS-64100II will provide interfacing for BUS Controllers.

The BUS-64100II meets the full specifications of MIL-STD-1553 A & B and those of MACAIR A5690, A3818, A4905 and A5232. The hybrid is available with MIL-STD-883B screening and operates over the full MIL temperature range of −55°C to +125°C.

FEATURES

- *16 BIT OR 8 BIT BYTE PARALLEL OR SERIAL I/O*
- *PERFORMS MIL-STD-1553 FUNCTIONS:*
  - *BROADCAST*
  - *MODE CODE*
  - *OWN ADDRESS*
  - *TIME OUT*
- *ON/OFF LINE SELF-TEST*
- *DUAL RANK REGISTERS*
- *LOW POWER LSI DESIGN*



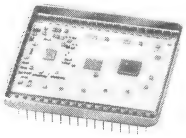
B-ABR

FIGURE 1. BUS-64100II BLOCK DIAGRAM

DDC
ILC DATA DEVICE CORPORATION

BUS-65101II AND BUS-65102II

MIL-STD-1553 DUMB RTU HYBRID



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-65101II MIL-STD-1553 Dumb Remote Terminal Unit (RTU) consists of a transceiver, and encoder/decoder, control logic, dual rank I/O registers and internal clock oscillator packaged in a 1.6" x 1.9" hermetic hybrid. It provides all the functions required to interface between a MIL-STD-1553 serial MUX data bus and a subsystem parallel 3-state data highway. Utilizing several DDC custom monolithic ICs, the BUS-65101II provides sufficient handshaking, control and data lines to permit versatile operation as a remote terminal, a bus controller or a bus monitor, in either single or dual redundant data bus configurations.

As a transmitter, the BUS-65101II accepts 8 bit or 16 bit parallel data from the subsystem, and outputs serial Manchester II coded Command, Status or Data words, under subsystem control. As a receiver, it accepts serial MIL-STD-1553 transmissions and transfers all Command, Status and Data words to the 8 bit or 16 bit data highway, under subsystem control. The BUS-65101II also provides flags to the subsystem when Broadcast, Mode Code, and Own Address (with parity) commands are decoded.

The BUS-65101II contains a terminal fail-safe timeout circuit which flags message lengths exceeding 768 microseconds, and terminates serial data transmission. Wraparound self-test is initiated by a control line which causes the encoder serial output to be connected to the decoder input. The BUS-65101II provides a serial output of decoded words, thus allowing Command Word look-ahead, for the fastest terminal response.

FEATURES

- *INCLUDES:*
  - *TRANSCEIVER*
  - *ENCODER/DECODER*
  - *DUAL RANK I/O REGISTERS*
  - *FAIL-SAFE TIMER*
  - *CLOCK OSCILLATOR*
- *SMALL 1.6" x 1.9" HYBRID*
- *PROVIDES FLAGS FOR:*
  - *OWN ADDRESS (WITH PARITY)*
  - *MODE CODE*
  - *BROADCAST*
  - *TIME OUT*
  - *VALID WORD*
  - *SYNC TYPE*
- *16 BIT OR 8 BIT 3-STATE PARALLEL I/O AND SERIAL OUT*
- *WRAPAROUND BUILT-IN TEST*
- *SIMPLE CONTROLS FOR SINGLE OR DUAL REDUNDANT DATA BUS CONFIGURATIONS*

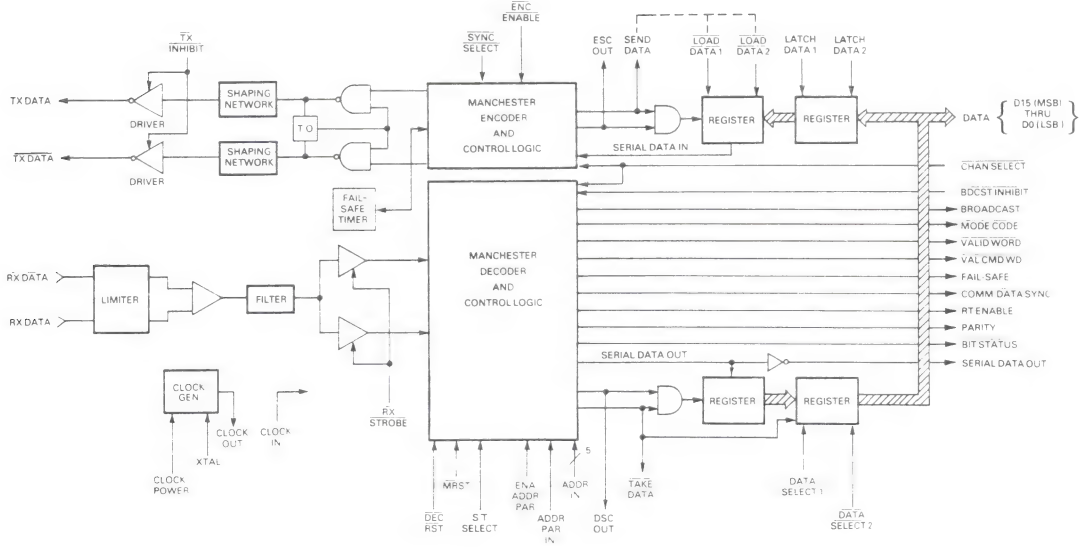


FIGURE 1. BUS-65101II BLOCK DIAGRAM

J

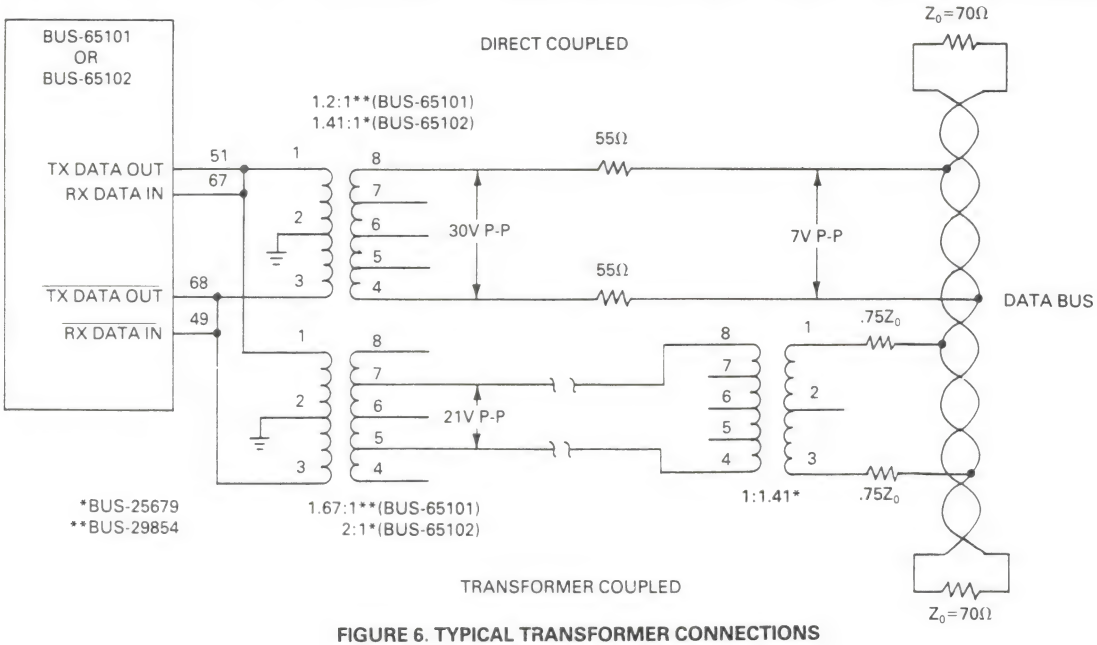
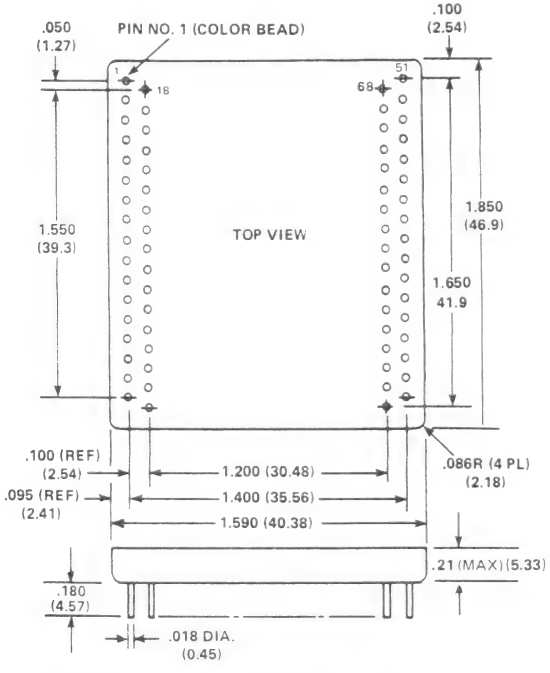


FIGURE 6. TYPICAL TRANSFORMER CONNECTIONS

MECHANICAL OUTLINE



Note: Dimensions in inches (millimeters)

A-ABR

ORDERING INFORMATION

BUS-65101II-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

Blank = 0° to 70° C

Power Supply Option:

1 = −12 VDC

2 = −15 VDC

Note:

Use BUS-29854 transformer with BUS-65101II (direct-coupled).

Use BUS-25679 transformer with BUS-65102II (direct-coupled).

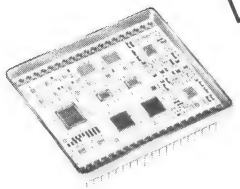
Order BUS-65201 For MCAIR Applications.

DDC
ILC DATA DEVICE CORPORATION

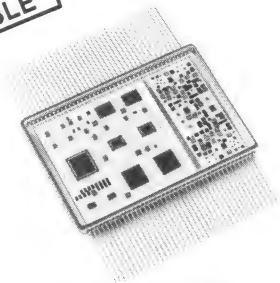
BUS-65112 AND BUS-65117

MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID

FULL DATA SHEET AVAILABLE



BUS-65112 DDIP



BUS-65117 FLATPACK

DESCRIPTION

The BUS-65112 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. Based upon DDC custom ICs, it includes 2 transceivers, 2 encoder/decoders, 2 bit processors, RTU protocol, data buffers, and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count outputs. Error detection and recovery are enhanced by BUS-65112 special features. A 14 bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BUS-65112 performs continuous on-line wrap-around self-test, and provides 4 error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its small hermetic package, −55°C to +125°C operating temperature range, and complete RTU operation make the BUS-65112 ideal for most MIL-STD-1553 applications.

FEATURES

- *SMALL SIZE & LOW POWER*
- *COMPLETE RTU PROTOCOL*
- *SUPPORTS 13 MODE CODES: ANY COMBINATIONS CAN BE ILLEGALIZED*
- *TRANSFERS DATA WITH DMA TYPE HANDSHAKING*
- *LATCHED OUTPUTS FOR COMMAND WORD AND WORD COUNT*
- *14 BIT BUILT-IN-TEST WORD REGISTER*
- *4 ERROR FLAG OUTPUTS*
- *CONTINUOUS ONLINE SELF-TEST*
- *PLUG-IN & FLATPACK PACKAGING*

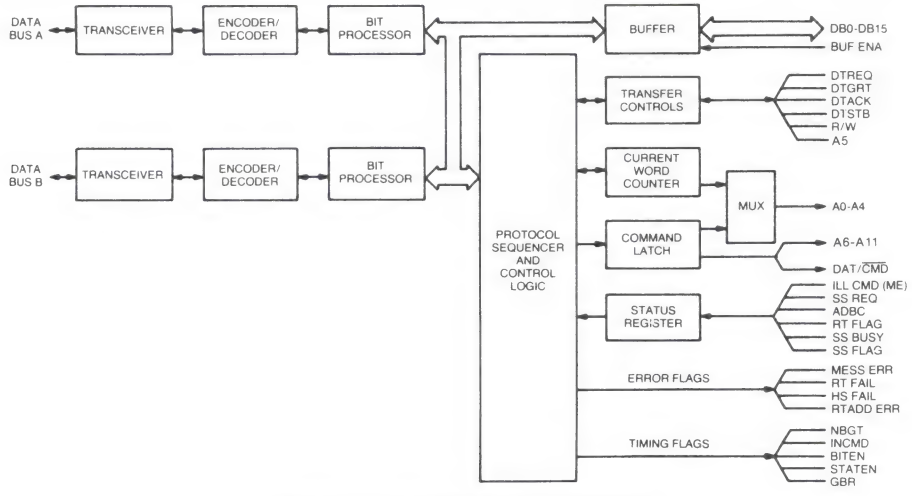


FIGURE 1. BUS-65112 BLOCK DIAGRAM

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FACTORY TEST

The BUS-65112 is capable of performing two internal tests.

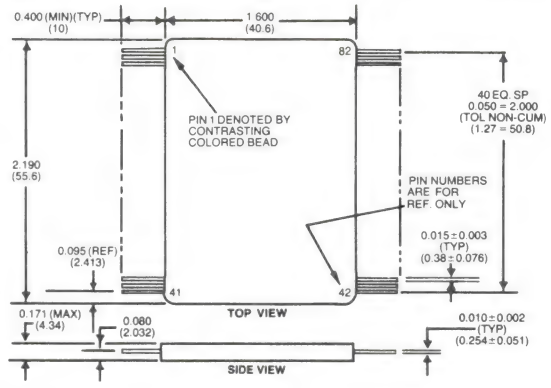
TEST 1, PIN 70. A logic low on this pin will cause the last word of the next message to be repeated continuously until the built in Watch Dog Timeout circuit disables the transmitter. The transmitter will be re-enabled upon receipt of the next valid command to the BUS-65112 on that channel.

TEST 2, PIN 31. This pin indicates the result of the loop test comparison test. It is performed for every word transmitted to the 1553 bus.

(1 = Pass, 0 = Fail) The result is reset upon transmission of the next word over the bus.

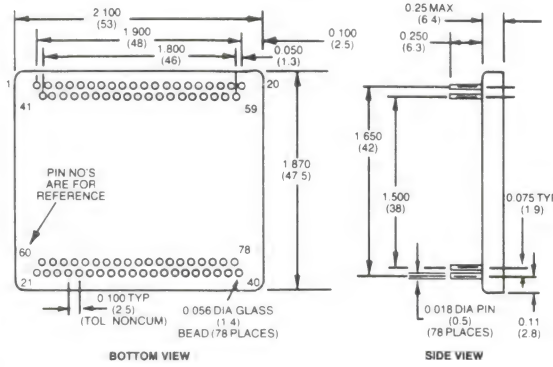
BUS-65117 FLATPACK PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	NC	42	NC
2	A10	43	$\overline{\text{NBGT}}$
3	A9	44	$\overline{\text{STATEN}}$
4	A8	45	TXDATA OUT A
5	A7	46	$\overline{\text{TXDATA}}$ OUT A
6	A6	47	−15V A
7	DB0	48	+15V A
8	DB1	49	+5V A
9	DB2	50	GND A
10	DB3	51	$\overline{\text{RXDATA}}$ IN A
11	DB4	52	RXDATA IN A
12	DB5	53	$\overline{\text{BITEN}}$
13	DB6	54	$\overline{\text{ME}}$
14	DB7	55	$\overline{\text{SRQ}}$
15	DB8	56	$\overline{\text{SSFLAG}}$
16	DB9	57	$\overline{\text{ILLCMD}}$
17	DB10	58	$\overline{\text{BUSY}}$
18	DB11	59	A11
19	DB12	60	TEST 1
20	DB13	61	TEST 2
21	DB14	62	$\overline{\text{RTFLAG}}$
22	DB15	63	$\overline{\text{ABDC}}$
23	+5V	64	$\overline{\text{RESET}}$
24	BRO ENA	65	$\overline{\text{DTREQ}}$
25	GROUND	66	$\overline{\text{BUF ENA}}$
26	ADDRE	67	$\overline{\text{RTFAIL}}$
27	ADDRD	68	12 MHz IN
28	ADDRC	69	A5
29	ADDRB	70	$\overline{\text{GBR}}$
30	ADDRA	71	$\overline{\text{DTSTR}}$
31	ADDRP	72	R/$\overline{\text{W}}$
32	$\overline{\text{RTADERR}}$	73	$\overline{\text{HSFAIL}}$
33	TXDATA OUT B	74	A4
34	$\overline{\text{TXDATA}}$ OUT B	75	INCMD
35	−15VB	76	$\overline{\text{DTACK}}$
36	+15VB	77	$\overline{\text{DTGRT}}$
37	+5VB	78	A0
38	GND B	79	A1
39	$\overline{\text{RXDATA}}$ IN B	80	A2
40	RXDATA IN B	81	A3
41	NC	82	NC



Note: Dimensions are in inches (millimeters).

FIGURE 7. BUS-65117 MECHANICAL OUTLINE (FLATPACK)



Note: Dimensions are in inches (millimeters).

FIGURE 8. BUS-65112 MECHANICAL OUTLINE (DDIP)

ORDERING INFORMATION

BUS-65112 – 883B

Reliability Grade:
- 883B = Fully compliant with MIL-STD-883.
- B = Screened to MIL-STD-883 but without QCI testing.
- Blank = Standard DDC procedures.

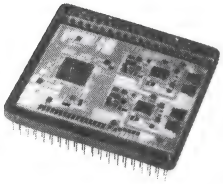
Power Supply and Packaging
- 2 = ±15VDC, DDIP
- 3 = ±12VDC, DDIP
- 7 = ±15VDC, Flatpack
- 8 = ±12VDC, Flatpack

I-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-65142 AND BUS-65144

MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-65142 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. The device is based upon two DDC custom ICs, which includes two monolithic low power Mark II transceivers and one CMOS-SOS RTU protocol containing data buffers and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count outputs. Error detection and recovery are enhanced by BUS-65142 special features. A 14 bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BUS-65142 performs continuous on-line wrap-around self-test, and provides 4 error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its small hermetic package, −55°C to +125°C operating temperature range, and complete RTU operation make the BUS-65142 ideal for most MIL-STD-1553 applications requiring hardware or microprocessor subsystems.

FEATURES

- *LOW POWER & LOW COST*
- *HIGH RELIABILITY*
- *SOS & BIPOLAR*
- *SUPPORTS ALL 13 MODE CODES*
- *MODE CODE/COMMAND WORD ILLEGALIZATION*
- *DMA TRANSFERS*
- *CONTINUOUS SELF-TEST*
- *SEAFAC TESTED COMPONENTS*
- *BUILT-IN-TEST WORD REGISTER*
- *16MHz DECODERS OFFER IMPROVED NOISE REJECTION & ZERO CROSSING DETECTION*

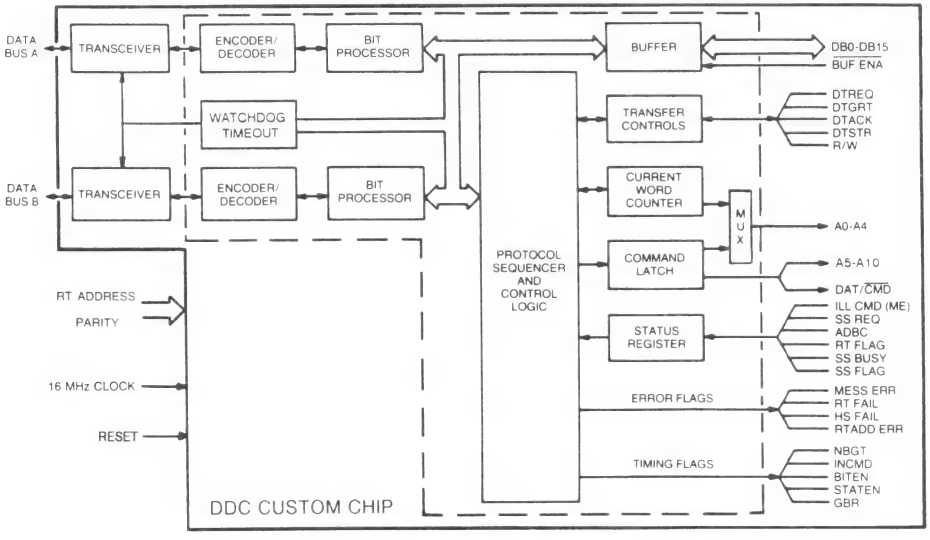


FIGURE 1. BUS-65142 BLOCK DIAGRAM

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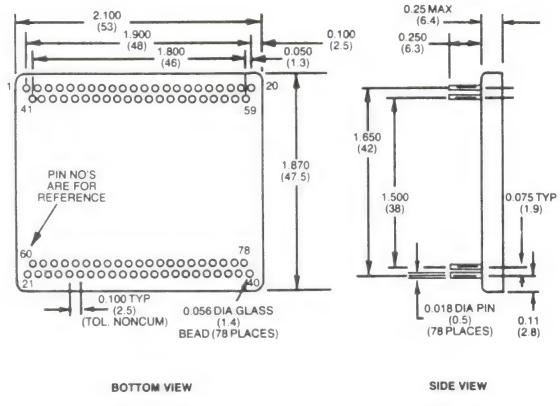
PIN FUNCTION TABLE			
PIN	NAME	PIN	NAME
1	A9	41	A8
2	A7	42	A6
3	A5	43	DB0
4	DB1	44	DB2
5	DB3	45	DB4
6	DB5	46	DB6
7	DB7	47	DB8
8	DB9	48	DB10
9	DB11	49	DB12
10	DB13	50	DB14
11	DB15	51	+5V
12	BRO ENA	52	GND
13	ADDRE	53	ADDRD
14	ADDRC	54	ADDRB
15	ADDRA	55	ADDRP
16	$\overline{\text{RTADERR}}$	56	TXDATA B
17	$\overline{\text{TXDATA B}}$	57	–15VB
18	NC	58	+5VB
19	GND B	59	$\overline{\text{RXDATA B}}$
20	RXDATA B	60	A2
21	A3	61	A0
22	A1	62	$\overline{\text{DTACK}}$
23	$\overline{\text{DTGRT}}$	63	A4
24	INCMD	64	R/$\overline{\text{W}}$
25	$\overline{\text{HSFAIL}}$	65	$\overline{\text{GBR}}$
26	$\overline{\text{DTSTR}}$	66	16 MHz IN
27	(DAT/$\overline{\text{CMD}}$)	67	$\overline{\text{BUF ENA}}$
28	$\overline{\text{RTFAIL}}$	68	$\overline{\text{RESET}}$
29	$\overline{\text{DTREQ}}$	69	$\overline{\text{RTFLAG}}$
30	$\overline{\text{ADBC}}$	70	TEST 1
31	TEST2	71	$\overline{\text{BUSY}}$
32	A10 (T/$\overline{\text{R}}$)	72	$\overline{\text{SSFLAG}}$
33	$\overline{\text{ILLCMD}}$	73	$\overline{\text{ME}}$
34	$\overline{\text{SRQ}}$	74	RXDATA A
35	$\overline{\text{BITEN}}$	75	GNDA
36	$\overline{\text{RXDATA A}}$	76	NC
37	+5VA	77	$\overline{\text{TXDATA A}}$
38	–15VA	78	$\overline{\text{STATEN}}$
39	TXDATA A		
40	$\overline{\text{NBGT}}$		



Note: Dimensions are in inches (millimeters).

FIGURE 7. BUS-65142 MECHANICAL OUTLINE (DDIP)

ORDERING INFORMATION

BUS-65142-883 *

Reliability Grade:
- 883B = Fully compliant with MIL-STD-883.
- B = Screened to MIL-STD-883 but without QCI testing.

Power Supply Option & Packaging
- 2 = –15VDC DDIP
- 3 = –12VDC DDIP
- 4 = –15VDC Flatpack
- 5 = –12VDC Flatpack

* Contact factory about class 'S' screening.

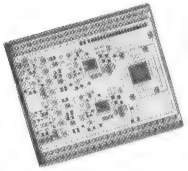
Mating Data Bus Transformers:
for BUS-65142 use DDC BUS-25679
for BUS-65143 use DDC BUS-29854

D-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-65149

MIL-STD-1553A/B & McAIR UNIVERSAL MULTI-PROTOCOL REMOTE TERMINAL



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-65149 is the world's first dual redundant universal MIL-STD-1553 Remote Terminal (RT) hybrid. The BUS-65149 features a universal sinusoidal transceiver and pin selectable options providing for support of MIL-STD-1553A; MIL-STD-1553B; McAIR A3818, A5232, and A5690; the various G.D. F16 protocols; and GRUMMAN SPG151A.

The BUS-65149 provides all of the functions required to interface between a MIL-STD-1553 dual redundant serial data bus and a subsystem parallel three-state data bus. A pair of BUS-27765 transformers are required to interface between the BUS-65149 and the 1553 bus. See Figure 1, block diagram.

The BUS-65149 is compatible with all microprocessors, supporting both DMA and shared RAM interfaces. In addition, the 8/16-bit direct memory inteface (DMA) handshake and three-state parallel data and address buses facilitate the interface to simple systems without a microprocessor.

The BUS-65149 implements all MIL-STD-1553 message formats. Complete error detection capability is provided. This includes sync, encoding, parity, bit and word count, undefined commands, and RT-to-RT transfer errors.

The BUS-65149 features the capability for implementing all dual redundant MIL-STD-1553B mode codes. In addition, any command may (optionally) be illegalized through the use of an external PROM, PAL, or RAM device.

The device is available screened to MIL-STD-883B in a MIL-STD-1772 certified facility and operates over the full military temperature range of -55° C to +125° C.

FEATURES

- *SUPPORTS:*
  - *MIL-STD-1553A/B*
  - *McAIR A3818, A5232, AND A5690*
  - *GENERAL DYNAMICS 16PP303 (F16)*
  - *GRUMMAN SPG151A*
- *DUAL UNIVERSAL TRANSCEIVER SATISFIES McAIR AND 1553A/B*
- *SUPPORTS 1553A/B MODE CODES*
- *INTERNAL AND EXTERNAL OPTIONS FOR STATUS AND BIT WORDS*
- *INTERFACE FLEXIBILITY*
  - *SIMPLE SYSTEMS*
  - *8/16-BIT DMA OR SHARED RAM*
- *SUPPORTS COMMAND ILLEGALIZATION*
- *CONTINUOUS ON-LINE, BUILT-IN-TEST*
- *12 OR 16 MHZ CLOCK OPERATION*

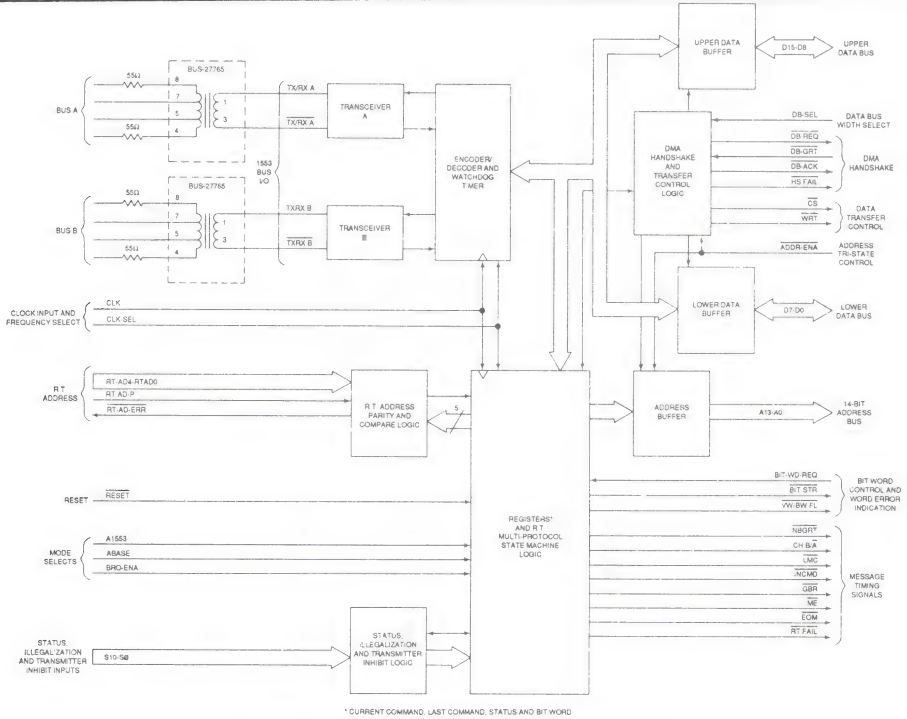
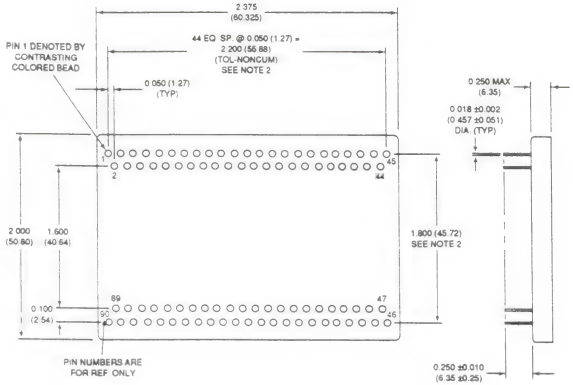


FIGURE 1. BUS-61549 BLOCK DIAGRAM

J

TABLE 4. BUS-65149 PINOUT (preliminary, 2/14/90)			
PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	+5V (LOGIC)	46	-12/15V_B
2	D15	47	GND_A
3	D14	48	+12/15V_A
4	D13	49	+5V_A
5	D12	50	TX/RX_A
6	D11	51	$\overline{\text{TX/RX\_A}}$
7	D10	52	$\overline{\text{CH\_B/A}}$
8	D09	53	$\overline{\text{EOM}}$
9	D08	54	$\overline{\text{RESET}}$
10	D07	55	$\overline{\text{T-D-STR}}$
11	D06	56	$\overline{\text{INCMD}}$
12	D05	57	$\overline{\text{NBGRT}}$
13*	D04	58	CLOCK_SEL
14	D03	59	ABASE
15	D02	60	A1553
16	D01	61	$\overline{\text{LMC}}$
17	D00	62	A13
18	RT_AD-4	63	A12
19	RT_AD_3	64	A11
20	RT_AD_2	65	A10
21	RT_AD_1	66	A09
22	RT_AD_0	67	A08
23	RT_AD_P	68	A07
24	BRO_ENA	69	A06
25	BIT_WD_REQ	70	A05
26	$\overline{\text{DT\_GRT}}$	71	A04
27	$\overline{\text{HS\_FAIL}}$	72	A03
28	$\overline{\text{CS}}$	73	A02
29	$\overline{\text{BW\_STR}}$	74	A01
30	$\overline{\text{WRT}}$	75	A00
31	DB_SEL	76	$\overline{\text{TEST\_MODE}}$
32	VW_BW_FL	77	CLOCK_IN
33	$\overline{\text{ADDR\_ENA}}$	78	$\overline{\text{T\_A\_STR}}$
34	$\overline{\text{DT\_REQ}}$	79	S10
35	$\overline{\text{RT\_FAIL}}$	80	S09
36	$\overline{\text{ME}}$	81	S08
37	$\overline{\text{RT\_AD\_ERR}}$	82	S07
38	$\overline{\text{GBR}}$	83	S06
39	$\overline{\text{DT\_ACK}}$	84	S05
40	$\overline{\text{TX/RX\_B}}$	85	S04
41	TX/RX_B	86	S03
42	+5VB	87	S02
43	+12/15V_B	88	S01
44	GND_B	89	S00
45	-12/15V_B	90	GND (LOGIC)



Notes:
1. Dimensions are in inches (millimeters).
2. Pin cluster to be centralized within ±0.010 (0.25 mm) of outline dimensions.

BUS-65149 MECHANICAL OUTLINE (90-PIN DIP HYBRID)

ORDERING INFORMATION

BUS-65149-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

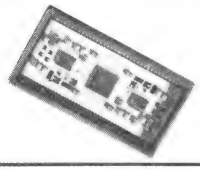
B = Screened to MIL-STD-883 but without QCI testing.

Blank = 0° to 70° C

B-ABR

BUS-65153

MIL-STD-1553B, NOTICE 2 & MIL-STD-1760A "STIC" – SMALL TERMINAL INTERFACE CIRCUIT



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-65153 is a complete, dual redundant MIL-STD-1553B Remote Terminal. Packaged in a 1.90 x 1.0 x 0.2", 70-pin ceramic package, the BUS-65153 provides the output voltage level required for MIL-STD-1760. Also in support of MIL-STD-1760, the RT address inputs are latchable.

The BUS-65153 contains two (2) low power transceivers and a DDC custom designed chip. This chip includes dual encoder/decoder, RT protocol logic, 3-state data buffers, and DMA transfer control logic. The BUS-65153 supports all 13 dual redundant mode codes, any combination of which may be illegalized by an external PROM, PLD, or RAM device.

Parallel data transfers are accomplished via a DMA type handshake. Both 8-bit and 16-bit transfers are supported.

The BUS-65153 can be easily interfaced to most CPU's. In addition, the BUS-65153 can interface directly to minimum complexity subsystems such as switches, D/A converters, etc.

The address bus and transfer control signals may be configured for either two-state or three-state operation. Use of the three-state address mode reduces the number of external components required for a DMA processor interface.

The input clock frequency is user selectable for either 12 or 16 MHz. In the 12 MHz mode, the decoder operates at 24 MHz, providing superior word error rate and zero crossing distortion tolerance. The Busy, Service Request, and Subsystem Flag RT Status Word bits are provided as discrete pins, allowing for easy access by the subsystem.

Various message timing and error flag indicators are provided to facilitate the subsystem interface.

FEATURES

- *Supports MIL-STD-1553B Notice 2 and MIL-STD-1760A Stores Management*
- *Complete Integrated Remote Terminal Including:*
  - *Dual Low Power Transceiver*
  - *Complete RT Protocol Logic*
- *Small, 70-Pin Ceramic Package*
- *Reduces External Component Count*
  - *Selectable 8/16-bit DMA Interface*
  - *Optional Tristate Address Bus and Control Signals*
- *Direct Interface to Simple Systems*
- *Selectable Input Clock, 12, or 16 MHz*
- *883B Processing Available*

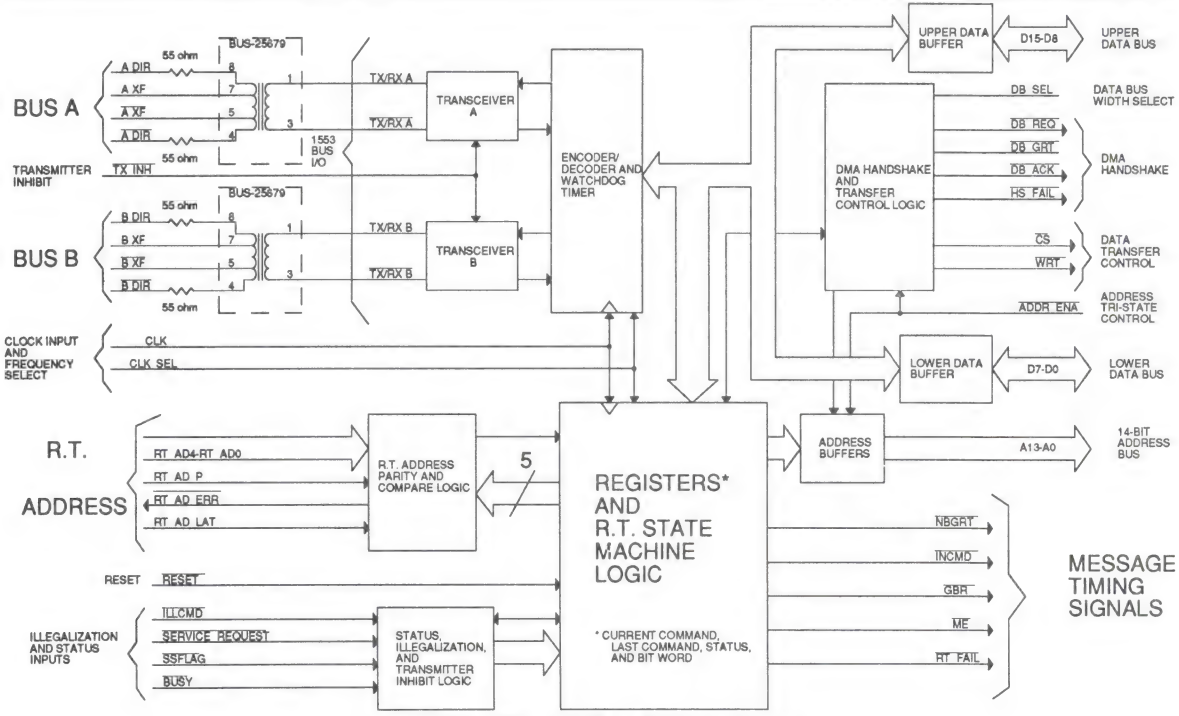


FIGURE 1. BUS-65153 BLOCK DIAGRAM

J

TABLE 4. BUS-65153 PIN DESCRIPTIONS	
PIN #	NAME
1	$\overline{\text{DT\_GRT}}$
2	$\overline{\text{DTACK}}$
3	$\overline{\text{CS}}$
4	$\overline{\text{WRT}}$
5	RX/TX B
6	$\overline{\text{HS\_FAIL}}$
7	$\overline{\text{ADDR\_ENA}}$
8	$\overline{\text{DB\_SEL}}$
9	$\overline{\text{RX/TX B}}$
10	DB15 (MSB)
11	DB14
12	DB13
13	DB12
14	DB11
15	DB10
16	DB09
17	DB08
18	GND
19	DB07
20	DB06
21	DB05
22	DB04
23	DB03
24	DB02
25	DB01
26	DB00 (LSB)
27	$\overline{\text{RT\_ADD\_ERR}}$
28	$\overline{\text{RT\_ADD\_LAT}}$
29	$\overline{\text{RT\_ADD\_P}}$
30	RTADD00 (LSB)
31	RTADD01
32	RTADD02
33	RTADD03
34	RTADD04 (MSB)
35	+5 VA
36	-15 VOLTS
37	$\overline{\text{GBR}}$

TABLE 4. BUS-65153 PIN DESCRIPTIONS	
PIN #	NAME
38	$\overline{\text{RTFAIL}}$
39	$\overline{\text{NBGRT}}$
40	RX/TX A
41	$\overline{\text{INCMD}}$
42	$\overline{\text{ME}}$
43	CLOCKSEL
44	$\overline{\text{RX/TX A}}$
45	$\overline{\text{RESET}}$
46	FACTORY TEST POINT
47	FACTORY TEST POINT
48	FACTORY TEST POINT
49	$\overline{\text{TXINH}}$
50	A13
51	CLOCK IN
52	A12
53	A11 (MSB)
54	A10
55	A09
56	A08
57	A07 (LSB)
58	A06
59	A05 (MSB)
60	A04
61	A03
62	A02
63	A01 (LSB)
64	A00
65	$\overline{\text{ILLEGAL}}$
66	$\overline{\text{SERVREQ}}$
67	$\overline{\text{SSFLAG}}$
68	$\overline{\text{BUSY}}$
69	$\overline{\text{DT\_REQ}}$
70	+5 VOLTS B

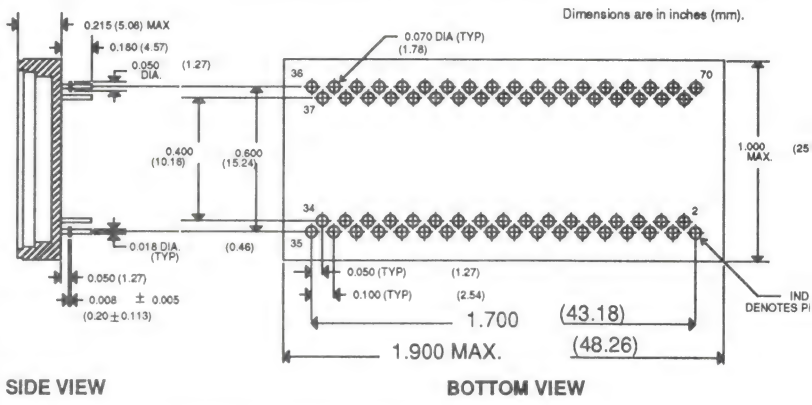


FIGURE 11. BUS-65153 MECHANICAL OUTLINE

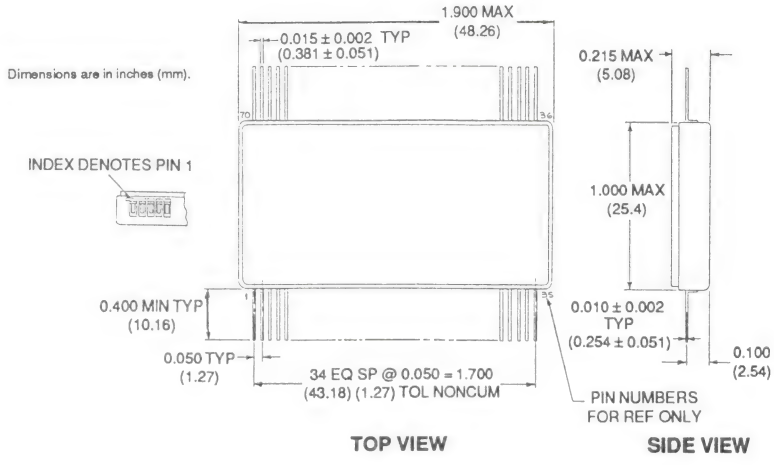

1.900 MAX (48.26)
0.015 ± 0.002 TYP (0.381 ± 0.051)
Dimensions are in inches (mm).
0.215 MAX (5.08)
INDEX DENOTES PIN 1
1.000 MAX (25.4)
0.400 MIN TYP (10.16)
0.010 ± 0.002 TYP (0.254 ± 0.051)
0.100 (2.54)
0.050 TYP (1.27)
34 EQ SP @ 0.050 = 1.700 (43.18) (1.27) TOL NONCUM
PIN NUMBERS FOR REF ONLY
TOP VIEW
SIDE VIEW

FIGURE 12. BUS-65163 MECHANICAL OUTLINE

ORDERING INFORMATION

BUS-65153 - X

Reliability Grade:
883B = Fully compliant 883B processing available.
B= 883B processing available but without QCI testing.
Blank = 0° to 70° C operation.

Package:
5 = Plug-in
6 = Flatpack

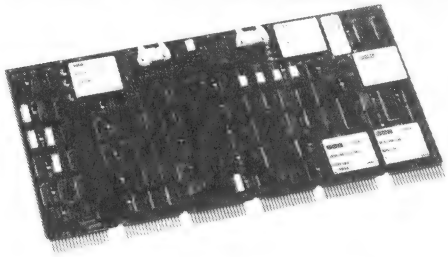
Data Bus Transformers:
For BUS-65153 use DDC BUS-25679 or B-2203 or M21038/12-02.

B-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-65505 AND BUS-65506

MIL-STD-1553B BC/RTU/MT UNIBUS® INTERFACE UNIT



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-65505 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B data bus and the DEC Unibus. The BUS-65505 Unibus Interface Unit (UBIU) can be operated as a 1553 bus monitor (MT), bus controller (BC) or remote terminal (RTU). The UBIU's 1553 data bus mode of operation is under the control of the subsystem processor's software. The BUS-65505 is packaged on one multilayer printed circuit card conforming to Unibus size specifications and complies fully with MIL-STD-1553B; supporting 12 mode codes, all message formats and complete wraparound Built-In-Test capability.

The BUS-65505 is easy and flexible to use. User overhead is reduced by the onboard 4K x 16 memory, vectored interrupt priority and bus grant levels.

Unit mode and operation are under subsystem control with functional and electrical compatibility with Unibus specifications.

Double buffering the UBIU's onboard memory prevents partially updated data from being read by the subsystem processor or transmitted to the 1553 data bus. The BUS-65505 will store, respond to and transmit up to 119 messages, depending on the mode of operation selected.

All MIL-STD-1553B functions: address recognition, Manchester coding validation, bit count and mode code response are provided transparent to and without user subsystem intervention.

FEATURES

- *COMPLETE DUAL REDUNDANT INTELLIGENT BC/RTU/MT WITH UNIBUS INTERFACE*
- *SUPPORTS ALL MIL-STD-1553B MESSAGE FORMATS AND 12 MODE CODES*
- *4K x 16 DUAL PORT RAM STORES: 60 BC MESSAGES PLUS ADDRESS STACK, POINTER AND MESSAGE COUNT; 119 RTU MESSAGES PLUS COMMAND WORDS AND POINTERS; 16 MT DATA AREAS AND POINTER*
- *STANDARD ONE HEX HEIGHT UNIBUS CARD*
- *UNIBUS NON-PROCESSOR REQUEST DMA TRANSFERS*
- *COMPLETE WRAP AROUND BUILT-IN-TEST*

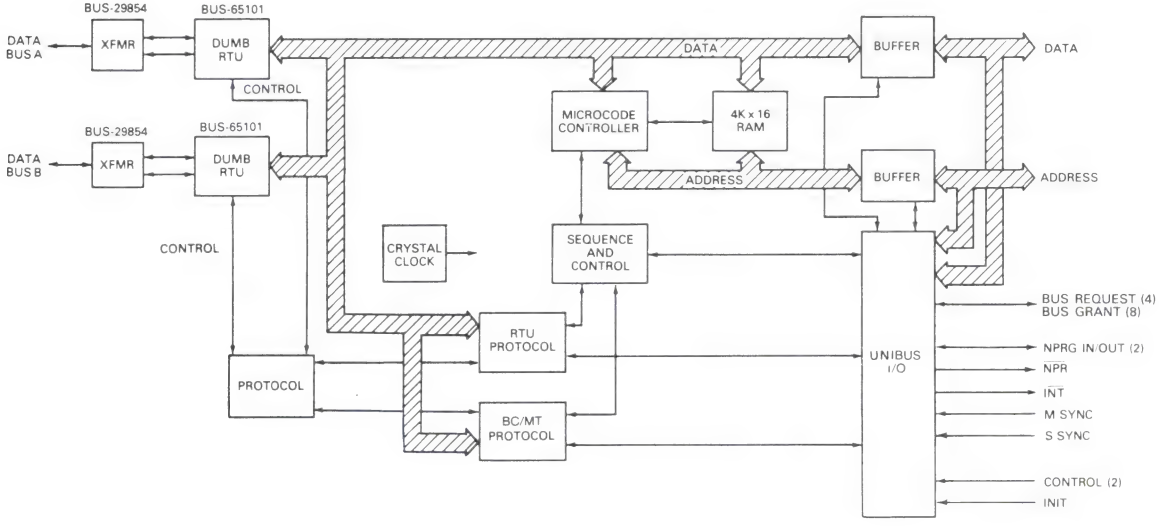
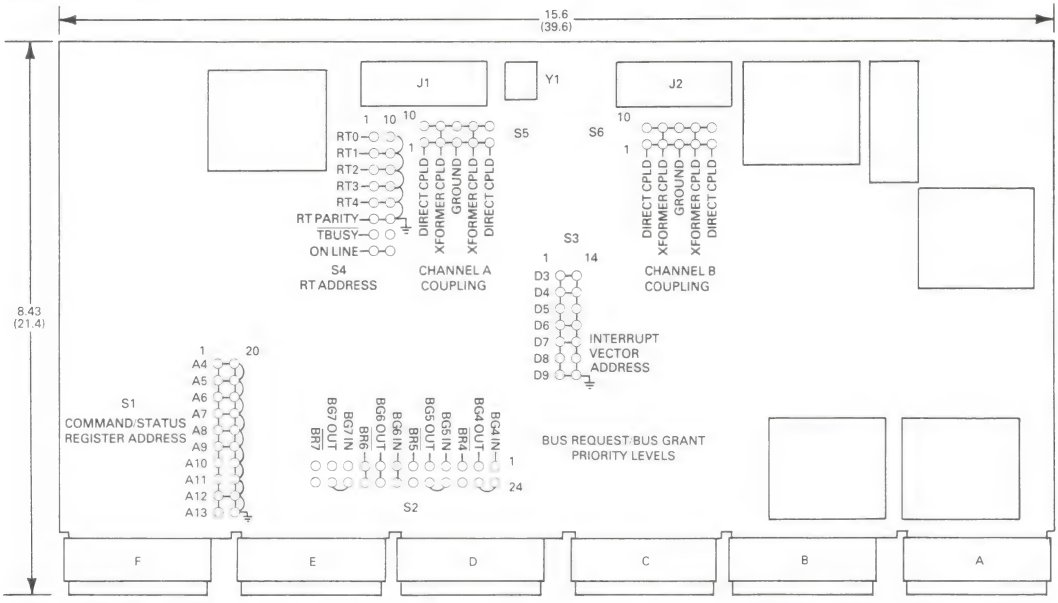


FIGURE 1. BUS-65505 BLOCK DIAGRAM

®Unibus is a Registered Trademark of Digital Equipment Corporation.

Dimensions are in inches (cm).



Notes:

(1) Command Status Register address bits A14-A17 are non-selectable and set to logic "1". Bits A4-A13 are user selectable.

(2) Interrupt Vector Address bits, D0, D1, and D10 through D15 are non-selectable and set internally to logic "0". D2 indicates the type of interrupt: CSR1 or CSR2, (1 = interrupt received, 0 = no interrupt active).

(3) The UBIU is shipped factory strapped for:
1553 Channel A = XFMR Coupled
1553 Channel B = XFMR Coupled
Remote Terminal Address = 01
Command/Status Register Address = 111 110 110 000 00- ---
Interrupt Vector = 0 000 000 100 100 -00
Interrupt Priority Level = 6

(4) Pin Definitions

Pin No.	J1 Connector Connection
J1/1	BUS A POS
J1/3	
J1/5	BUS A NEG
J1/2	FRAME GROUND
J1/4	FRAME GROUND
J1/6	FRAME GROUND

Pin No.	J2 Connector Connection
J2/1	BUS B POS
J2/3	
J2/5	BUS B NEG
J2/2	FRAME GROUND
J2/4	FRAME GROUND
J2/6	FRAME GROUND

FIGURE 12. MECHANICAL OUTLINE AND JUMPER CONFIGURATIONS

ORDERING INFORMATION

BUS-65505

Power Supply Option:
5 = ±12VDC supplies
6 = ±15VDC supplies

Mating J1/J2 1553 connectors supplied with card:
2 each – BERG 65846-007 (connector housing)
12 each – BERG 47712 (associated terminals)

For Driver Software contact:

Digital Equipment Corporation
1901 West 14th Street
Tempe, Az. 85281-6983

Contact: Ms. Darla Lasky
602/894-4751

Part No. DDC VAX UNIBUS DRIVER

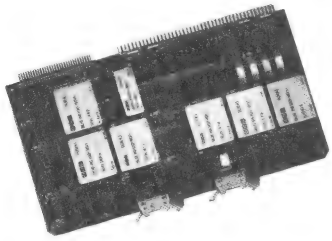
Reference DDC Part Nos.:
P/N 5500-0609-0001 Magnetic Tape
P/N 5500-0611-0001 Cassette
P/N 5500-0610-0001 Floppy Disk

F-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-65508 AND BUS-65509

MIL-STD-1553B BC/RTU/MT MULTIBUS® INTERFACE UNIT



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-65508 provides full, intelligent interfacing between the dual redundant MIL-STD-1553B serial data bus and the Intel Multibus (IEEE-796). The BUS-65508 Multibus Interface Unit (MBIU) can be operated as a 1553 bus monitor (MT), bus controller (BC) or remote terminal (RTU). The MBIU's 1553 data bus mode of operation is under the control of the subsystem processor's software. The BUS-65508 is packaged on one multi-layer printed circuit card conforming to Multibus size specifications and complies fully with MIL-STD-1553B; supporting 12 mode codes, all message formats and complete wrap-around Built-In-Test capability.

The BUS-65508 is easy and flexible to use. User overhead is reduced by the onboard 4K x 16 memory and six types of user interrupts. Unit mode and operation are under subsystem control with functional and electrical compatibility with Multibus specifications.

Double buffering the MBIU's onboard memory prevents partially updated data from being read by the subsystem processor or transmitted to the 1553 data bus. The BUS-65508 will store, respond to and transmit up to 119 messages, depending on the mode of operation selected.

All MIL-STD-1553B functions: address recognition, Manchester coding validation, bit count and mode code response are provided transparent to and without user subsystem intervention.

FEATURES

- *COMPLETE DUAL REDUNDANT INTELLIGENT BC/RTU/MT WITH MULTIBUS INTERFACE*
- *SUPPORTS ALL MIL-STD-1553B MESSAGE FORMATS AND 12 MODE CODES*
- *4K x 16 RAM STORES: 59 BC MESSAGES PLUS ADDRESS STACK AND POINTER; 119 RTU MESSAGES PLUS COMMAND STACK AND POINTER; 16 MT DATA AREAS AND POINTER*
- *6.75" x 12" MULTIBUS CARD*
- *SEVEN COMMAND REGISTERS*
- *INTERRUPT LEVEL SELECTABLE TO ANY OF THE EIGHT MULTIBUS INTERRUPTS*
- *WRAPAROUND BUILT-IN-TEST CAPABILITY*

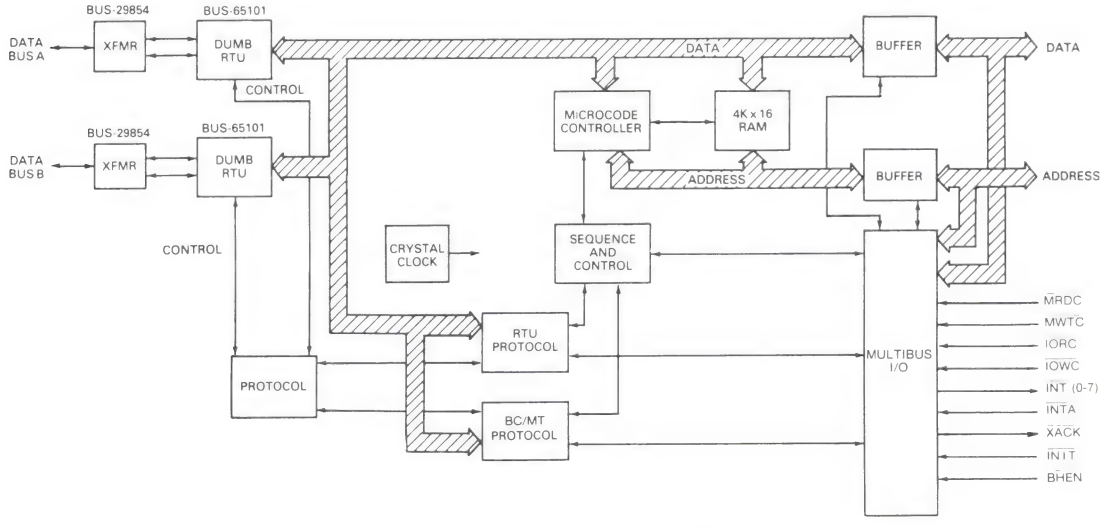


FIGURE 1. BUS-65508 BLOCK DIAGRAM

®Multibus is a Registered Trademark of Intel Corporation.

TABLE 1. BUS-65508 SPECIFICATIONS		
Values at nominal power supply voltages.		
PARAMETER	**UNITS**	**VALUE**
LOGIC		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See Pin Function & Loading Table
V_{OH}	V	2.5 min
V_{OL}	V	0.4 max
V_{IH}	V	2.4 min
V_{IL}	V	0.8 max
POWER SUPPLIES		
+5V Supply		
Voltage Tolerance	%	10
Current Drain	A	4.0 max
+15V Supply*		
Voltage Tolerance	%	5
Current Drain	mA	300 max
−15V Supply*		
Voltage Tolerance	%	5
Current Drain	mA	300 max
TEMPERATURE RANGE (Case)		
Operating**	°C	0 to +70
Storage	°C	−65 to +150
SIZE	in (cm)	6.75×12.0×0.6 max (17.2×30.5×0.157)

*BUS-65508 uses ±15V supplies and BUS-65509 uses ±12V supplies.
**Consult factory for wider operating temperature range.

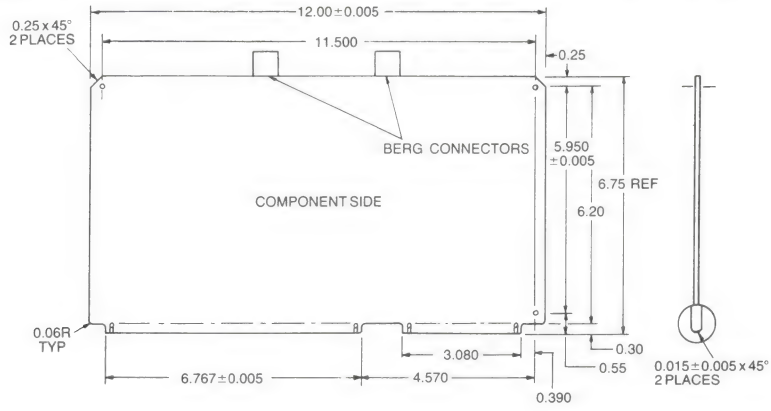


FIGURE 19. BUS-65508 MECHANICAL OUTLINE

ORDERING INFORMATION

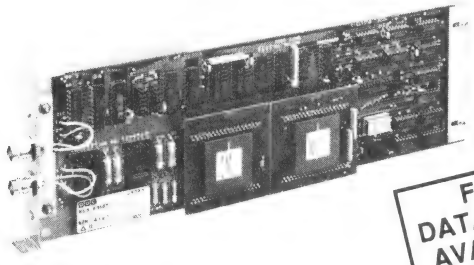
BUS-65508

Power Supply Option:
8 = ±15VDC supplies
9 = ±12VDC supplies

Mating J1/J2 1553 connectors supplied with card:
2 each – BERG 65846-007 (connector housing)
12 each – BERG 47712 (associated terminals)

F - ABR

MIL-STD-1553 BC/RTU/MT IBM PC® INTERFACE UNIT



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-65515 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the IBM PC Bus. Software controls the BUS-65515's operation as either a 1553 Bus Controller (BC), Remote Terminal Unit (RTU), or Bus Monitor (MT).

The BUS-65515 is packaged on one full size IBM PC printed circuit card. Its onboard 4K x 16 dual access RAM is double buffered, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus.

Additional features include a dynamic wrap-around Built-In-Test (BIT), onboard Time Tag Counter, jumper programmable interrupt level and BUS-65515 RTU address selection. The BUS-65515 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for dynamic simulation applications.

FEATURES

- *IBM PC INTERFACE WITH INTELLIGENT BC/RTU/MT*
- *STANDARD IBM PC CARD SIZE*
- *SUPPORTS ALL 1553B DUAL REDUNDANT MESSAGE FORMATS AND MODE CODES*
- *DYNAMIC WRAP-AROUND BUILT-IN TEST*
- *ON-BOARD TIME TAG COUNTER*
- *DEDICATED 4K x 16 DUAL ACCESS RAM*
- *DOUBLE BUFFER MEMORY ARCHITECTURE TO INSURE DATA INTEGRITY*
- *MEMORY MAPPED INTERFACE*
- *SOFTWARE PROGRAMMABLE RTU ADDRESS AND DATA BLOCK ALLOCATIONS*
- *JUMPER PROGRAMMABLE INTERRUPT LEVEL SELECTION*

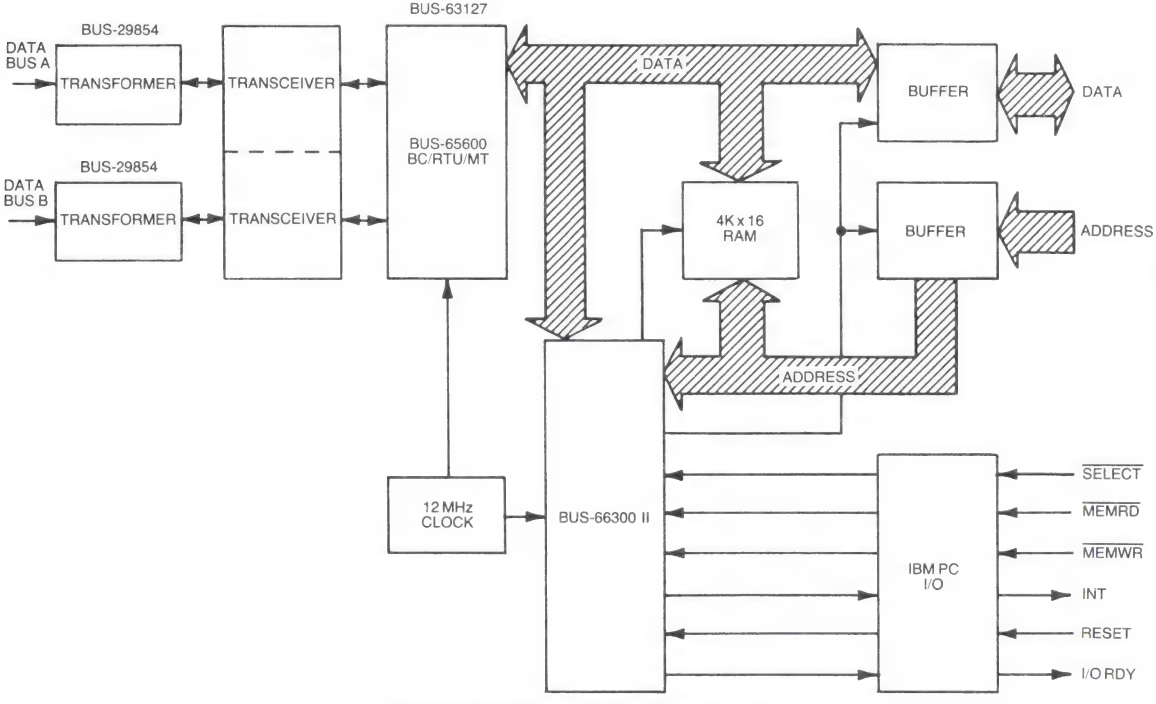


FIGURE 1. BUS-65515 BLOCK DIAGRAM

®IBM is a registered trademark of International Business Machines Corporation.

TABLE 10. BUS-65515 PIN FUNCTIONS		
PIN	SIGNAL NAME	DESCRIPTION
A1	IO CHCK	Not Used
A2	D7	Data Bit 7 (MSB)
A3	D6	Data Bit 6
A4	D5	Data Bit 5
A5	D4	Data Bit 4
A6	D3	Data Bit 3
A7	D2	Data Bit 2
A8	D1	Data Bit 1
A9	D0	Data Bit 0
A10	IO CHRDY	I/O Ready
A11	AEN	Address Enable
A12	A19	Address Bit 19 (MSB)
A13	A18	Address Bit 18
A14	A17	Address Bit 17
A15	A16	Address Bit 16
A16	A15	Address Bit 15
A17	A14	Address Bit 14
A18	A13	Address Bit 13
A19	A12	Address Bit 12
A20	A11	Address Bit 11
A21	A10	Address Bit 10
A22	A9	Address Bit 9
A23	A8	Address Bit 8
A24	A7	Address Bit 7
A25	A6	Address Bit 6
A26	A5	Address Bit 5
A27	A4	Address Bit 4
A28	A3	Address Bit 3
A29	A2	Address Bit 2
A30	A1	Address Bit 1
A31	A0	Address Bit 0

TABLE 10. BUS-65515 PIN FUNCTIONS (Cont.)		
PIN	SIGNAL NAME	DESCRIPTION
B1	GND	Signal Ground
B2	RESET	Reset
B3	+5V	Logic Power Supply
B4	IRQ2	Interrupt Request 2
B5	−5V	Not Used
B6	DRQ2	Not Used
B7	−12V	System Power Supply
B8	Not Used	Not Used
B9	+12V	System Power Supply
B10	GND	Signal Ground
B11	−MEMW	Memory Write
B12	−MEMR	Memory Read
B13	−IOW	Not Used
B14	−IOW	Not Used
B15	−DACK3	Not Used
B16	DRQ3	Not Used
B17	−DACK1	Not Used
B18	DRQ1	Not Used
B19	−DACK0	Not Used
B20	CLK	Not Used
B21	IRQ7	Interrupt Request 7
B22	IRQ6	Interrupt Request 6
B23	IRQ5	Interrupt Request 5
B24	IRQ4	Interrupt Request 4
B25	IRQ3	Interrupt Request 3
B26	−DACK2	Not Used
B27	T/C	Not Used
B28	ALE	Address Latch Enable
B29	+5V	Logic Power Supply
B30	OSC	Not Used
B31	GND	Signal Ground

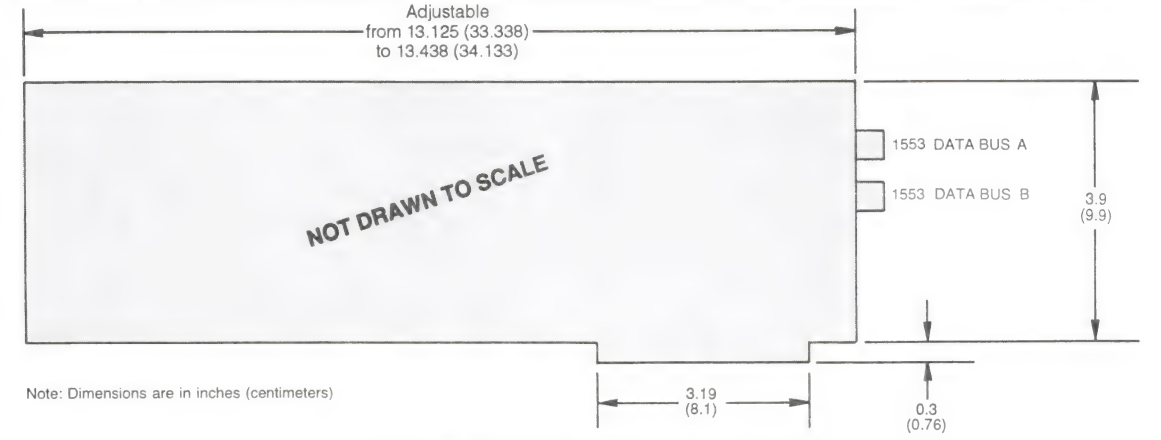


FIGURE 35. BUS-65515 MECHANICAL OUTLINE

ORDERING INFORMATION BUS-65515

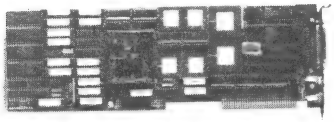
SOFTWARE

- Contact factory for free Software P/N BUS-69052
- Contact P.T.I.

Phase Two Industries
4800 Great America Parkway
Suite 400
Santa Clara, CA 95054
Phone (408) 986-8801
Fax (408) 986-0646

For driver and application Software (PC-AID-D): Mr. Andy Werbach

IBM PC® COMPATIBLE MIL-STD-1553 SIMULATOR AND TESTER CARD



FULL DATA SHEET AVAILABLE

DESCRIPTION

DDC's BUS-65517II is a versatile, full size IBM PC printed circuit card designed for the test and simulation of MIL-STD-1553 systems. It provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553 data bus and the IBM PC. The user friendly software allows the BUS-65517II to simultaneously simulate a Bus Controller (BC), multiple Remote Terminal Units (RTUs), and/or a selectable, triggerable Bus Monitor (MT). The BUS-65517II may be either direct or transformer coupled to an external 1553 bus for use with user provided 1553 devices.

The BC and RTUs evaluate each 1553 message in real-time, determining if any format errors have occurred. Separate registers are maintained for the last command word and the last status word of each emulated RTU. In addition, the user may inject errors into any 1553 message issued by the emulated BC or RTUs. These errors include word count, bit count, zero crossing, parity, and, in the case of emulated RTUs, response errors (including the setting of any bit within the particular RTU's status word).

The intelligent MT captures the 1553 bus traffic. The user can define when MT operation is to begin and which messages (based on the RTU address, T/$\overline{R}$ bit, and subaddress) are to be, captured. Monitored information is displayed on a message by message basis.

Operation requires an IBM PC or compatible (with DOS 2.1 or higher), 640K RAM, BUS-65517II card, and DDC provided software. Optional software is available to allow the BUS-65117II RTUs to respond within the timing constraints of MIL-STD-1553A. An optional driver allows the user to control the operation of the BUS-65517II through Turbo Pascal or Microsoft "C". These features make the BUS-65517II an excellent choice for dynamic simulation of MIL-STD-1553B systems.

FEATURES

- *SIMULATION AND TEST OF MIL-STD-1553 SYSTEMS*
- *SIMULTANEOUS EMULATION OF BC, UP TO 31 RTUs, AND MT*
- *MT MODE RECONSTRUCTS 1553 BUS TRAFFIC*
- *ERROR INJECTION/DETECTION CAPABILITIES*
- *USER FRIENDLY SOFTWARE*
- *OPTIONAL RT PRODUCTION TEST PLAN SOFTWARE*
- *OPTIONAL 1553A RESPONSE AND REAL-TIME DRIVER SOFTWARE AVAILABLE*

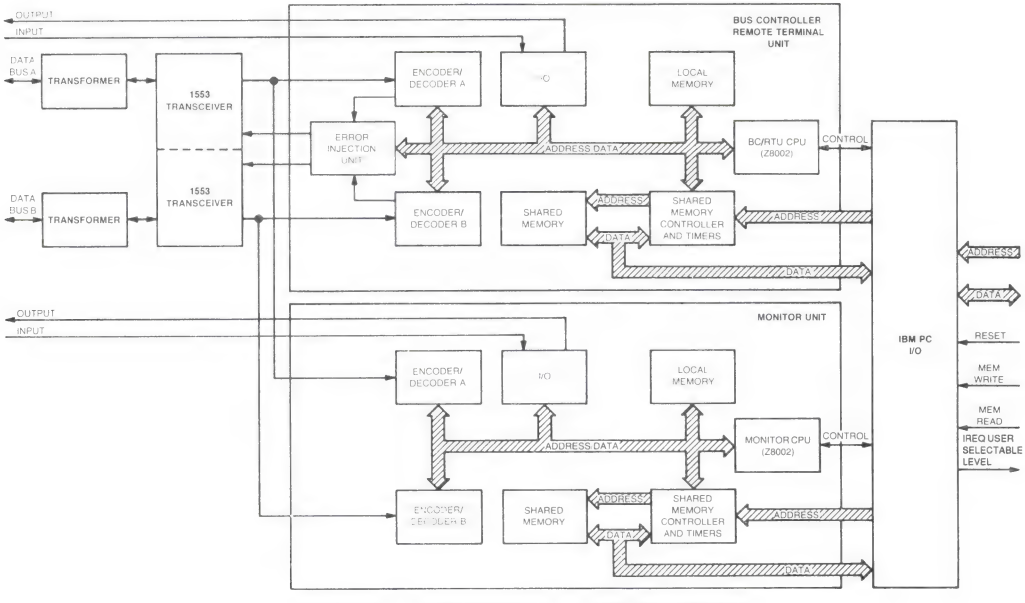


FIGURE 1. BUS-65517II BLOCK DIAGRAM

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Note: Dimensions are in inches (centimeters)

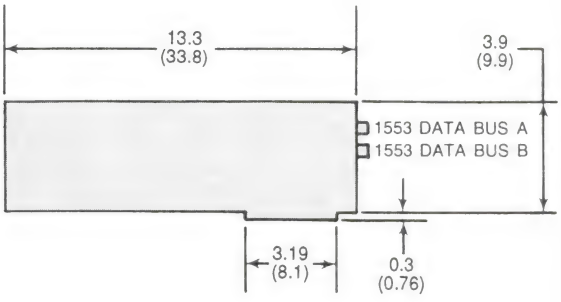


FIGURE 7. BUS-65517II MECHANICAL OUTLINE

ORDERING INFORMATION

BUS-65517II MIL-STD-1553 Simulator and Tester Card, includes menu software.

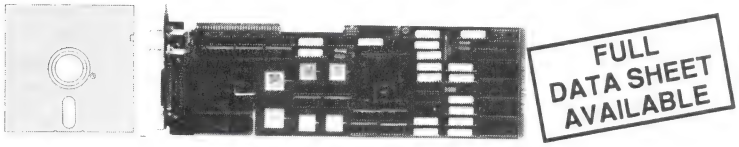
BUS-690XXII

Software Upgrades:

- 08 = MIL-STD-1553B Real Time Software and "C" Driver
- 09 = MIL-STD-1553A&B Real Time Software and "C" Driver
- 18 = MIL-STD-1553B Real Time Software and Pascal Driver.
- 19 = MIL-STD-1553A&B Real Time Software and Pascal Driver.
- 23 = MIL-STD-1553A&B Real Time Software, Pascal & "C" Drivers, and RT Production Test Plan Software.
- 24 = MIL-STD-1553A&B Real Time Software, Pascal & "C" Drivers, and RT Production Test Plan Software, **plus** Validation Test Plan Software.

Call the technical support number listed below for additional literature.

MIL-STD-1553 RT PRODUCTION TEST PLAN PROTOCOL TESTING SOFTWARE & HARDWARE



DESCRIPTION

The BUS-65519 is a turnkey system used to automate the protocol tests of the SAE RT Production Test Plan. A number of military contracts are imposing this test plan on MIL-STD-1553 suppliers.

With the BUS-65519, the test engineer characterizes the Unit Under Test (UUT) via the user friendly, menu driven software. Once this is done, the configuration can be saved to disk. The BUS-65519 can execute the ENTIRE production test plan in under 20 seconds. A report detailing the results of the test is automatically generated.

The BUS-65519 reduces the time required to generate customize test software from an estimated 3 months, to less than 10 minutes.

The product consists of an IBM PC MIL-STD-1553 interface card, an optional parallel I/O card to generate static inputs to the UUT (see ordering information), and the menu driven software.

FEATURES

- *IMPLEMENTS COMPLETE SAE RT PRODUCTION TEST PLAN PROTOCOL TESTS (PTP) INCLUDING NOTICE II TESTS*
- *COMPLIES WITH LATEST PTP SAE RELEASE AS4112*
- *COMPLETES TEST IN LESS THAN 20 SECONDS*
- *DISK STORAGE OF PTP-SUBSET AND RT CONFIGURATIONS*
- *USER FRIENDLY MENU DRIVEN DISPLAYS WITH HELP SCREENS*
- *RUNS ON IBM PC/XT/AT OR COMPATIBLE*
- *INCLUDES BUS-65517II "C" AND PASCAL LIBRARIES*
- *OPTIONAL DISCRETE I/O BOARD (CONTROL RT ADDRESS AND STATUS BITS)*

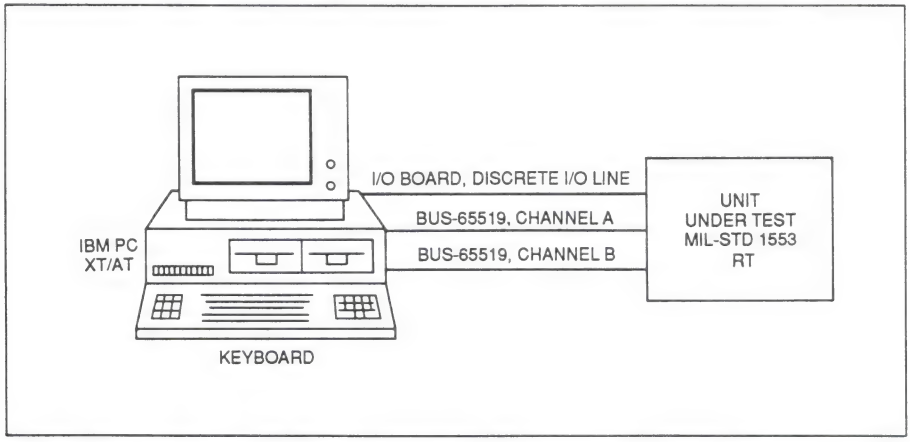


FIGURE 1. BUS-65519 OPERATING ENVIRONMENT

J

REPORTS MENU

This menu sends a report to either the disk or printer. The user may specify N for NO RESULTS, F for FAILED RESULTS, or A for ALL RESULTS.

FILE MENU

This menu allows the user to save or load a previously saved PTP-subset and RTU configuration to or from a disk. This provides the user a convenient way of setting up a variety of products to be tested.

RUN MENU

After the user has gone through all the setup menus or selected a previous file, this selection will run all tests selected in the TEST MENU. As each test is being run, it will be displayed on the screen and if any errors occur they will also be displayed.

RESULTS MENU

After all the tests are completed, the Results menu will display a list (see FIGURE 10) of all tests with any failures that had occured.

```
**********************************************

              Production Tests

**********************************************

Bus A   Bus B        Test

Pass             5.2.1.1.1        Valid RT Address
Pass             5.2.1.1.2        Invalid RT Address
Pass             5.2.1.2          Word Count
Pass             5.2.1.3          Subaddress
Pass             5.2.1.4          Error Injection
Pass             5.2.2.1          Dual Redundant Operation
Pass             5.2.2.2.6.1      Dual Redundant Shutdown and Overrides
N/A              5.2.2.2.6.2      Selective Bus Shutdown and Overrides
```

FIGURE 10. RESULTS MENU

ORDERING INFORMATION

BUS-65519 - Includes MIL-STD-1553 Tester (BUS-65517II) and Production Test Plan Software.

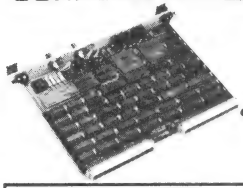
BUS-65520 - Includes MIL-STD-1553 Tester (BUS-65517II) and Production Test Plan Software, **plus** Validation Test Plan Software.

Optional parallel I/O Card (PIO-12) - Available from
METRABYTE 440 Myles Standish Blvd., Taunton, MA 02780
(508) 880-3000

D-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-65522II, 65523II, & 65524



NEW

FULL DATA SHEET AVAILABLE

MIL-STD-1553B BC/RT/MT VME/VXI INTERFACE UNIT

DESCRIPTION

The BUS-65522II/65523II/65524 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the parallel VMEbus and VXIbus. Software controls the BUS-65522II's operation as either a MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT).

The BUS-65522II VME/VXI board is packaged on one double eurocard size printed circuit card. Its on-board 8K X 16 of dual access RAM is double buffered, preventing partially updated data from being read by the VME/VXI host or transmitted to the 1553 Data Bus. The CPU can access any part of the shared RAM as needed.

All MIL-STD-1553 functions: address recognition, Manchester coding and parity validation, bit count, and mode code response are provided without host processor intervention. The BUS-65522II contains eleven VME/VXI and 1553 registers which allow the VME/VXI host to configure its operation under software control.

The BUS-65522II supports four groups of vectored interrupts. A custom interrupt may be programmed by means of an on-board PROM. The interrupt request logic may be software controlled as to enable/disable, priority level and 8-bit vector.

Additional features include an on-line built-in loop test, Time Tag counter, software programmable base memory address, and RT address. The BUS-65522II supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for real-time applications.

FEATURES

- *VMEbus/VXIbus Interface*
- *Standard Double Eurocard Size*
- *BUS-65524 Ruggedized Option Available*
- *8K X 16 On-board Dual Access RAM*
- *D16 Data Transfers*
- *A16/A24, A16/A32 Jumper Selectable*
- *On-board Time Tag Counter*
- *On-board Memory Management*

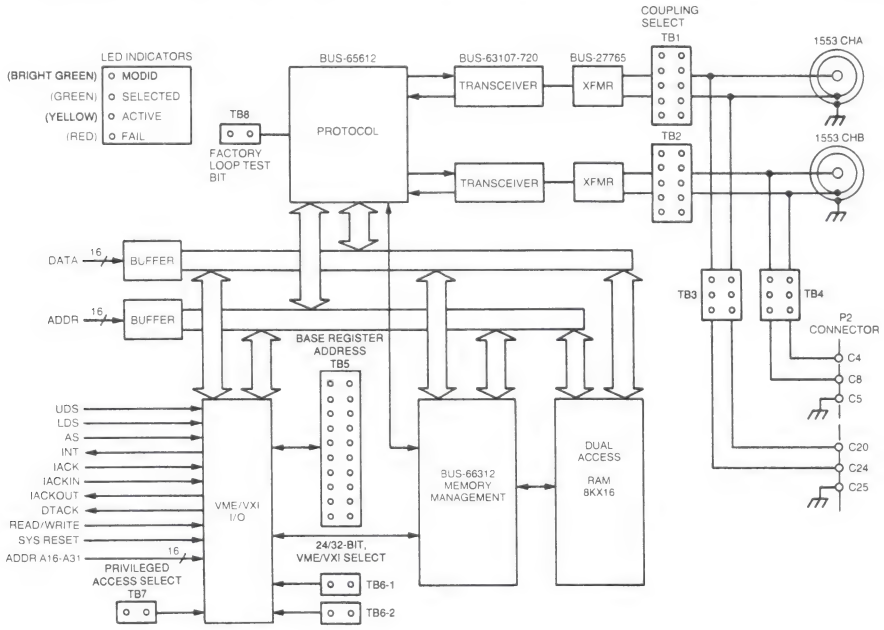


FIGURE 1. BUS-65522II BLOCK DIAGRAM

J

TABLE 16. BUS-65522II & BUS-65523II P2 PIN CONNECTIONS					
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1		B1	+5V	C1	
A2		B2	GND	C2	
A3		B3		C3	
A4		B4	A24	C4	BUS B POS
A5		B5	A25	C5	BUS B SHEILD
A6		B6	A26	C6	
A7		B7	A27	C7	
A8		B8	A28	C8	BUS B NEG
A9		B9	A29	C9	
A10		B10	A30	C10	
A11		B11	A31	C11	
A12		B12	GND	C12	
A13		B13	+5V	C13	
A14		B14		C14	
A15		B15		C15	
A16		B16		C16	
A17		B17		C17	
A18		B18		C18	
A19		B19		C19	
A20		B20		C20	BUS A NEG
A21		B21		C21	
A22		B22		C22	
A23		B23		C23	
A24		B24		C24	BUS A POS
A25		B25		C25	BUS A SHEILD
A26		B26		C26	
A27		B27		C27	
A28		B28		C28	
A29		B29		C29	
A30		B30		C30	
A31		B31	GND	C31	
A32		B32	+5V	C32	

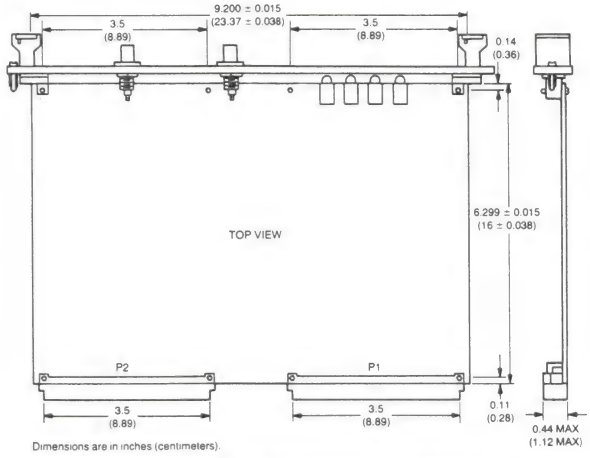


FIGURE 40. MECHANICAL OUTLINE

ORDERING INFORMATION

BUS-6552X

Board Configuration:

2II = Trapezoidal Transceiver (1553 B), 0 to 70°C

3II = Sinusoidal Transceiver (MACAIR), 0 to 70°C

4 = Ruggedized Board, with Trapezoidal Transceiver (1553 B), -55 to +125°C

BUS-69053 **free** Microsoft "C" Run Time library of routines available which supports VME/1553 application software.

For additional information, please contact the Data Bus Applications Group at 1-800-DDC-1772 x234.

In New York State, (516) 567-5600 x234.

A-ABR

VMEbus-to-STANAG 3838/3910 INTERFACE CARD FOR BC/MULTI-RT/MT

Advance Information

DESCRIPTION

The BUS-65525 provides a complete interface between a VMEbus backplane and a dual redundant STANAG 3838/3910 low-speed/high-speed (LS/HS) bus. The BUS-65525 consists of a double height (6.3" X 9.2") intelligent VME slave device and an external fiber optic transceiver. The board provides capability for operating as a STANAG 3838 (low-speed) Bus Controller (BC), Remote Terminal (RT), or Monitor (MT). In addition, the board provides complete capability to operate as a 20 Mbps STANAG 3910 (high-speed) RT.

The BUS-65525 features DDC's BUS-61560 Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er), the BUS-63910 Fiber Optic Front End (FOF), the BUS-63920 STANAG 3910 Data Retiming Unit (DRU), the BUS-63930 STANAG 3910 RT Protocol Unit, and 64K words of 3910 (high-speed) message RAM.

The VME board portion of the BUS-65525 is register and memory mapped, allowing full selection and control of the STANAG 3838/3910 operating modes and control of memory management, base memory address, 3838/3910 RT address, and interrupt control. The architecture of the board supports flexible operation of the board for both interrupt-driven and polling applications.

For its front-end interface, the board has a 21-position D-connector. The D-connector supports a direct interface to the BUS-63910 dual STANAG 3910/EFAbus fiber optic transceiver (included). Alternatively, the BUS-65525 may be interfaced to a BUS-60000-635 STANAG 3910 electrical (50 ohm coax) transceiver.

The BUS-65525 includes built-in self-test features for both the low-speed and high-speed sections. The flexible memory-mapped architecure of the BUS-65525 makes it an ideal choice for real-time simulation, test, and system integration applications.

Features

- ***STANAG 3838/3910/EFAbus Compliant.***
- ***Includes Board Assembly and Fiber Optic Transceiver; Also Supports Electrical Transceiver Applications***
- ***A24 Memory, A16 Register Mapped, D16 Double Height VME Board.***
- ***BUS-61560 STANAG 3838/MIL-STD-1553B Notice 2 AIM-HY'er .***
- ***Comprehensive STANAG 3910 Clock/Data Recovery and High-Speed RT Protocol .***
- ***On-Board RAM: 8K Words Low-Speed; 64K Words High-Speed.***
- ***On-Board Self-Test***

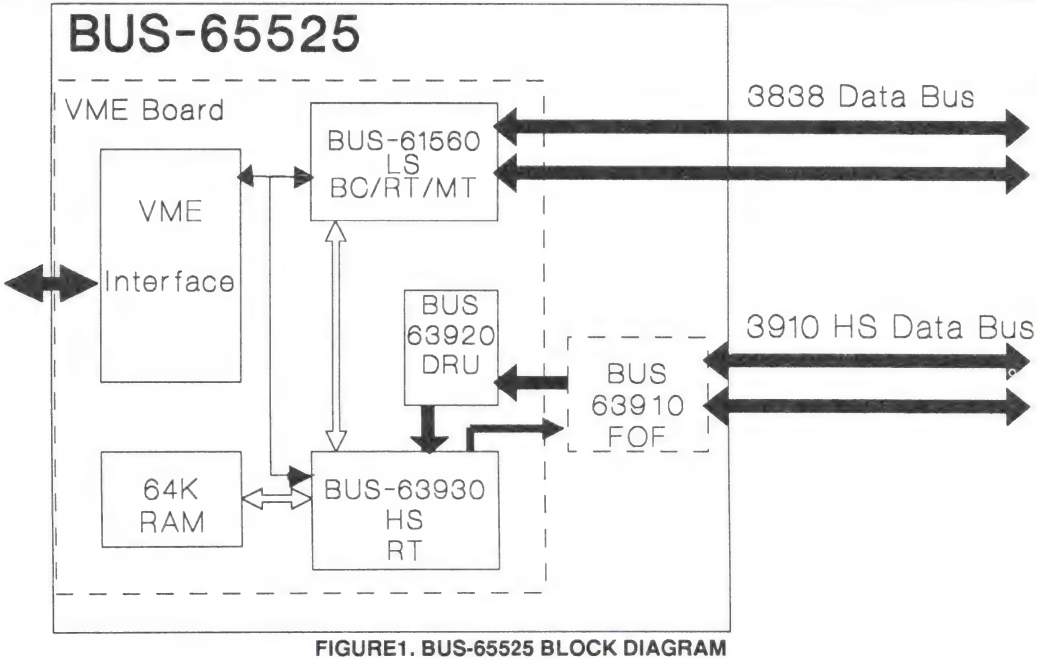


FIGURE1. BUS-65525 BLOCK DIAGRAM

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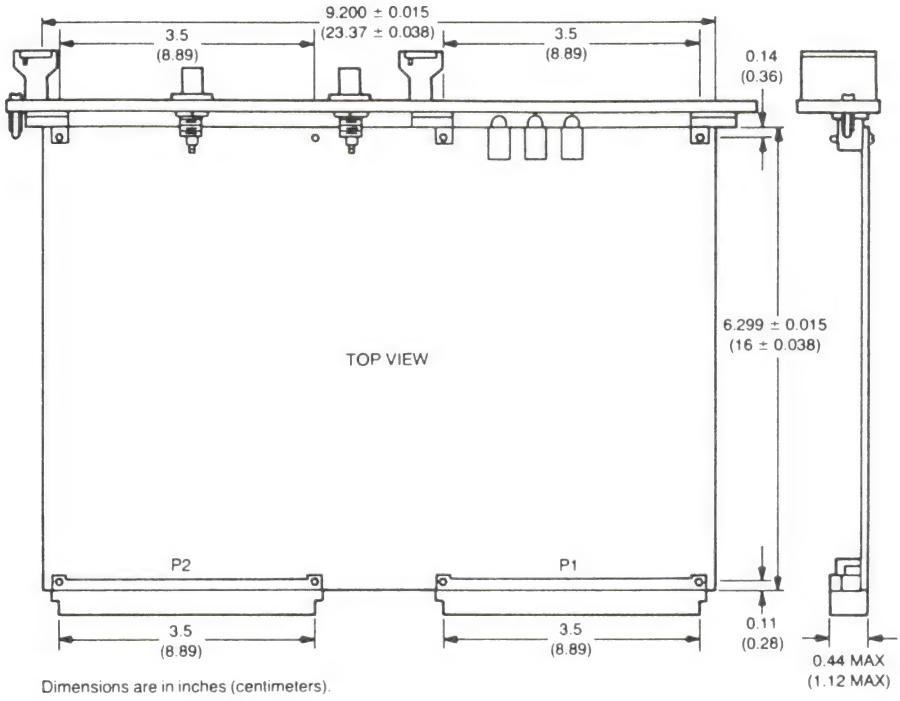


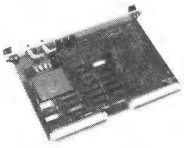
FIGURE 2. BUS-65525 MECHANICAL OUTLINE

ORDERING INFORMATION

BUS-6552X

- 5 = STANAG 3838/3910 Board
- 6 = STANAG 3838 (MIL-STD-1553B) Board

A



VMEbus-to-MIL-STD-1553B NOTICE 2 INTERFACE BOARD

PRELIMINARY

DESCRIPTION

The BUS-65526 provides a complete interface between a VMEbus backplane and a dual redundant MIL-STD-1553B Notice 2 bus. The board comprises a double height (6.3" X 9.2") intelligent VME slave device, operating in 1553 Bus Controller (BC), Remote Terminal (RT), or Monitor (MT) modes.

The BUS-65526 features DDC's BUS-61560 Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). As such, it includes dual transceiver and encoder/decoder, complete 1553B protocol, 8K x 16 words of on-board RAM, and complete memory management for all three modes.

The board includes a set of ten on-board registers. These registers allow selection of the 1553 operating modes and control of memory management, base memory address, 1553 RT address, and interrupt control.

On-board Interrupt Mask and Interrupt Status Registers support flexible operation for both interrupt and polling type applications.

The memory management scheme for RT mode provides an option for separation of broadcast data plus a circular buffer option for individual RT subaddresses to off-load the VME host CPU.

Additional features of the BUS-65526 include RT command illegalization and a free "C" software subroutine library, the BUS-69058. The illegalization scheme allows RT Commands Words to be illegalized as a function of T/$\overline{R}$ bit, subaddress and word count/mode code. The flexible memory-mapped architecture of the BUS-65526 makes it an ideal choice for real-time simulation, test, and system integration applications.

Features

- ***Complete 1553B Notice 2 BC/RT/MT***
- ***STANAG 3838 Compliant***
- ***A24 Memory Mapped, 8K x 16 On-Board RAM***
- ***Advanced RT Memory Management Features***
- ***Interrupt Status and Time Tag Registers***
- ***On-Board Self-Test***
- ***Free Software Library Available***

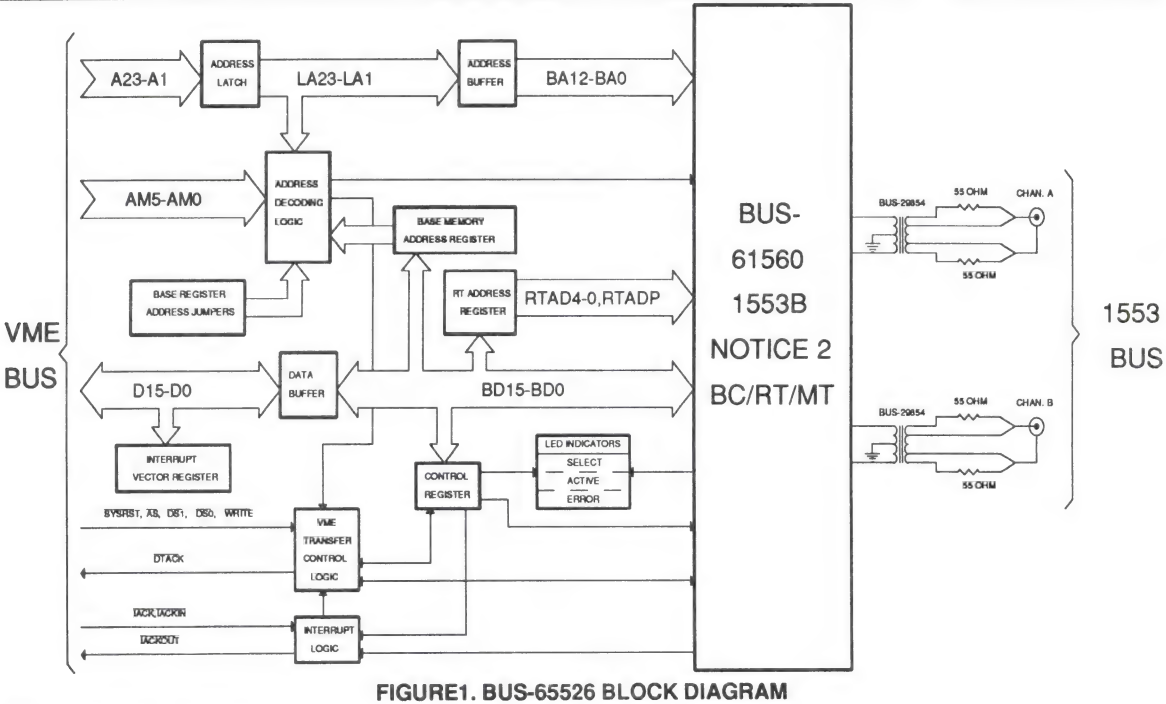


FIGURE1. BUS-65526 BLOCK DIAGRAM

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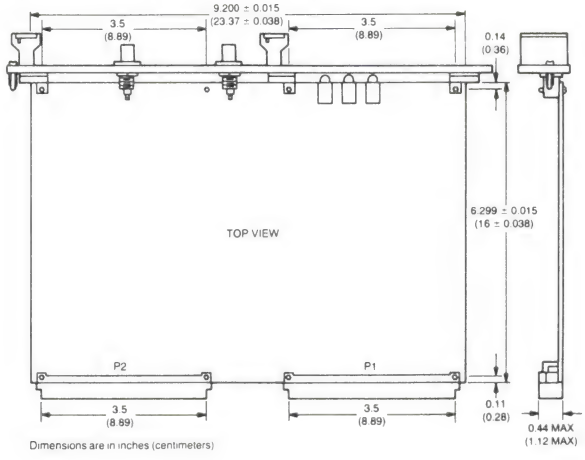


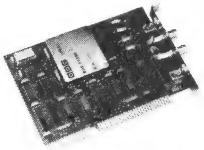
FIGURE 2. BUS-65526 MECHANICAL OUTLINE

ORDERING INFORMATION

BUS-65526
└ +5V/-12V Board

BUS-69058 "C" Software Library Package

A



FULL DATA SHEET AVAILABLE

MIL-STD-1553 BC/RT/MT IBM PC/AT® INTERFACE UNIT

DESCRIPTION

The BUS-65529 provides full, intelligent interfacing between a dual redundant MIL-STD-1553B Data Bus and the IBM PC/AT Bus. Software controls the BUS-65529's operation as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT).

The BUS-65529 is packaged on a half size IBM PC/AT printed circuit card. The board features DDC's BUS-61560 Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). As such, it includes dual transceiver and encoder/decoder, complete 1553B protocol, 8K words of shared RAM and memory management logic for all three modes.

The board includes a set of ten onboard registers. These registers allow selection of the 1553 operating modes and control of memory management, base memory address, 1553 RT address, and interrupt control.

Background Mode Operation prevents inadvertent access to the card during power-on self-test.

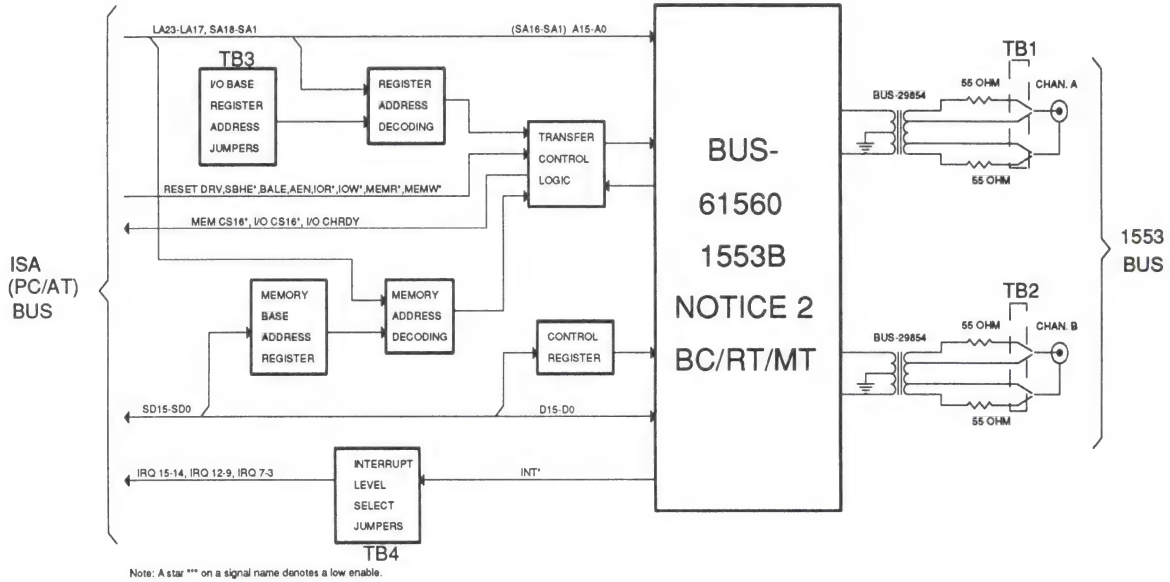
On-board Interrupt Mask and Interrupt Status Registers support flexible operation for both interrupt and polling applications.

The memory management scheme for RT mode provides an option for separation of broadcast data plus a circular buffer option for individual RT subaddresses to offload the PC host CPU.

Additional features include a wrap-around Built-In-Test, jumper programmable interrupt level, software programmable RT address selection and a free C software subroutine library, the BUS-69054. The BUS-65529 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for real-time simulation, test, and system integration applications.

FEATURES

- *1/2 Size IBM PC/AT ISA Compatible 16 Bit Interface Card*
- *1553B Notice 2 Dual Redundant BC\RT\MT (STANAG 3838 Compliant)*
- *Built-In-Test (BIT)*
- *8K x 16 Shared RAM*
- *Software Programmable RT Address, Data Block Allocations, Interrupts, and Illegalization*
- *Selectable Interrupt Level*
- *Low Power*
- *Background Mode Operation*
- *Free Library Software Available*



Note: A star "*" on a signal name denotes a low enable.

FIGURE 1. BUS-65529 BLOCK DIAGRAM

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JUMPER CONFIGURATION

TB1: 1553 CHANNEL A. Connection selected by jumpers at TB1.
TB2: 1553 CHANNEL B

Pin#	Coupling Type
1	DIRECT COUPLED
2	TRANSFORMER COUPLED*
3	CENTER TAP*
4	TRANSFORMER COUPLED*
5	DIRECT COUPLED

NOTE: * Installed by factory.

TB3: I/O BASE ADDRESS. The BUS-65529 is I/O mapped to the CPU. The user must know the I/O map of the PC that they are using to find an available address. (Adding a jumper sets the selected address bit to a logic "0".)

Pin#	Address
1	SA9
2	SA8
3	SA7*
4	SA6
5	SA5

NOTE: * Installed by factory
(DEFAULT I/O ADDRESS = 0360).

TB4: Interrupt Level Select. The BUS-65529 allows the user to select the Interrupt Request output from among IRQ levels 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15. To select the desired interrupt request line, connect the pin corresponding to the desired interrupt level.

PIN#	Hardware Interrupt Level
1	IRQ 9 Highest Priority
2	IRQ 10
3	IRQ 11
4	IRQ 12
5	IRQ 14
6	IRQ 15
7	IRQ 3
8	IRQ 4
9	IRQ 5
10	IRQ 6
11	IRQ 7 Lowest Priority

ORDERING INFORMATION

BUS-65529
Software:
BUS-69054 FREE "C" Library Software (included)

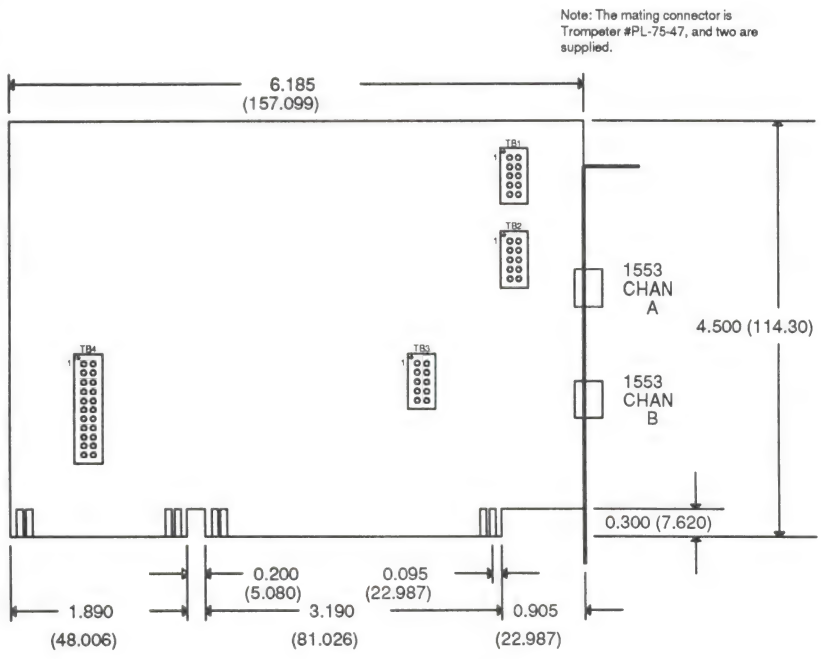


FIGURE 22. MECHANICAL OUTLINE (with jumper locations)

B-ABR

BUS-65535

VME/VXI MIL-STD-1553 SIMULATOR AND TESTER CARD

Advance Information

DESCRIPTION

DDC's BUS-65535 is a versatile, "B" size (6 x 9") VME/VXI printed circuit card designed for the test and simulation of MIL-STD-1553 systems. With an architecture based on the popular BUS-65517II IDEA board for the IBM PC/XT/AT, the card provides full, intelligent interfacing between a dual redundant MIL-STD-1553 data bus and a VME/VXI backplane. The BUS-65535 software library(provided), allows the card to simultaneously emulate a Bus Controller (BC), multiple Remote Terminals (up to 31 RTs), and/or a selectable, triggerable Bus Monitor (MT). The BUS-65535 includes provisions to be direct or transformer coupled to an external 1553 bus.

The board provides true BC/multi-RT emulation, while processing validating messages in real time, and maintains separate memory locations for the last Command Word and the last Status Word for each emulated RT.

In addition, the user may inject errors into any 1553 message issued by the emulated BC or RTs. These errors include word count, bit count, Manchester and sync encoding, gaps, zero crossing, inverse sync, and parity. In addition, for the emulated RTs the user may induce: late response errors, response on the wrong bus, and incorrect status bit errors.

The intelligent MT stores the 1553 bus traffic. The user can define conditions to initiate monitor storage and select which messages are to be stored, based on Command Word address, T/R bit, and subaddress. Thousands of messages can be stored in real-time.

The software library for the BUS-65535 consists of an extensive library of driver routines and is available in Microsoft C. DDC supports DOS and Unix 5.0. Contact DDC for additional operating system support software.

Features

- ***Simultaneous Emulation of BC, up to 31 RTs, and MT.***
- ***"B" Size, A32 or A24, A16, D16 VME/VXI Slave.***
- ***VXI Smart Register-Based Device with Self-Test.***
- ***Real-Time Subsystem Emulation.***
- ***Extensive Error Injection/Detection Capabilities.***
- ***Front Panel Status LEDs.***
- ***Discrete TTL Inputs & Outputs for Special Applications.***

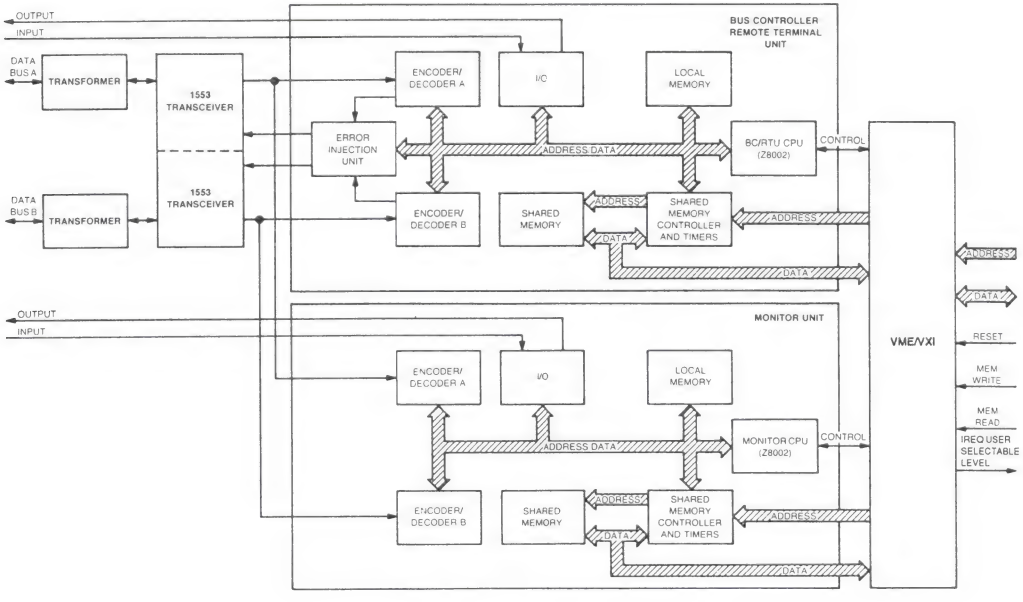


FIGURE1. BUS-65535 BLOCK DIAGRAM

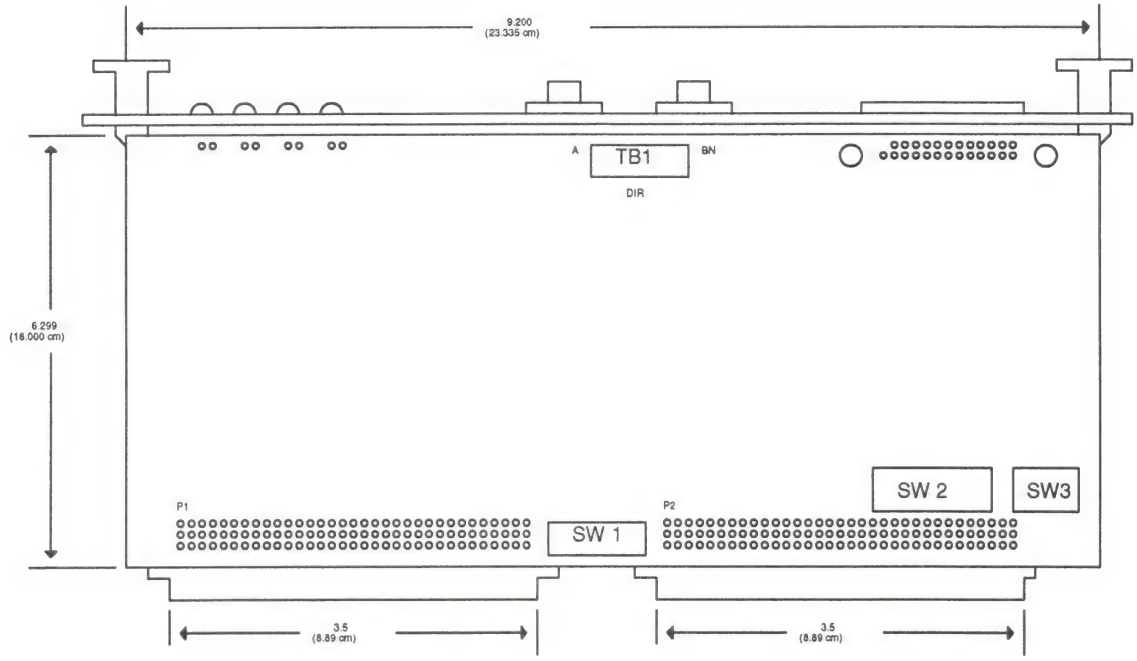


FIGURE 2. BUS-65535 MECHANICAL OUTLINE

ORDERING INFORMATION

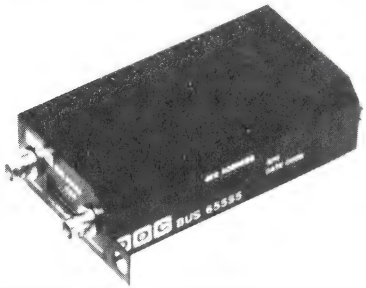
BUS-65535VME/VXI MIL-STD-1553 SIMULATOR AND TESTER CARD

BUS-69060"C" Run-Time Library Routines

A

BUS-65555

MIL-STD-1553 RTU/BC/MT MODULE FOR GRiD© RUGGEDIZED LAPTOP PC



DESCRIPTION

The BUS-65555 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the rugged GRiD 1520, 1530, and 1535 series laptop XT/AT® compatible computers. Software controls the BUS-65555's operation as either a 1553 Remote Terminal Unit (RTU), Bus Controller (BC), or Bus Monitor (MT).

The BUS-65555 is packaged in a GRiD internal battery cartridge so that it becomes an integral part of the computer. It offers the Dual 1553 ports through standard 1553 triaxial connectors. The module is equipped factory strapped for transformer coupling. Its on-board 8K x 16 dual access shared RAM is double buffered, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus. The base address of the registers and the onboard shared RAM is user selectable by DIP switches.

Additional features include a wrap-around on-line Built-In-Test, on-board message Time Tag Counter, RTU address register, Monitor word count register. The BUS-65555 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for dynamic simulation in the lab or for flight line applications. It can also be used as a software development tool for the AIM-HY series MIL-STD-1553 terminals.

FEATURES

- *MIL-STD-1553B RTU/BC/MT INTERFACE FOR GRiD 1520,1530, AND 1535 SERIES RUGGEDIZED LAPTOP PC'S*
- *SMALL SIZE & LOW POWER*
- *SUPPORTS ALL 1553B DUAL REDUNDANT MESSAGE FORMATS AND MODE CODES, OPTIONAL ILLEGIZATION PROM*
- *DYNAMIC WRAP-AROUND ON-LINE BUILT-IN-TEST*
- *ON-BOARD TIME TAG COUNTER & MT WORD COUNTER*
- *DEDICATED 8K x 16 DUAL ACCESS RAM*
- *SOFTWARE I/O REGISTERS*
- *MEMORY MAPPED INTERFACE*
- *SOFTWARE PROGRAMMABLE RTU ADDRESS AND DATA BLOCK ALLOCATIONS*
- *LEVEL 5, INTERRUPT PROVIDED*

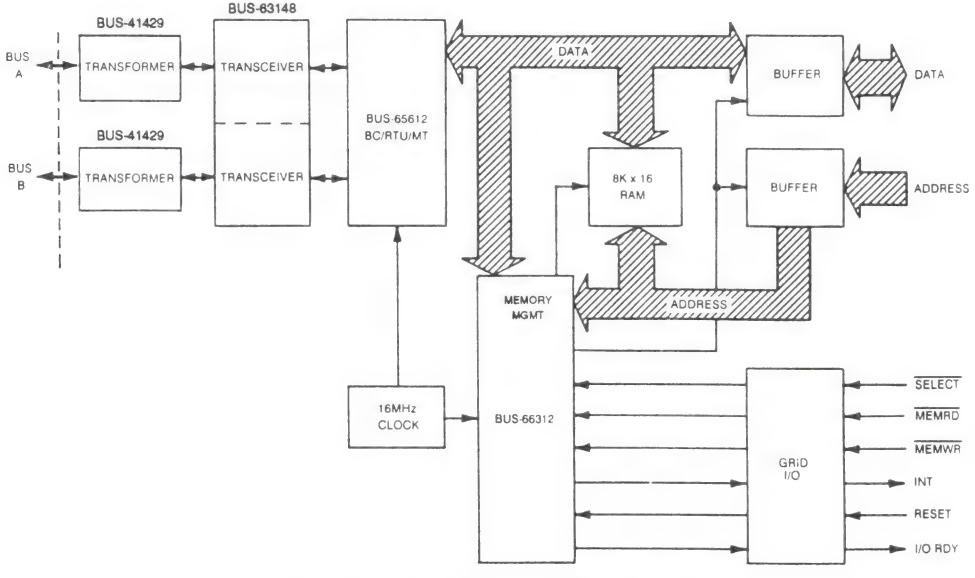


FIGURE 1. BUS-65555 BLOCK DIAGRAM

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© GRiD and GRiDCASE are registered trademarks of GRiD Systems Corporation

TABLE 1. BUS-65555 SPECIFICATIONS Specifications at nominal power supply voltages and 25°C.		
PARAMETERS	**UNIT**	**VALUE**
LOGIC	V	2.4
V_{OH}	V	0.4
V_{OL}	µA	40
I_{IH}	mA	1.6
I_{IL}		2
V_{IH}	V	0.6
V_{IL}	V	
POWER SUPPLIES		
Voltage,Current Drain	V,Amps	+5.0 +10% ,1.70 max
TEMPERATURE RANGE		
Operating (Case)	°C	0 to +70
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in (cm)	2.9 x 1.45 x 5.5 (7.4 x 3.7 x 13.97)

Table 3. SEGMENT ADDRESS SWITCH ASSIGNMENT	
SWITCH	**ADDRESS**
SW-1	A15*
SW-2	A16*
SW-3	A17*
SW-4	A18
* Preset to "ON" position, which selects C000. A15 selects segment C000 or C800.	

TABLE 2. REGISTERS/DECODER ADDRESS DEFINITION			
OFFSET BYTE ADDRESS IN HEX	**DEFINITION**	**R/W**	**CLEARED BY RESET COMMAND**
:4000	Interrupt Mask Register	R/W	YES
:4001	Illegal	–	–
:4002	Illegal	–	–
:4003	Configuration Register	R/W	YES
:4004	Illegal	–	–
:4005	Illegal	–	–
:4006	Start/Reset Register	W	–
:4007	Illegal		–
:4008	RTU Address Register	R/W	NO
:4009	Illegal	–	–
:400A	Time Tag Register (byte 0)*	R	YES
:400B	Time Tag Register (byte 1)*	R	YES
:400C	Interrupt Reset Command Register	W	YES
:400D	Illegal		–
:400E	External EOM Command Register	W	NO
:400F	Illegal	–	–
* in MT mode this becomes a 16 bit word count register.			

CONTACT FACTORY FOR:

1) Interactive Menu Driven Software

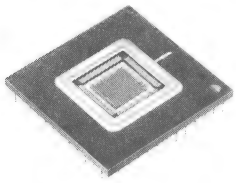
2) Operations Manual

ORDERING INFORMATION

BUS-65555

F

BUS-65612



MIL-STD-1553 BUS CONTROLLER REMOTE TERMINAL AND BUS MONITOR

CONTACT FACTORY FOR MORE INFORMATION

DESCRIPTION

The BUS-65612 is a 16 MHz single chip dual redundant MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT). Packaged in a Pin Grid Array (PGA), the BUS-65612 performs all the functions required to interface a MIL-STD-1553 dual redundant serial data bus transceiver, such as DDC's BUS-63125, and a subsystem parallel three-state data bus.

Using a single DDC custom monolithic SOS IC, the BUS-65612 features pin-for-pin and functional BUS-65600 compatibility, user initiated self-test, and low power consumption.

Compatible with most microprocessors, the BUS-65612 provides a 16 bit three-state parallel data bus and uses direct memory access (DMA type) handshaking for subsystem transfers.

All message transfer timing, DMA, and control lines are provided internally; thereby reducing the subsystem overhead associated with message transfers.

The BUS-65612 implements all dual redundant MIL-STD-1553 mode codes. In addition, any mode code may (optionally) be illegalized through the use of an external PROM. Complete error detection is provided by the BUS-65612 for BC and RTU operation. Error detection includes: response time-out, inter-message gaps, sync, parity, Manchester, word count, and bit count. The BUS-65612 is fully compliant with MIL-STD-1553 and operates over the full military temperature range of -55°C to +125°C - making it an excellent choice for MIL-STD-1553 applications.

FEATURES

- *COMPLETE BC, RTU, OR MT OPERATION*
- *16 MHz SINGLE CHIP BUS-65600 REPLACEMENT*
- *CMOS-SOS TECHNOLOGY*
- *PGA PACKAGES*
- *IMPLEMENTS ALL DUAL REDUNDANT MODE CODES*
- *SELECTIVE MODE CODE ILLEGALIZATION AVAILABLE*
- *BC CHECKS STATUS WORD FOR CORRECT ADDRESS AND SET FLAGS*
- *DMA HANDSHAKING FOR SUBSYSTEM MESSAGE TRANSFERS*
- *CONTINUOUS ON-LINE AND INITIATED BUILT-IN-TEST*

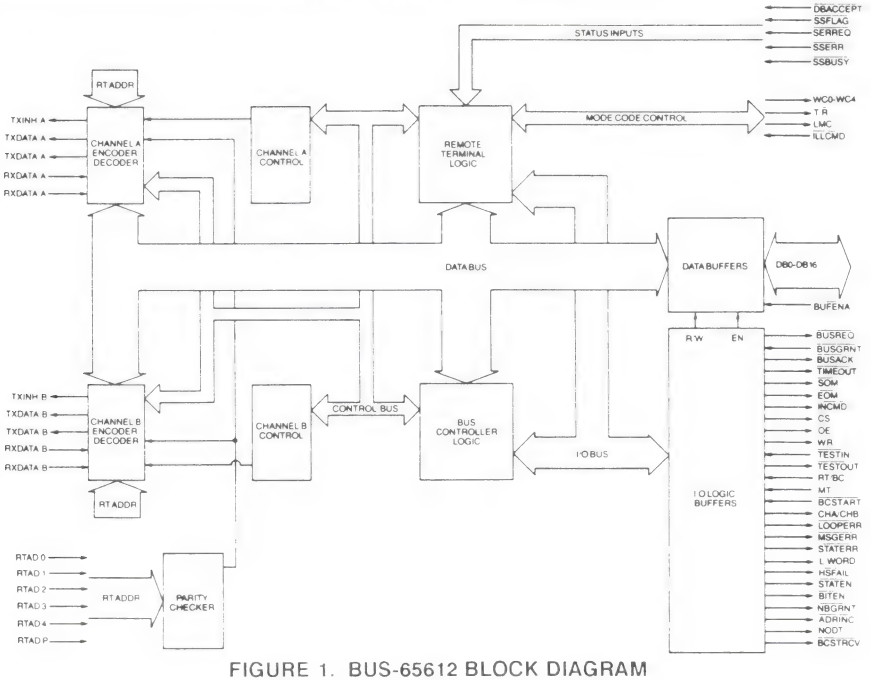


FIGURE 1. BUS-65612 BLOCK DIAGRAM

TABLE 1. BUS-65612 PIN FUNCTIONS (PGA)			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
A01	TIM2	C05	A RX
A02	A NBRQ	C06	TESTENA
A03	PCLK	C07	VSS
A04	A RX	C08	RTAD1
A05	B RX	C09	VDD
A06	PARENA	C10	BRO
A07	RTADPAR	C11	NW
A08	RTAD3	C12	LMC
A09	RTAD0	C13	SA3 MC3
A10	CLKRST	D01	DB10
A11	ND	D02	DB12
A12	VW	D03	DB15
A13	VA	D11	RTFAIL
B01	VDD	D12	SA2 MC2 B8
B02	LOOPERR	D13	SA0 MC0 B6
B03	RTPARERR	E01	DB08
B04	TEST1	E02	DB09
B05	B RX	E03	DB11
B06	BROENA	E11	SA1 MC1 B7
B07	RTAD4	E12	WC4 CWC4 B5
B08	RTAD2	E13	WC3 CWC3 B4
B09	CLK	F01	DB05
B10	TIM1	F02	DB06
B11	MC	F03	DB07
B12	CMD	F11	WC2 CWC1 B3
B13	SA4 MC4	F12	WC1 CWC1 B2
C01	DB13	F13	WC0 CWC0 B1
C02	DB14	G01	DB02
C03	TD	G02	DB04
C04	B NRBQ	G03	DB03

TABLE 1. BUS-65612 PIN FUNCTIONS (PGA) (Continued)			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
K03	A TX	N01	VSS
K11	BUFENA2	N02	TS0
K12	BUSGRNT	N03	LWORD
K13	ILLCMD	N04	OE
L01	B TX	N05	CS
L02	CYCENA	N06	INCMD
L03	MT	N07	ERROR
L04	TEST2	N08	ADRINC
L05	R/W	N09	BUSACK
L06	SOM	N10	BUSREQ
L07	EOM	N11	T/R
L08	CMDTRF	N12	GBR
L09	BITEN	N13	VSS
L10	STATEN	G11	WCMUXENA
L11	CSTINH	G12	VDD
L12	WRMASK	G13	SAMUXENA
L13	RESET	H01	DB01
M01	A TX	H02	DB00
M02	TS1	H03	TIMEOUT
M03	HSFAIL	H11	SVCRQST
M04	STATSET	H12	SEL2
M05	WR	H13	SSFLAG
M06	INCMD	J01	TACT
M07	ME	J02	CH B/A
M08	DTSTR	J03	A TXINH
M09	TIMERR	J11	RTFLAG
M10	DBACC	J12	ADBC
M11	NBGRNT	J13	SSBUSY
M12	RT/BC	K01	B TXINH
M13	BUFENA1	K02	B TX

ORDERING INFORMATION

BUS-65612-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 without QCI testing

Blank = Standard DDC procedures

Packaging: PGA (Pin Grid Array)

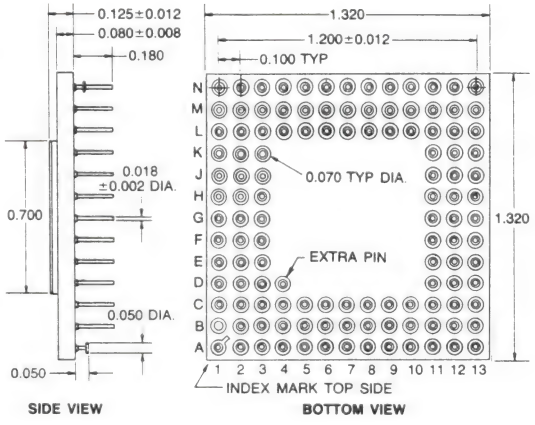
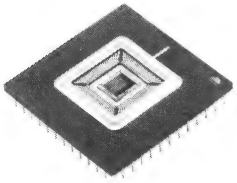


FIGURE 2. BUS-65612 MECHANICAL OUTLINE (PGA)

A

BUS-66312

MIL-STD-1553 TO MICROPROCESSOR INTERFACE UNIT



FULL DATA SHEET AVAILABLE

REFER TO BUS-61553 FOR MEMORY MANAGEMENT DESCRIPTION AND TIMING.

DESCRIPTION

DDC's BUS-66312 MIL-STD-1553 to Microprocessor Interface Unit simplifies the CPU to 1553 Data Bus interface while offloading the CPU. It is packaged in a small PGA hermetically sealed.

The BUS-66312 is designed to be used as an intermediary between the CPU and a MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU) or Bus Monitor (MT). The BUS-66312 provides a method for using a RAM accessible to both the CPU and the 1553 terminal. By using this shared RAM for operation, the CPU can transmit or receive 1553 traffic simply by accessing the shared memory.

The BUS-66312 allows all 1553 message transfers to be entirely memory or I/O mapped. Thus the CPU's interface to this device is simple and hardware and software interfacing is minimal. The BUS-66312 supports 1553 interface devices such as DDC's BUS-65149 dual Universal RTU or the BUS-65612 dual BC, RTU, and MT. By operating autonomously, the BUS-66312 reduces CPU overhead for maintaining the 1553 interface. Available screened to MIL-STD-883, the BUS-66312 is ideal for demanding military and industrial microprocessor to 1553 interface applications. The BUS-66312 operates over the full military -55°C to +125°C temperature range.

FEATURES

- *COMPATIBLE WITH MIL-STD-1750 CPUs*
- *COMPATIBLE WITH MOTOROLA, INTEL, AND ZILOG CPUs*
- *COMPATIBLE WITH DDC BUS-65612 BC/RTU/MT AND BUS-65149 UNIVERSAL RTU*
- *MINIMIZES CPU OVERHEAD*
- *SIGNAL CONTROLS FOR SHARED MEMORY IMPLEMENTATION*
- *TRANSFERS COMPLETE MESSAGES TO SHARED MEMORY*
- *PROVIDES MEMORY MAPPED 1553 INTERFACE*
- *IBM PC® DEVELOPMENT CARD (BUS-65515) AVAILABLE*

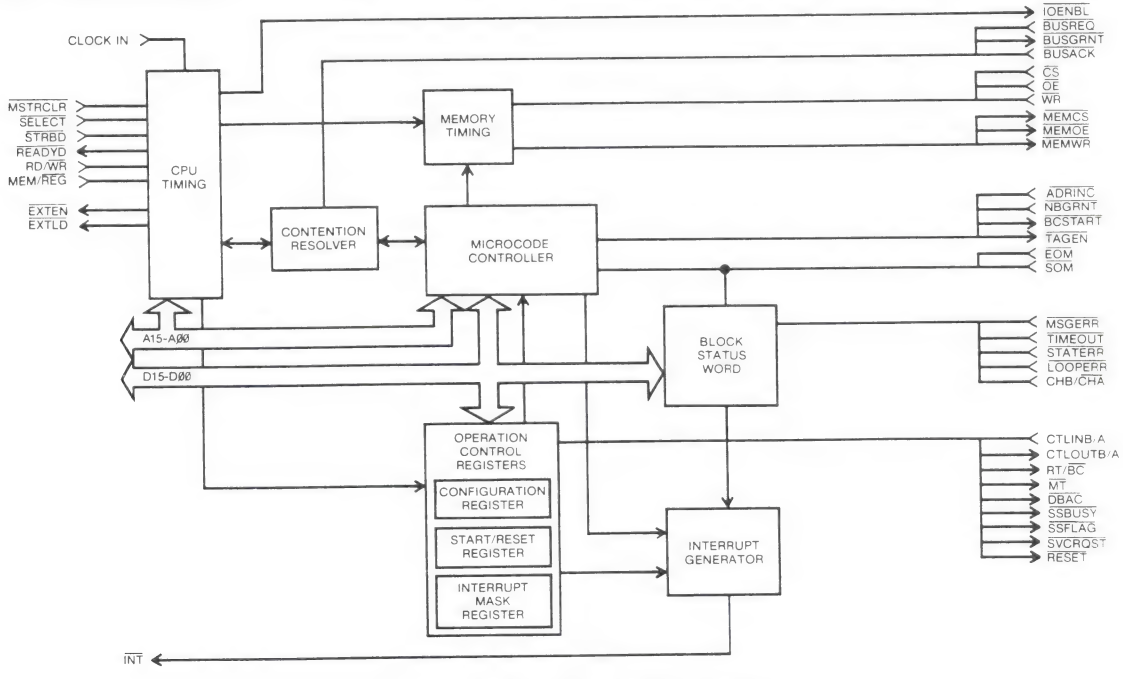


FIGURE 1. BUS-66312 BLOCK DIAGRAM

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PIN NO.	FUNCTION	PIN NO.	FUNCTION
A01	NC	G11	GND
A02	A09	G12	CTLOUTB/$\overline{A}$
A03	A08	G13	VCC
A04	A06	H01	D00
A05	A05	H02	D01
A06	A03	H03	GND
A07	A02	H11	$\overline{ADRINC}$
A08	GND	H12	CTLINB/$\overline{A}$
A09	$\overline{NBGRNT}$	H13	MEM/$\overline{REG}$
A10	$\overline{OE}$	J01	D02
A11	$\overline{MEMCS}$	J02	D03
A12	NC	J12	$\overline{STATERR}$
A13	$\overline{CS}$	J13	$\overline{MSGERR}$
B01	NC	K01	D04
B02	GND	K02	D05
B03	NC	K12	$\overline{SOM}$
B04	A07	K13	$\overline{RESET}$
B05	GND	L01	VCC
B06	VCC	L02	D07
B07	A00	L06	D13
B08	$\overline{ADRDIR}$	L07	$\overline{DDIR}$
B09	$\overline{MEMWR}$	L08	$\overline{IOENBL}$
B10	$\overline{MEMOE}$	L12	$\overline{EOM}$
B11	NC	L13	$\overline{BCSTART}$
B12	GND	M01	D06

PIN NO.	FUNCTION	PIN NO.	FUNCTION
B13	$\overline{BUSGRNT}$	M02	GND
C01	A11	M03	D08
C02	A10	M04	D10
C06	A04	M05	D12
C07	A01	M06	D14
C08	$\overline{MT}$	M07	VCC
C12	$\overline{WR}$	M08	RD/$\overline{WR}$
C13	$\overline{BUSACK}$	M09	GND
D01	A13	M10	$\overline{EXTEN}$
D02	A12	M11	$\overline{INT}$
D12	$\overline{BUSREQ}$	M12	GND
D13	$\overline{MSTRCLR}$	M13	VCC
E01	A15	N01	NC
E02	A14	N02	NC
E12	$\overline{LOOPERR}$	N03	D09
E13	$\overline{TIMEOUT}$	N04	D11
F01	$\overline{SSBUSY}$	N05	GND
F02	$\overline{DBAC}$	N06	D15
F03	RTU/$\overline{BC}$	N07	$\overline{SELECT}$
F11	CLOCKOUT	N08	$\overline{STRBED}$
F12	CLKSEL	N09	$\overline{READYD}$
F13	CLOCKIN	N10	$\overline{EXTLD}$
G01	$\overline{SSFLAG}$	N11	CHB/$\overline{CHA}$
G02	VCC	N12	$\overline{TAGEN}$
G03	$\overline{SVCRQST}$	N13	NC

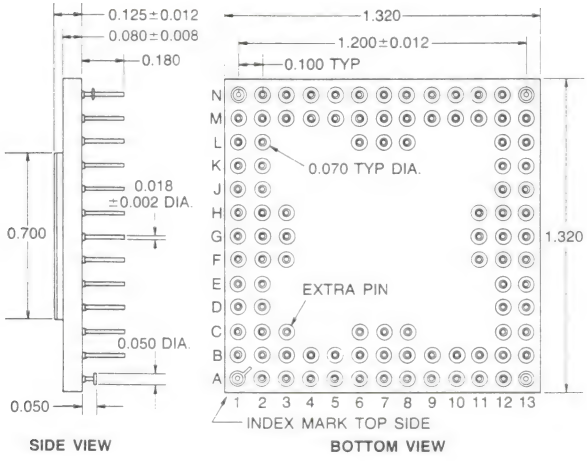


FIGURE 8. BUS-66312 MECHANICAL OUTLINE

D-ABR

ORDERING INFORMATION

BUS-66312-883B

Reliability Grade:

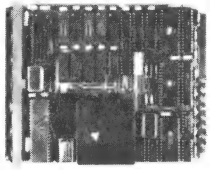
883B = Fully compliant with MIL-STD-883

B = Screened to MIL-STD-883 but without QCI testing.

Blank = Blank = 0° to 70° C

DDC
ILC DATA DEVICE CORPORATION

BUS-67007



MIL-STD-1750A CPU SEM E CARD WITH MIL-STD-1553 RTU/BC/MT

DESCRIPTION

The BUS-67007, Microcomputer SEM E card, provides a general purpose, single chip, 16 bit CMOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support conforming to the MIL-STD-1750A instruction set architecture. The PACE 1750A microcomputer and on-board 32K x 16 of EPROM offers the user an embedded system controller that can be used as a generic 1750A processor with a full, intelligent dual redundant MIL-STD-1553 RTU/BC/MT terminal. Its RS-422 port facilitates software development and system integration.

The BUS-67007 is packaged on a standard SEM E card with a 150 pin connector. Its on-board 8K x 16 SRAM supports the 1750A CPU. The separate internal 8K x 16 dual access shared RAM of the BUS-61555 AIM-HY supports the 1553B messages, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus. The AIM-HY off-loads the microprocessor from the tasks of 1553 communication protocol and offers the host additional RAM for program or data.

The card is equipped with 8 L.E.D.'s which gives visual BIT feedback as to the CPU self-test, unrecoverable errors, software errors, RS-422 status, EPROM status, SRAM status, 1553 terminal self-test status, and the CPU watch-dog timer status. The BUS-67007, requires 5 volt DC power, with a total power dissipation under 5 watts.

FEATURES

- *MIL-STD-1750A CPU CARD (PACE MICROPROCESSOR) AND MIL-STD-1553 TERMINAL (BUS-61555, 5V AIM-HY)*
- *16K WORDS RAM, 32K WORDS EPROM ON CARD*
- *RS-422 PORT FOR SOFTWARE DEVELOPMENT AND DEBUG*
- *VISUAL BIT (8 L.E.D.s)*
- *LOW POWER, < 5 WATTS, +5 VDC*

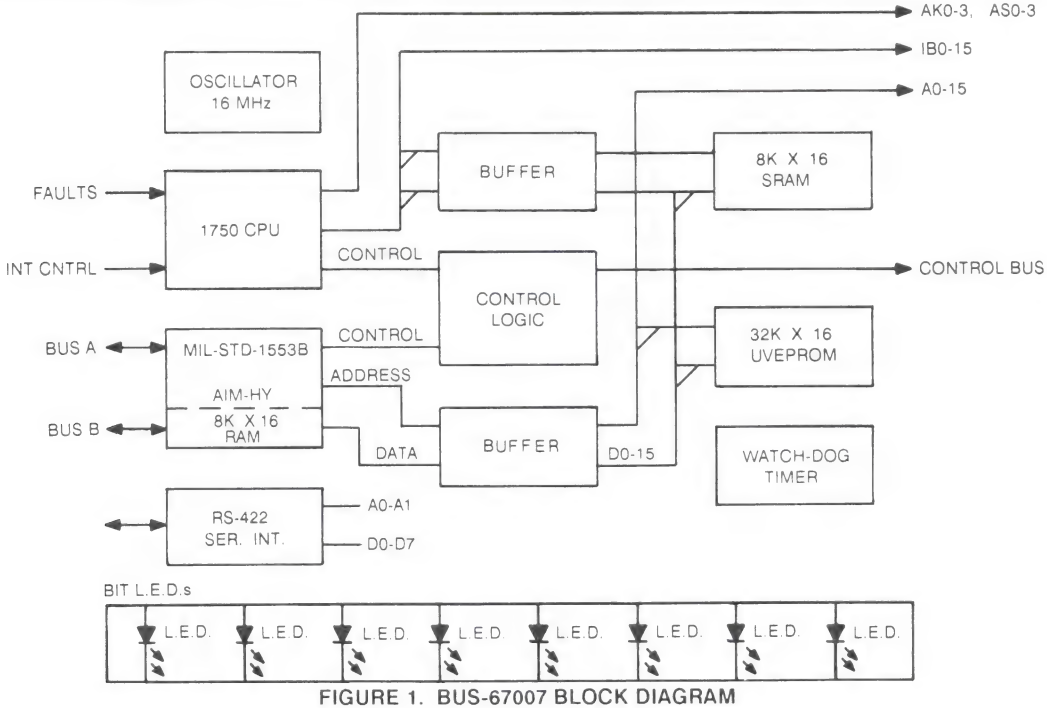


FIGURE 1. BUS-67007 BLOCK DIAGRAM

J

TABLE 1. PIN-OUTS

SIGNAL NAME	TYPE	PIN NUMBER	DESCRIPTION
IB0 - IB15	I/O	6,56,7,57,8,9,59,60,11,61, 12,62,17,63,125,126	INFORMATION BUS MULITPLEXED ADDRESS AND DATA USED AS DATA BUS OFF MODULE.(IB0 = MSB) TRI-STATE
A0 - A15	O	139,138,24,74,25,75,26,76,20 ,70,21,71,22,72,23,73	ADDRESS BUS (A15 = MSB) TRI-STATE
AK0 - AK3 AS0 - AS3	O	105,106,107,108 111,112,113,114	EXTENDED ADDRESS BUS TRI-STATE
PA0 - PA7 PB0 - PB7 PC0 - PC2	I/O	34,33,32,31,81,82,83,84 48,49,131,100,99,98,47 146,44,45,97	PARALLEL I/O PA0 - PB7 CAN BE DEFINED AS INPUT OR OUTPUT BY 8 BITS. PC0 - PC2 OUTPUT ONLY
16CLKOUT 1.8MOUT 100KHZ 8MCLK-1MCLK	O	85 86 27 128,28,78,79	16 MHz CLOCK OUTPUT BAUD RATE CLOCK OUTPUT 100KHz OUTPUT 8,4,2,1 MHz CLOCK OUTPUTS (SYNCHRONOUS)
IOINT1,IOINT2 INT2 - INT5 PDINT	I	14,13 66,65,16,64 122	I/O INTERRUPTS GENERAL INTERRUPTS POWER DOWN INTERRUPT
CONREQ-	I	2	CONSOLE REQUEST ACTIVE LOW
BSGNT-	I	3	INDICATES THAT THIS 1750A MAY USE THE BUS
M_IO	O	4	INDICATES MEMORY OR I/O ACCESS
RDYD	I	5	INDICATES DATA CYCLE IS READY TO TERMINATE
RDYA	I	55	INDICATES ADDRESS CYCLE IS READY TO TERMINATE
D_I	O	54	INDICATES A DATA OR INSTRUCTION ACCESS
TRGRST-	O	53	PULSED RESET FROM 1750A PROGRAM CONTROL (ACTIVE LOW)
BSLOCK-	I/O	52	INDICATES THAT THE BUS CANNOT BE ACCESSED (ACTIVE LOW)
SNEW	O	51	INDICATES AN OPCODE FETCH FROM 1750A
RESET-	O	104	SYSTEM RESET OUTPUT (ACTIVE LOW)
DAEN-	I	69	TRI-STATE CONTROL FOR DATA BUS (ACTIVE LOW)
STRBD-	O	58	DATA STROBE (ACTIVE LOW)
STRBA	O	67	ADDRESS STROBE (ACTIVE HIGH)
LR_W	O	68	LATCHED READ WRITE CONTROL
ANALOG_GND	I	15	ANALOG GROUND
-15VDC	I	38	ANALOG INPUT SUPPLY -15VDC
+15VDC	I	133	ANALOG INPUT SUPPLY +15VDC
UNUSED	NA	129,130	
CSRAMO-	O	37	RAM CHIP SELECT OUTPUT (ACTIVE LOW)
CSRAMI-	I	88	RAM CHIP SELECT INPUT (ACTIVE LOW)
LROMCS-	I	90	LOW BYTE ROM CHIP SELECT INPUT (ACTIVE LOW)
HROMCS-	I	142	HIGH BYTE ROM CHIP SELECT (ACTIVE LOW)
CSROM-	O	136	ROM CHIP SELECT OUTPUT (ACTIVE LOW)
OE-	I	91	ROM OUTPUT ENABLE (ACTIVE LOW)
VPP	I	89	UVEPROM PROGRAMMING VOLTAGE
A14IN	I	41	ALLOWS EEPROM TO BE USED IF DESIRED
ERROR1	O	35	UNRECOVERABLE ERROR 1750A
ERROR2	O	77	MAJOR ERROR 1750A
MPTER-	I	115	MEMORY POINTER ERROR (ACTIVE LOW) 1750A
MPAER-	I	116	MEMORY PARITY ERROR (ACTIVE LOW) 1750A
XARER-	I	117	EXTERNAL ADDRESS ERROR (ACTIVE LOW) 1750A
SFLT0	I	117	SYSTEM FAULT 1750A
SFLT1	I	119	SYSTEM FAULT 1750A
BSREQ-	O	121	INDICATES THAT THE 1750A DESIRES USE OF THE BUSSES
REC	I	46	SERIAL COMMUNICATIONS PORT RECEIVE DATA
XMIT	O	148	SERIAL COMMUNICATIONS PORT TRANSMIT DATA
CTS	I	46	SERIAL COMMUNICATIONS PORT CLEAR TO SEND
RTS	O	149	SERIAL COMMUNICATIONS PORT REQUEST TO SEND
R_W	O	120	READ WRITE OUTPUT
GND	I	10,40,110,140	LOGIC GROUND
BUFDIR-	I	123	EXTERNAL CONTROL OF 1553 BUFFERS
RESIN-	I	132	MASTER RESET INPUT (ACTIVE LOW)
CPUCLK	I	127	CLOCK INPUT TO 1750A
WE-	O	134	WRITE STROBE (ACTIVE LOW)
RD-	O	135	READ STROBE (ACTIVE LOW)
RTAD0-RTAD4	I	92,137,42,141,93	REMOTE TERMINAL ADDRESS
RTADP	I	145	REMOTE TERMINAL ADDRESS PARITY
RTPARERR-	O	96	REMOTE TERMINAL ADDRESS PARITY ERROR
WAITCLK	I	36	INPUT CLOCK TO WAIT STATE GENERATOR
WDCLK	I	80	INPUT CLOCK TO WATCH-DOG TIMER
EXTWAIT	I	87	OFF BOARD ENABLE OF WAIT STATE GENERATOR
16MCLK	I	94	INPUT CLOCK TO CLOCK DIVIDER
1.8MIN	I	143	INPUT BAUD RATE CLOCK
INJIN	I	109	INJECTOR CURRENT INPUT F9450 ONLY
TAGEN-	I	147	1553 TIME TAG ENABLE
WD	O	30	WATCH-DOG TIMER OUTPUT
DATA_A	I	144	1553 CHANNEL A
DATA_A-	I	39	1553 CHANNEL A
DATA_B	I	124	1553 CHANNEL B
DATA_B-	I	43	1553 CHANNEL B
VCC	I	1,50,101,150	LOGIC SUPPLY +5VDC

Table 2. VISUAL BIT L.E.D.s

FUNCTION	COLOR
CPU SELF-TEST	GREEN
ERROR CODE 1	RED
ERROR CODE 2	RED
RS-422 STATUS	GREEN
EPROM STATUS	GREEN
SRAM STATUS	GREEN
1553 STATUS	GREEN
WATCH-DOG	GREEN

ORDERING INFORMATION

BUS-67007

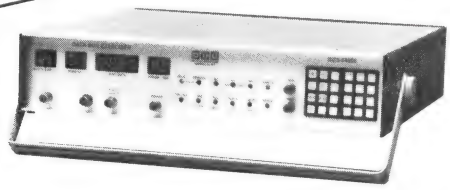
B

DDC
ILC DATA DEVICE CORPORATION

BUS-68005

MIL-STD-1553 DATA BUS EXERCISER

IMPROVED POWER SUPPLY



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-68005 is a low cost portable instrument for testing and troubleshooting MIL-STD-1553A and 1553B systems. It provides full function simulation of Remote Terminal Unit (RTU) and Bus Controller (BC) operation. The BUS-68005 implements the protocol tests of the proposed SAE AE-9A Production Test Plan for Remote Terminals. These tests include RT Address, Word Count, Subaddress, Error Injection, Dual-Redundant Operation, Mode Commands, Status Word, Broadcast Messages, and RT to RT Transfers. BUS-68005 offers simple and flexible operation including either local programming via the front panel 24 pad keyboard and 10 character alphanumeric display, or remote programming via an 8 bit parallel I/O port, RS-232, or IEEE-488 interfaces. The IEEE-488 interface is a Direct Memory Access (DMA) port, allowing for real-time operation. Additional features include error generation and error detection, single, repeat, or halt-on error operation modes, variable response time, variable message gap, variable transmitter amplitude, a real-time monitor port, programmable response time-out, and built-in self test. Its compact size, 3.47" x 14.5" x 17.0", and price/performance makes it a leader for test applications requiring BC and RTU simulation.

FEATURES

- *IMPLEMENTS PROTOCOL TESTS OF SAE AE-9 PROPOSED PRODUCTION TEST PLAN*
- *1553A OR 1553B SYSTEM TESTS*
- *SIMULATES:*
  BUS CONTROLLER
  MULTIPLE REMOTE TERMINALS
- *REAL-TIME MONITOR OUTPUT*
- *ALL PARAMETERS MANUAL AND REMOTE PROGRAMMABLE:*
  KEYBOARD/DISPLAY
  IEEE-488 WITH DMA
  RS-232
  8 BIT PARALLEL
- *ERROR GENERATION/DETECTION*
- *VARIABLE TRANSMITTER*
- *LOW COST*

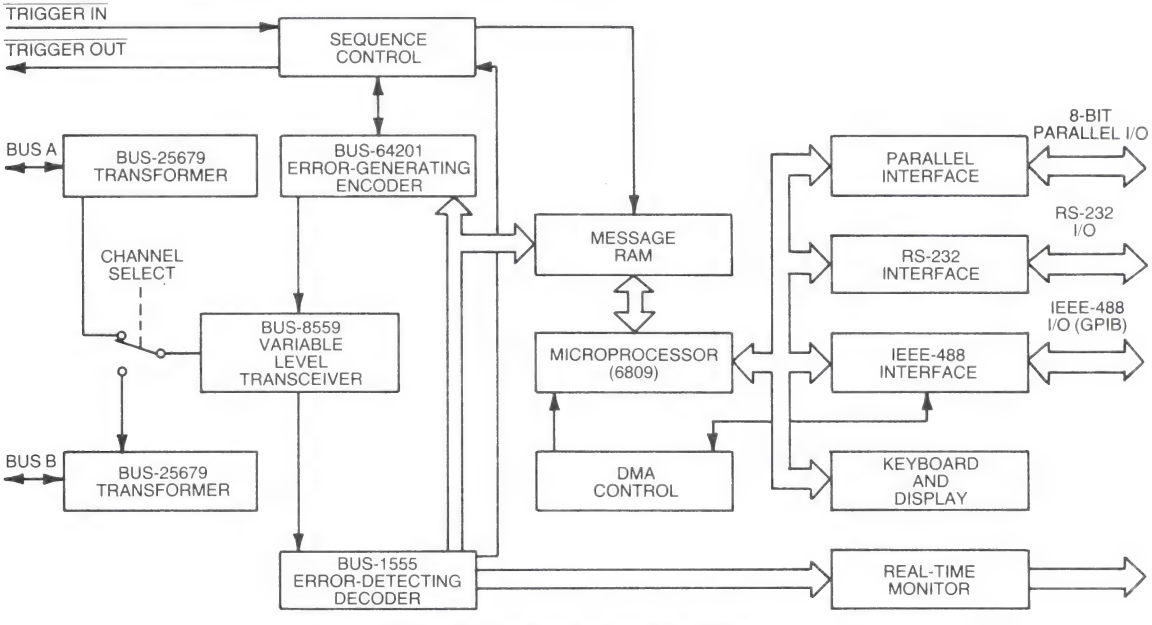


FIGURE 1. BUS-68005 BLOCK DIAGRAM

J

TABLE 14. MANUAL SWITCH/CONTROL FUNCTIONS		
SWITCH	**FUNCTION**	**REMARKS**
RUN	Starts the 1553 data bus message transfer cycle.	The ON-LINE indicator lights up and the display reads BUSY.
HALT	Stops the 1553 data bus message transfer cycle.	The ON-LINE indicator shuts off and the display reads HALT.
I/O SELECT	Selects I/O interface as either Parallel, IEEE-488 or RS-232.	Rear panel switch.
GPIB ADDRESS	Selects the Exerciser's GPIB (IEEE-488) address.	Address has 5 bits. Rear panel switch.
POWER	Turns on the internal power supply.	An initialization and self-test sequence is performed immediately after power turn-on.
VOLTAGE SELECT	Selects 115V or 230VAC line voltage.	Rear panel switch.

DIMENSIONS IN INCHES (CENTIMETERS)
17 x 14.5 x 3.47 (43.2 x 37 x 9.0)

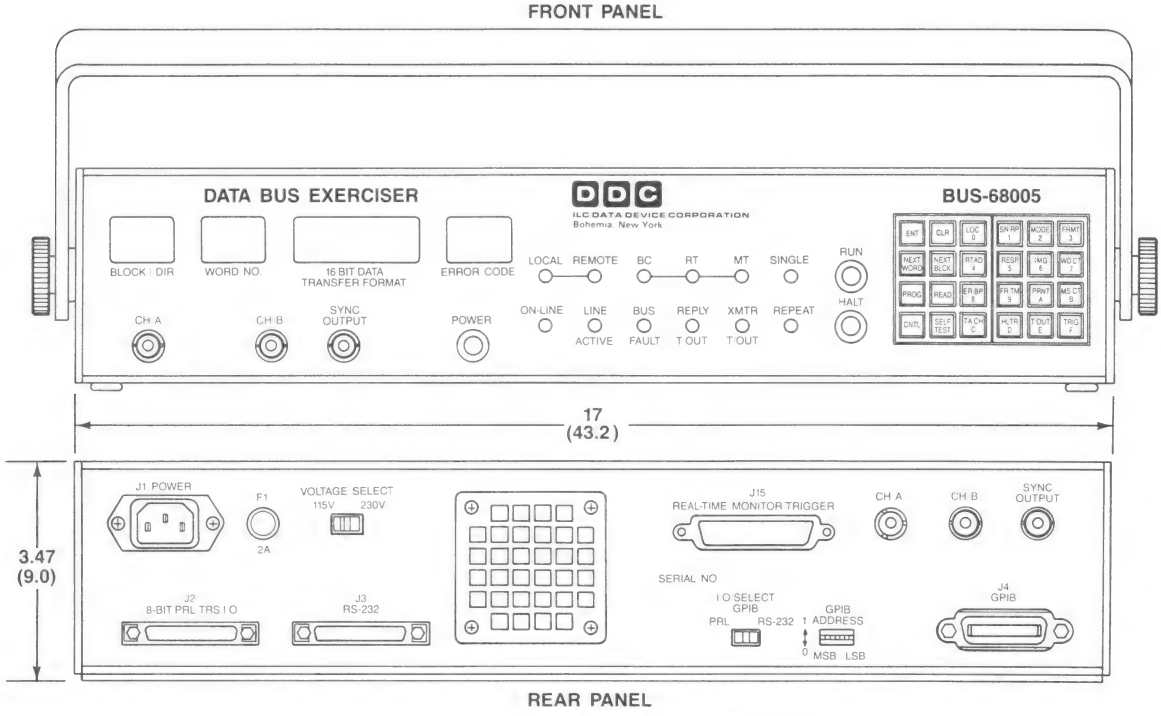


FIGURE 6. MECHANICAL OUTLINE

ORDERING INFORMATION

BUS-68005

Mating Connector for J15 Amphenol 17-10500-1-390 included.

1553 Mating Connector Trompeter PL75-47 (2 included).

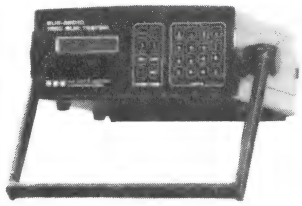
Also included are 2 rack adapters and hardware for full-rack mounting.

C-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-68010

MIL-STD-1553 DATA BUS TESTER



FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-68010 is a low cost bench top portable instrument for testing and troubleshooting MIL-STD-1553 systems. Its price/performance makes it a leader for Bus Controller, Remote Terminal or Bus Monitor simulation applications.

Its simple and flexible operation is controlled via a 24 pad keyboard, with the aid of a 16 character alphanumeric display. Packaged in a 3.5 x 8.5 x 9.3 inch enclosure, it features error generation and error detection, single or repeat messages, and variable inter-message gap time. BC to RT, RT to BC, RT to RT message formats are simulated by the BUS-68010.

The Data Bus Tester's versatility and small physical size make it an ideal choice for laboratory and field testing applications.

FEATURES

- *LOW COST*
- *SMALL SIZE: 3.5″ x 8.5″ x 9.3″*
- *FLEXIBLE OPERATION:*
  BUS CONTROLLER
  REMOTE TERMINAL
  BUS MONITOR
- *PROGRAMMABLE:*
  24 PAD KEYBOARD
- *ERROR GENERATION*
- *ERROR DETECTION*
- *16 CHARACTER ALPHANUMERIC DISPLAY*

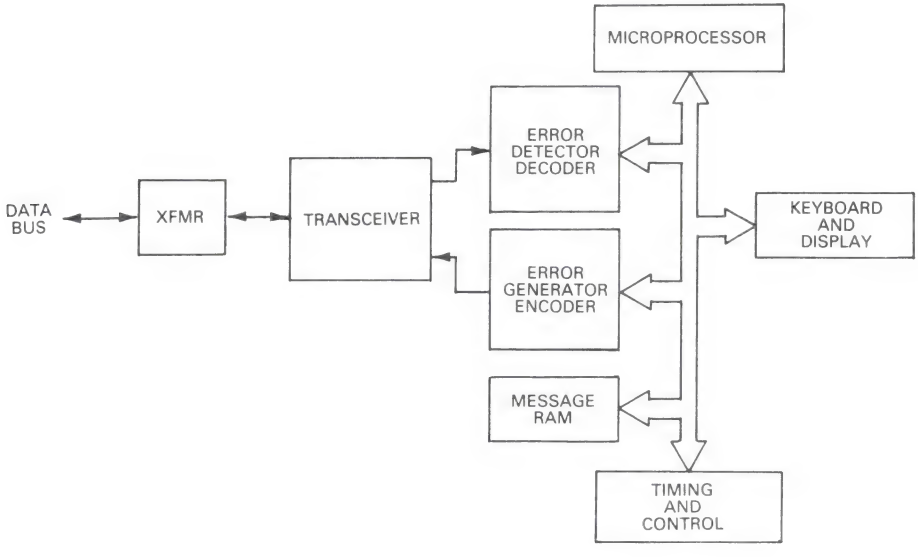


FIGURE 1. BUS-68010 BLOCK DIAGRAM

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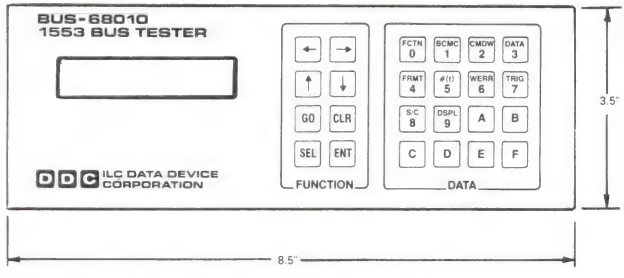
KEYBOARD AND DISPLAY FUNCTIONS		
KEY SEQUENCE	**FUNCTION**	**DISPLAY**
SEL FCTN ◂▸ or ◂▸ ENT	Selects Bus Controller, Remote Terminal or Monitor Mode. The arrows scroll to the next choice.	The current mode will be displayed.
SEL FRMT ◂▸ or ◂▸ ENT	For Bus Controller mode only. Selects Normal, RT (EXT) to RT (EXT), or RT (INT) to RT (EXT) message format.	The current message format will be displayed.
SEL S/C ◂▸ or ◂▸ ENT	Selects single, double or continuous message. The arrows scroll to the next choice.	The current message repetition will be displayed.
SEL TRIG *DIGIT* *DIGIT* ENT	For Remote Terminal mode. The RT address is entered with 2 (HEX) digits. For Monitor mode the trigger address is entered.	The entered address is displayed
SEL DATA ◂▸ or ◂▸ *DIGIT* • • *DIGIT* ENT	Data word and word errors are entered with 6 (hex) digits. Word errors include incorrect sync, parity error, long word and short word. The arrows scroll to the next word in memory. Command words are entered with 4 (HEX) digits or, when in expanded field format, 9 (HEX) digits.	The entered data and word error are displayed.
SEL WERR ◂▸ or ◂▸ ENT	Selects word count error 2 words short, or 1 word short, or correct, or 1 word long, or 2 words long. The arrow scrolls to the next choice.	The current word count error is displayed.
SEL BCMC ◂▸ or ◂▸ ENT	Selects Broadcast/Mode Code options. Either one may be ON or OFF. The arrows scroll to the next choice.	The current broadcast and mode code option is displayed.
SEL #(t) ◂▸ or ◂▸ ENT	Selects the intermessage gap time between 5 msec and 1000 msec. The arrows scroll to the next choice.	The current intermessage gap time is displayed.
GO	Starts operation. For continuous message operation, press CLR key to STOP.	
CLR	Stops operation. Clears last entry.	
SEL CMDW ◂▸ or ◂▸ ENT	Selects Command Word display format of 4-digit (HEX) or expanded field (HEX). The arrows scroll to the next choice.	The current Command Word display format choice is displayed.
SEL DSPL ◂▸ or ◂▸ ENT	Selects LCD viewing angle. Arrows scroll to the next choice.	The optimum display viewing angle varies through 4 choices.

FRONT PANEL CONTROLS/INDICATORS
24 PAD KEYBOARD
16 CHARACTER LCD DISPLAY

REAR PANEL SWITCHES/CONNECTORS
POWER ON/OFF SWITCH
1553 DIRECT COUPLED CONNECTOR
1553 STUB COUPLED CONNECTOR
SYNC OUTPUT

MECHANICAL OUTLINE

3.5" x 8.5" x 9.3"
(8.9 x 21.6 x 23.6 cm)



ORDERING INFORMATION

BUS-68010
└ Options:
0 = 115 VAC Power
1 = 230 VAC Power

D-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-68015

MIL-STD-1553 NOISE TESTER

FULL DATA SHEET AVAILABLE

FEATURES:

- *IMPLEMENTS MIL-STD-1553 NOISE REJECTION TESTS*
- *FULLY SELF-CONTAINED:*
  NOISE SOURCE
  FILTER AMPLIFIER
  BUS CONTROLLER
  WORD AND ERROR COUNTERS
- *PROGRAMMABLE:*
  16 PAD KEYBOARD
  IEEE-488 I/O
- *INDEPENDENTLY VARIABLE SIGNAL AND NOISE LEVELS*
- *LOW COST*
- *COMPACT SIZE:*
  8.25" x 3.5" x 14.5"
- *16 CHARACTER ALPHANUMERIC DISPLAY*
- *AUTOMATIC SELF-TEST*

DESCRIPTION

The BUS-68015 Noise Tester is a low cost bench top portable instrument used for performing the noise rejection tests specified in MIL-STD-1553.

It is fully self-contained, thereby eliminating the need for special test equipment. The BUS-68015 has the noise source, amplifiers, filters, and tester logic built in. Signal and noise levels are user controlled and may be varied independently. The BUS-68015 includes a self-test feature initialized during power-on.

Packaged in a compact 8.25 x 3.5 x 14.5 inch enclosure, manual operation is easily controlled via a 16 pad keyboard, with the aid of a 16 character alphanumeric display. For ATE applications, the BUS-68015 is controlled by means of its IEEE-488 interface.

The BUS-68015 Noise Tester's versatility and small physical size make it an ideal choice for laboratory and field testing applications.

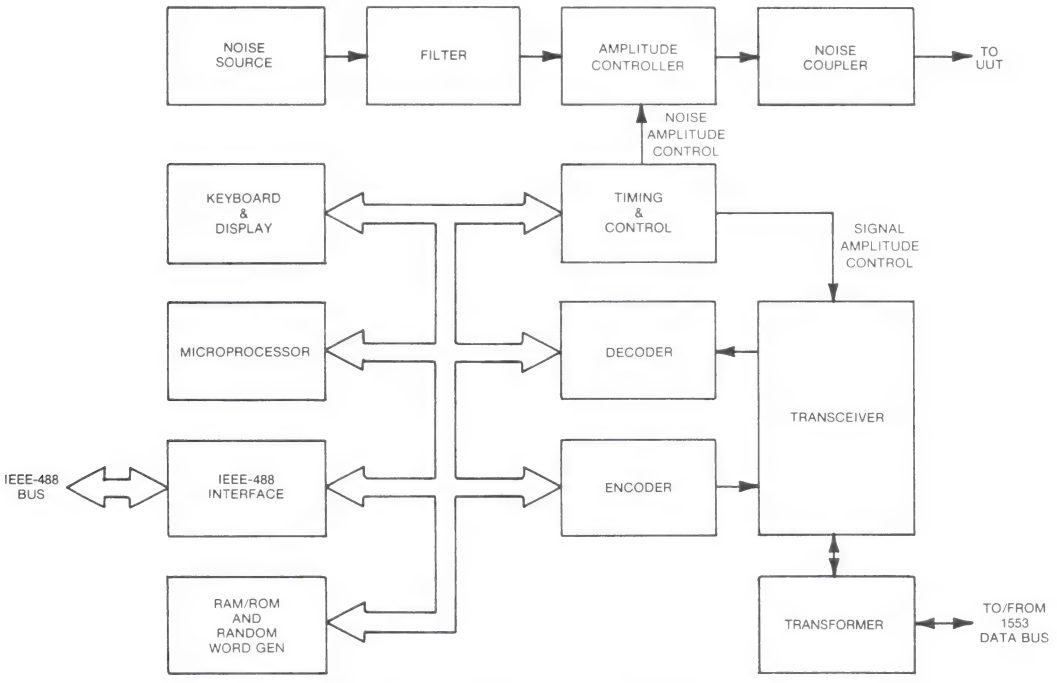


FIGURE 1. BUS-68015 BLOCK DIAGRAM

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DIMENSIONS IN INCHES (CENTIMETERS)
8.25 x 3.5 x 14.5 (20.64 x 8.0 x 36.83)

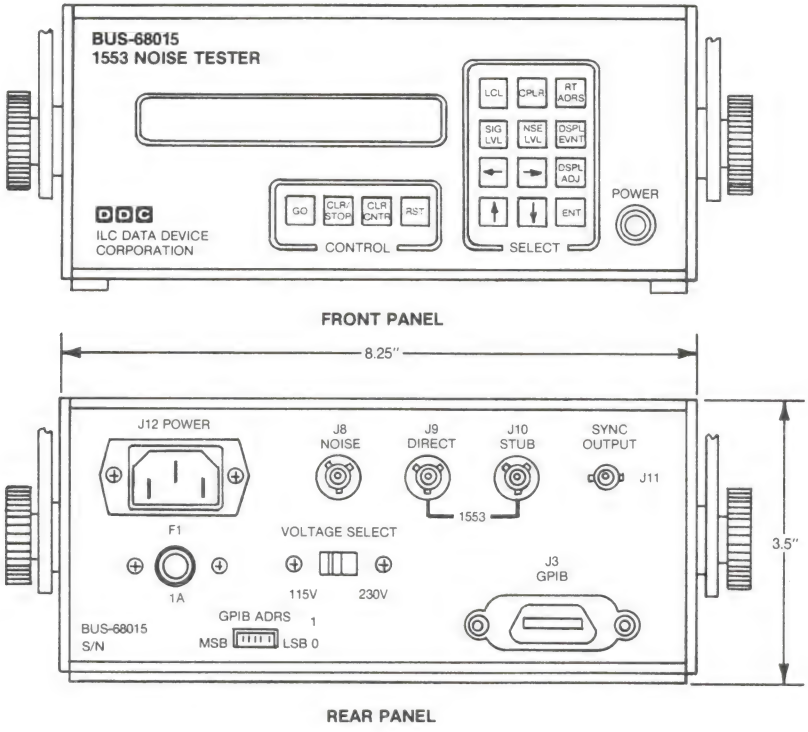

FIGURE 9. MECHANICAL OUTLINE

ORDERING INFORMATION
BUS-68015

Note: BUS-68015 is supplied with carry support handle. For ½ rack mounting brackets order PN 33395. For full rack mounting brackets order PN 33396.

D-ABR

BUS-69005

MIL-STD-1553 PROTOCOL SOFTWARE

FULL DATA SHEET AVAILABLE

DESCRIPTION

The BUS-69005 MIL-STD-1553 Protocol Test software provides a menu-driven Automatic Test Equipment (ATE) environment using an IBM PC/XT/AT host along with DDC's BUS-68005 Data Bus Exerciser and BUS-68015 Noise Tester to perform all protocol tests specified in the SAE RTU Production Test Plan (Section 5.2).

Using a National Instruments GPIB 488 I/O board, the Complete RTU Protocol PTP or any subgroup of tests can be executed simply by choosing the appropriate test(s) and factory or user-definable default parameters from respective menus. Halt on Error, Single Test Execution, Repeat Sequence and Continuous testing options are all supported and menu-selectable.

Test parameters describing Unit-Under-Test (UUT) capabilities and tests to be performed are stored on disk in Configuration files. Multiple Configuration files can be updated and saved on a single disk to meet various device/test requirements. Minimizing operator set-up time, a Configuration file can be saved under the filename DEFAULT. and auto-loaded.

The BUS-69005 software features a simple-to-use on-line help facility allowing the user to select a particular test paragraph in the PTP option, depress the HELP (F1) key, and the respective paragraph within the SAE document is displayed. A print option is also available to produce hard copies of the Configuration files and individual UUT test results.

FEATURES

- *IMPLEMENTS COMPLETE SAE RTU PRODUCTION TEST PLAN PROTOCOL TESTING (PTP)*
- *MENU-DRIVEN COMPLETE/ PARTIAL PTP EXECUTION*
- *DISK STORAGE OF PTP-SUBSET AND RTU CONFIGURATIONS*
- *SINGLE, CONTINUOUS AND HALT-ON-ERROR EXECUTION*
- *SELECTABLE TEST DATA PRINTOUT*
- *MENU-DRIVEN HELP DISPLAYS PTP PARAGRAPHS*
- *RUNS ON IBM PC/XT/AT ® OR COMPATIBLE*

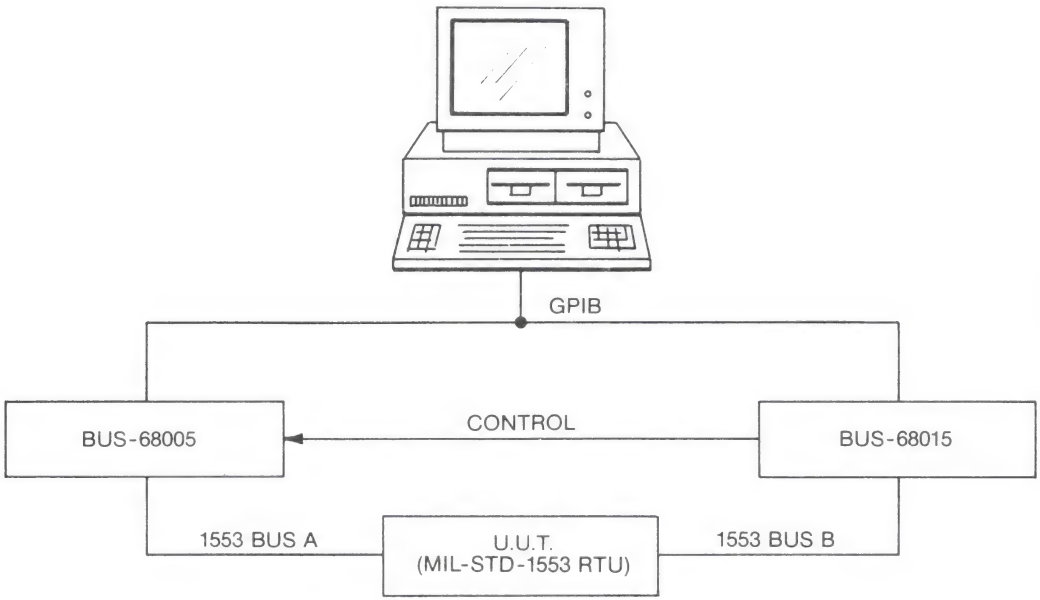

FIGURE 1. BUS-69005 OPERATING ENVIRONMENT

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BUS-69005 OPERATING ENVIRONMENT INSTALLATION

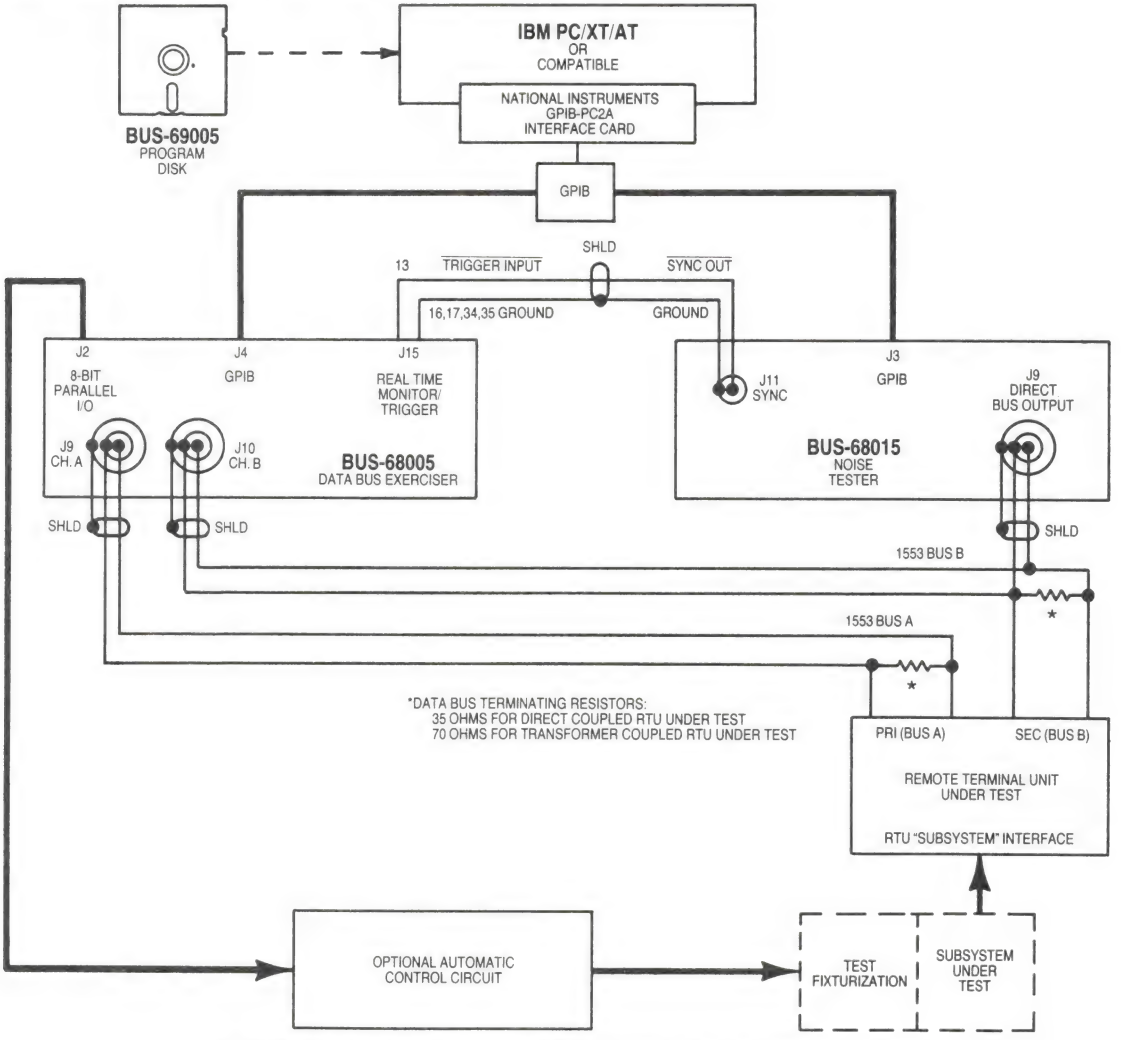


FIGURE 6. BUS-69005 OPERATING ENVIRONMENT ELECTRICAL SET-UP

ORDERING INFORMATION

BUS-69005 MIL-STD-1553 PROTOCOL SOFTWARE

To obtain data sheets on the following products, consult factory.

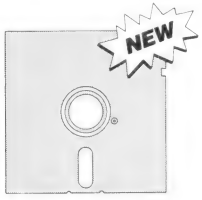
BUS-68005 MIL-STD-1553 DATA BUS EXERCISER

BUS-68015 MIL-STD-1553 NOISE TESTER

C-ABR

DDC
ILC DATA DEVICE CORPORATION

BUS-69006 ADDENDUM TO BUS-69005



MIL-STD-1553 PROTOCOL SOFTWARE

PERFORMS BUS SWITCHING TEST WITH TWO BUS-68005s

DESCRIPTION

The BUS-69006 MIL-STD-1553 Protocol Test software provides a menu-driven Automatic Test Equipment (ATE) environment using an IBM PC/XT/AT host along with two of DDC's BUS-68005 Data Bus Exercisers to perform all protocol tests specified in the SAE RTU Production Test Plan (Section 5.2).

The BUS-69006 Production Test Plan Software operates the same as the BUS-69005 Software with the following exception:

In order to run Paragraph 5.2.2.1 of the PTP Dual Redundant Operation (or Bus Switching Test), a second BUS-68005 Data Bus Exerciser is used (instead of a BUS-68015 Noise Tester) in conjunction with the primary BUS-68005. It is necessary to have two (2) BUS-68005s installed on the GPIB bus in order to run the BUS-69006 software.

The second BUS-68005 is referred to as BUS-68005 #2. The BUS-68005 #2's GPIB Address factory default is 2 and may be changed with the INS69006 (installation) program. The factory default of the National Instruments GPIB-PC2A Card and BUS-68005 #1 remain 0 and 1, respectively.

In the TEST CONFIGURATION menu for the BUS-69006, there is an entry for the BUS-68005 #2 Transmitter Amplitude. The factory default is 87, the same as BUS-68005 #1 CH A and CH B. This provides approximately 3.0 Vpp across 35 Ohms as required by the PTP for direct coupled RTUs.

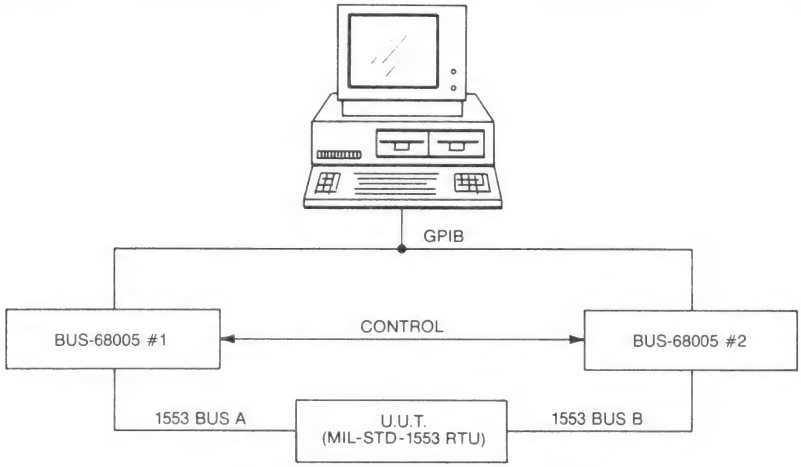


FIGURE 1. BUS-69006 OPERATING ENVIRONMENT

BUS-69006 OPERATING ENVIRONMENT INSTALLATION

Figure 2 illustrates the full electrical set-up required to use the BUS-69006 operating environment. Table 1 lists the cable connectors required.

The BUS-69006 set-up is similar to the BUS-69005 with the following exceptions:

1. *The BUS-68005 Data Bus Exerciser is designated BUS-68005 #1 and the BUS-68005 (which replaces the BUS-68015) is designated BUS-68005 #2.*
2. *Connection to the optional automatic control circuit for control of RTU Address and Status Word bits is from the Parallel I/O port connector J2 of BUS-68005 #1, not BUS-68005 #2.*
3. *1553 Bus A connects from J9 (CH A) of BUS-68005 #1 to BUS A input of the RTU under test. 1553 Bus B connects from J10 (CH B) of BUS-68005 #1 to J9 (CH A) of BUS-68005 #2, and to the BUS B input of the RTU under test.*
4. *As shown in figure 1, a cable is required to connect between the two Real Time Monitor/Trigger I/O connectors (J15) of the two instruments. Note that TRIGGER OUTPUT (J15-12) from each BUS-68005 is connected to TRIGGER INPUT (J15-13) on the alternate instrument.*

TABLE 1. BUS-69006 SUGGESTED MATING CONNECTORS

BUS-68005	CONNECTOR
J2 (PARALLEL I/O)	TRW DB25S (DB25 FEMALE)
J15 (TRIGGER INPUT)	AMPHENOL 17-10500-1-390 50-PIN FEMALE
J9, J10 (CH A, CH B)	TROMPETER PL75-47 TRIAX MALE
CABLE, TRIAX	TROMPETER 14949

J

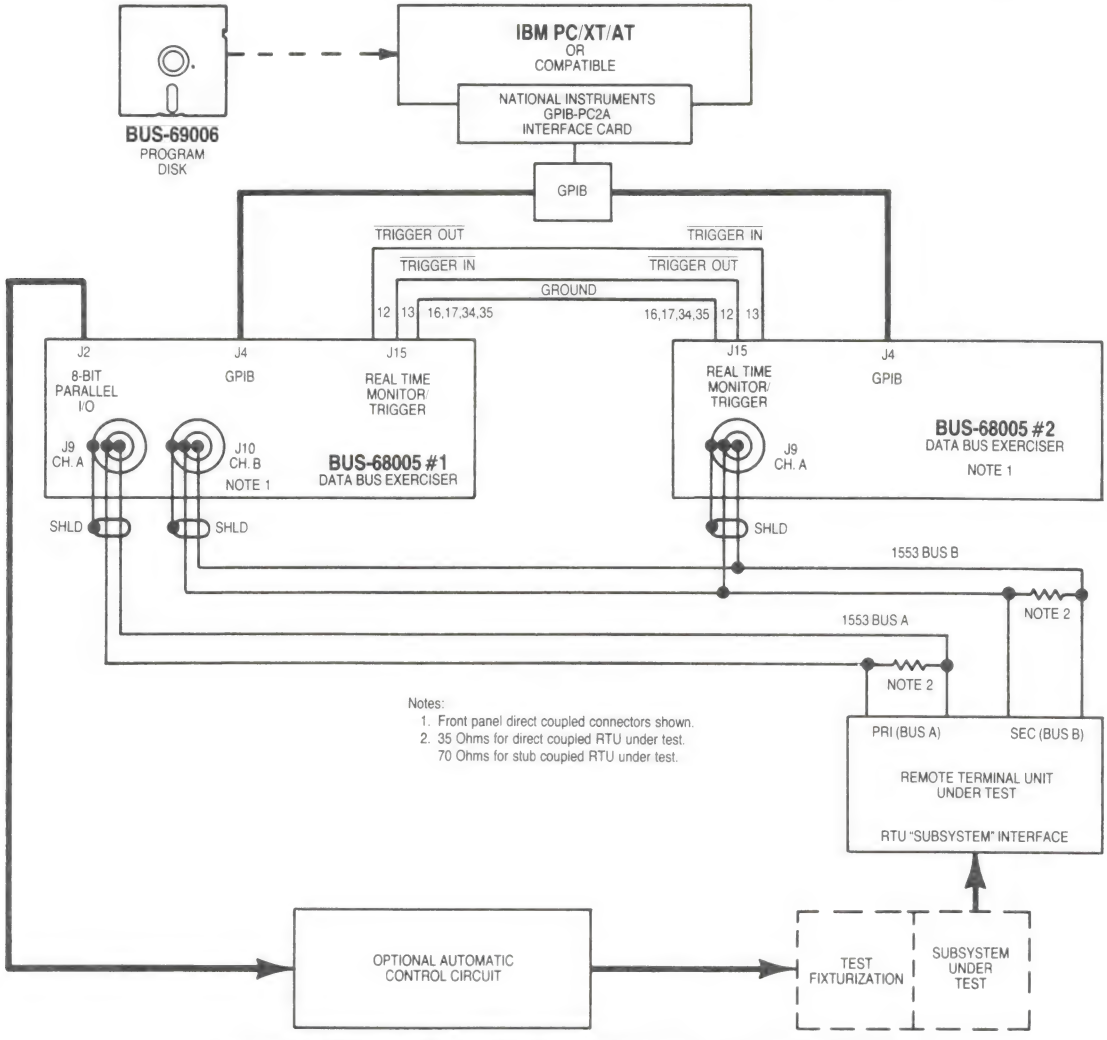


FIGURE 2. BUS-69006 OPERATING ENVIRONMENT ELECTRICAL SET-UP

ORDERING INFORMATION

BUS-69006 MIL-STD-1553 PROTOCOL SOFTWARE

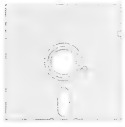
To obtain data sheets on the following products, consult factory.

BUS-68005 MIL-STD-1553 DATA BUS EXERCISER

BUS-69005 MIL-STD-1553 PROTOCOL SOFTWARE

A

"C" SOFTWARE LIBRARY TO SUPPORT THE BUS-61553, BUS-61559, BUS-65515, BUS-65522II, BUS-65529, BUS-65531, and BUS-65555



FULL DATA SHEET AVAILABLE

DESCRIPTION

Free software is now available to support the BUS-61553 (AIM-HY), BUS-61559(AIM-HY'er), BUS-65515, BUS-65522II, BUS-65529, BUS-65531, and BUS-65555. The use of these libraries allow the 1553 components and board level products to be controlled and accessed by means of high-level subroutine calls rather than by low-level bit and word operations.This dramatically reduces the time required to develop real time application software for MIL-STD-1553 terminals based on these products.

The software consists of a library of run time routines to perform common MIL-STD-1553 functions. Source code and complete documentation is provided to allow a programmer to customize the library, add additional routines, and incorporate the routines into in-line code. An extensive self test routine is also provided.

The "C" library routines provide structures for all internal registers and memory map. This greatly reduces the learning curve for new users, and provides clear, readable code.

Most applications can use the default data structures employed without modification.

Error codes indicate an invalid parameter has been detected; this reduces software debugging time.

The software is provided in ASCII format on a 5 1/2 inch, IBM® PC, DOS compatible floppy disk. The user can easily transfer this code to other, non-PC systems, such as VME based systems.

An IBM PC compatible card, containing either the AIM-HY or the AIM-HY'er, is available from DDC. This allows programmers to develop software for a DDC based MIL-STD-1553 terminal, while the terminal's hardware design is still in progress.

Features

- ***Free Library of "C" Routines***
- ***Source Code and Complete Documentation Provided***
- ***Provides Modular, Readable Code, Reducing Software Development Time***
- ***"C" Structures Eliminate Need to Learn Detailed Address / Bit Maps and Data Formats***

The following example sets up an AIM-HY or AIM-HY'er as a Bus Controller. It sends a massage to RT #1, instructing it to receive two words to subaddress #1.

```
/* Issue a Reset Command to Initialize AIM-HY */
flag = reset_AIM;
PRINT_ERROR_MSG(flag);
CLEAR_RAM():
flag = DEF_MODE(BC) ;
PRINT_ERROR_MSG(flag);

/* Define the Bus */
message.bus= BUS_A;

/* Define the type of message */
message.self_test= NO;
message.mask_broadcast_bit= NO;
message.broadcast  = NO;
message.mode_code = NO;
message.rt_rt  = NO;

/* Define the RT Address */
message.cmd_1.taddr      =1;

/* Define the T/R* bit */
message.cmd_1.t_r = RECEIVE;

/* Define the Word Count */
message.cmd_1.wcnt       = 2;

/* Define the Data Words */
data_buffer[0] = 0x1111;
data_buffer[0] = 0x2222;

/* Define the Message,  Format:  /
/* Message #, message, data buffer, word count */
flag = DEF_MSG(1, message, data_buffer, 2);
PRINT_ERROR_MSG(flag);

/* Define the frame, Format = frame #, starting position, # of
messages, # of times to run */
frame_item[0] = 1;
flag = DEF_FRAME(1, frame_item);
PRINT_ERROR_MSG(flag);

/* Issue the Message */
flag = RUN_BC(STACK_1, 1, 1, 1);
 PRINT_ERROR_MSG(flag);
```

EXAMPLE OF USE

® IBM PC/XT/AT is a registered trademark of International Business Machines.
™ GRiD and GRiDCASE are registered trademarks of GRiD Systems Corporation.

ORDERING INFORMATION

BUS-69050 — "C" Library for the BUS-61553(AIM-HY) Family of Components (BC/RT/MT)

BUS-69051 — "C" Library for the BUS-61559(AIM-HY'er) Family of Components (BC/RT/MT)

BUS-69052 — "C" Library for the BUS-65515 (IBM PC/XT/AT BC/RT/MT)

*BUS-69053 — "C" Library for the BUS-65522II (VME/VXI BC/RT/MT)

**BUS-69054 — "C" Library for the BUS-65529 (IBM PC/AT BC/RT/MT)

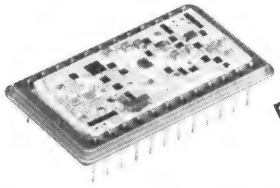
***BUS-69055 — "C" Library for the BUS-65555 (GRiD™ BC/RT/MT)

*BUS-69056 — "C" Library for the BUS-65531 (IBM PS/2 BC/RT/MT)

* Contact factory for Release Dates

**High Density 5¼ Diskette

***High Density 3½ Diskette



FULL DATA SHEET AVAILABLE

MIL-STD-1553 TRANSCEIVER

DESCRIPTION

The BUS-8553 Transceiver is a complete transmitter and receiver conforming fully to MIL-STD-1553A and 1553B. Features of this high reliability transceiver include: Harris 15530 type Encoder/Decoder direct interface capability, ±15V or +15V and −12V power supply voltage requirements, and an internal (factory pre-set) threshold level.

Figure 1 illustrates a block diagram of the BUS-8553 Transceiver. The receiver section accepts phase-modulated bipolar data from a MIL-STD-1553 Data Bus and produces TTL signal data at its outputs: RX Data Out and RX $\overline{\text{Data}}$ Out. These outputs represent positive and negative excursions of the input Bus signals beyond a preset threshold level. The receiver can be taken off-line (outputs disabled) by the application of a logic "0" to the STROBE input.

The transmitter section accepts bipolar TTL signal data at its TX Data and TX $\overline{\text{Data}}$ input lines and produces a 28Vpp differential signal across a 140 Ohm load that's coupled to the TX Data and TX $\overline{\text{Data}}$ outputs via transformer. An external input, INHIBIT, takes priority over the transmitter inputs and disables the transmitter when activated with a logic "1".

The BUS-8553 Transceiver is packaged in a 24 pin DDIP, measuring 1.4 x 0.8 x 0.2 inches. Its small size, low power dissipation, and direct interface compatibility with Harris 15530 type Encoder/Decoder make it an excellent choice for any MIL-STD-1553A or 1553B Transceiver application.

FEATURES

- *MEETS ALL MIL-STD-1553A AND 1553B REQUIREMENTS*
- *VERY LOW POWER DISSIPATION*
- *IMPROVED FILTERING ON RECEIVER TO ENHANCE BIT ERROR RATE OF SYSTEM*
- *±15V OR +15V AND −12V POWER SUPPLY VOLTAGES*
- *SCREENED TO MIL-STD-883*
- *HARRIS 15530 ENCODER/DECODER DIRECT INTERFACE COMPATIBILITY*

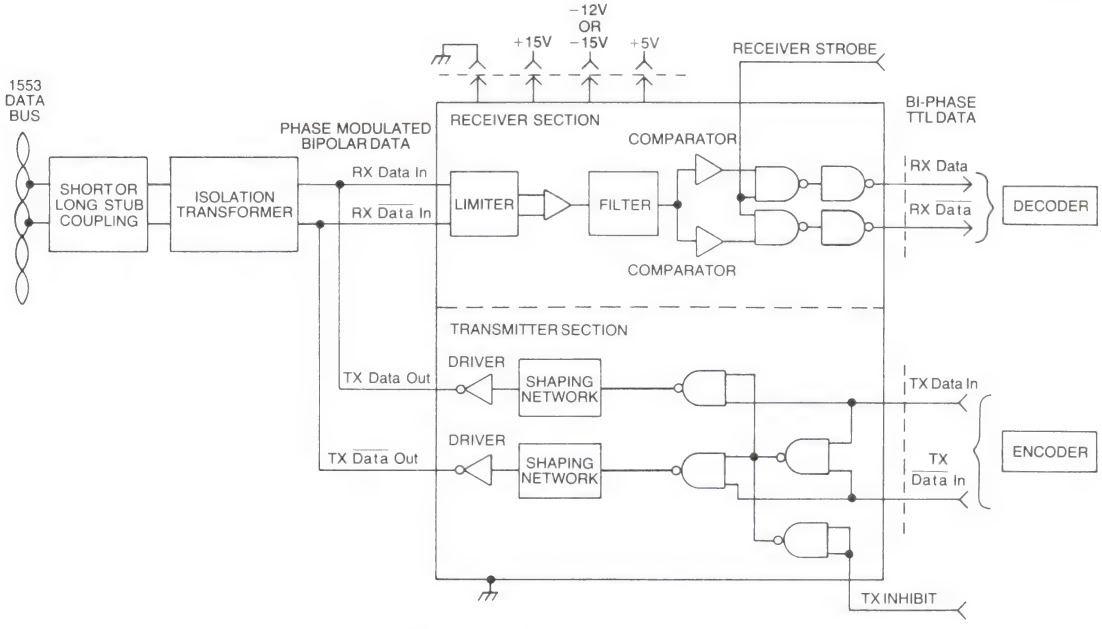


FIGURE 1. BUS-8553 BLOCK DIAGRAM

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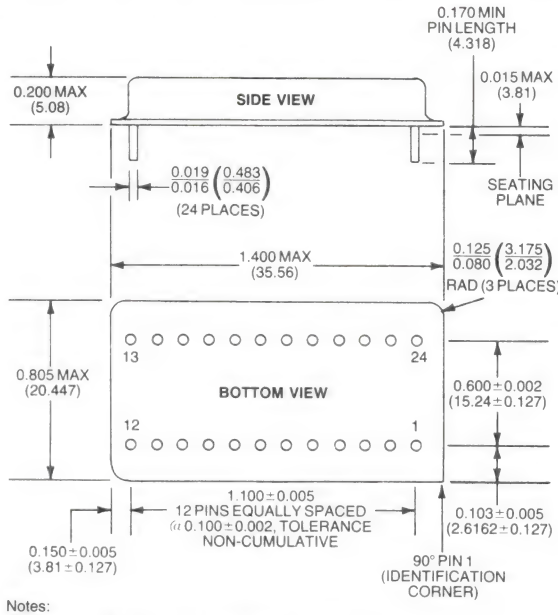
TABLE 1. BUS-8553 SPECIFICATIONS

PARAMETER	VALUE		
RECEIVER			
Input Level	40Vpp, differential, max		
Internal Threshold(1)	0.56Vpp min, 1Vpp max		
CMRR	40 db, min		
Input Resistance, differential	7K Ohm, min		
Input Capacitance, differential	5pf, max		
DRIVER			
Output Level	28Vpp, nominal, across 140 Ohm load		
Rise/Fall Time	130ns, typical		
Output Noise	10mVpp, differential, max		
Output Offset	±90mVpp, max differential across 35Ω load		
Output Impedance (Non-Transmitting)			
Output Resistance, differential	10K Ohm, min		
Output Capacitance, differential	5pf, max		
LOGIC; TTL/CMOS Compatible			
Receiver Strobe Input	2 LSTTL loads, max		
All Logic Outputs (Receiver)	10 LSTTL loads, min		
Transmitter Inhibit Input	1 TTL load, max		
Transmitter TX Data and TX Data Inputs	2 TTL loads, max		
POWER SUPPLY REQMTS	+5V±10%	+15V±5%	−15V±5%
Non-Transmitting (typ/max)	40/50mA	30/40mA	25/30mA
Transmitting, 50% duty cycle (typ/max)	40/50mA	110/130mA	25/30mA
Transmitting, 100% duty cycle (typ/max)	40/50mA	200/220mA	25/30mA
THERMAL			
Operating Junction Temp.(2)	−55°C to 160°C		
Operating Case Temperature(2)	−55°C to 125°C		
Storage Temperature	−65°C to 150°C		
Thermal Resistance			
Junction to Case (Hottest Die)	110°C/W		
Case to Air	30°C/W		
POWER DISSIPATION	**Total Hybrid**		
Non-Transmitting (typ/max)	1.0/1.3W		
Transmitting, 50% duty cycle (typ/max)	1.7/2.0W		
Transmitting, 100% duty cycle (typ/max)	2.3/2.8W		
POWER DISSIPATION	**Hottest Die**		
Transmitting, 50% duty cycle (typ/max)	0.14/0.16W		
Transmitting, 100% duty cycle (typ/max)	0.28/0.31W		
MECHANICAL			
Size, 24 Pin DDIP, inches (mm)	1.4 x 0.8 x 0.2 (35.6 x 20.3 x 5.1)		
Weight	0.4 oz typ		

Notes:
(1) The Threshold Level, as referred to in this specification, is meant to be the maximum peak to peak voltage (measured on the Data Bus) that can be applied to the receiver without causing the output to change from the OFF state.
(2) For any transmitting duty cycle (derating not required).



Notes:
(1) Dimensions are in inches (millimeters).
(2) Lead identification numbers are for reference only.
(3) Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
(4) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

FIGURE 4. MECHANICAL OUTLINE 24 PIN DDIP

ORDERING INFORMATION

BUS-8553-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883

B = Screened to MIL-STD-883 but without QCI testing.

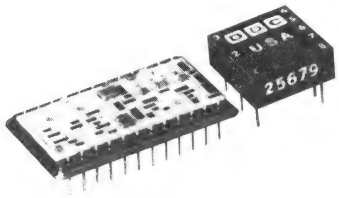
Blank = Standard DDC procedures.

Mating Transformer BUS-25679

G - ABR

BUS-8559

VARIABLE OUTPUT MIL-STD-1553 TRANSCEIVER



FULL DATA SHEET AVAILABLE

DESCRIPTION AND APPLICATIONS

Designed specifically for use in automatic test equipment when a variable transmitter output level is required, the DDC Model BUS-8559 Transceiver is a complete transmitter and receiver conforming to MIL standards 1553A and 1553B. The receiver section accepts phase-modulated bipolar data at the input and produces a bi-phase TTL signal at the output (Figure 1). The outputs, DATA and $\overline{\text{DATA}}$, represent positive and negative excursions of the input beyond an internally fixed threshold. These positive and negative thresholds are internally set at the factory for a nominal 1V p-p signal, measured at point "A", Figure 2. An external strobe input is provided to allow the removal of the receiver from the line. A logic "0" applied to "STROBE" will disable the receiver output.

The BUS-8559 transmitter section accepts bi-phase TTL data at the input and produces a 0 to 27 volt nominal p-p differential signal across the 145Ω load, when measured at point "B", Figure 2. When coupled to the data bus with the specified transformer*, isolated (on the data side) with two 55.0Ω fault isolation resistors, and loaded by two 70Ω terminations (plus additional receivers), the data bus signal produced is 0 to 7.5 volts nominal p-p measured at point "A" (Figure 2).

When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter presents a high impedance to the line. An external inhibit input is provided to allow the removal of the transmitter output from the line (Figure 3). A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter.

The transceiver is available in a 24 pin hybrid package measuring 1.4 x 0.8 x 0.2 inch, and can be used in any MIL-STD-1553 application which requires the use of a transceiver.

*Transformer P/N BUS-25679. See Mechanicals.

FEATURES

- *VARIABLE TRANSMITTER OUTPUT*
- *TRANSMITTER/RECEIVER IN A SINGLE 24 PIN DDIP HYBRID*
- *VERY LOW POWER DISSIPATION*
- *MEETS MIL-STD-1553A AND 1553B*
- *IMPROVED FILTERING ON RECEIVER TO ENHANCE BIT ERROR RATE OF SYSTEM*
- *±15V OR +15 AND −12V OPERATION*

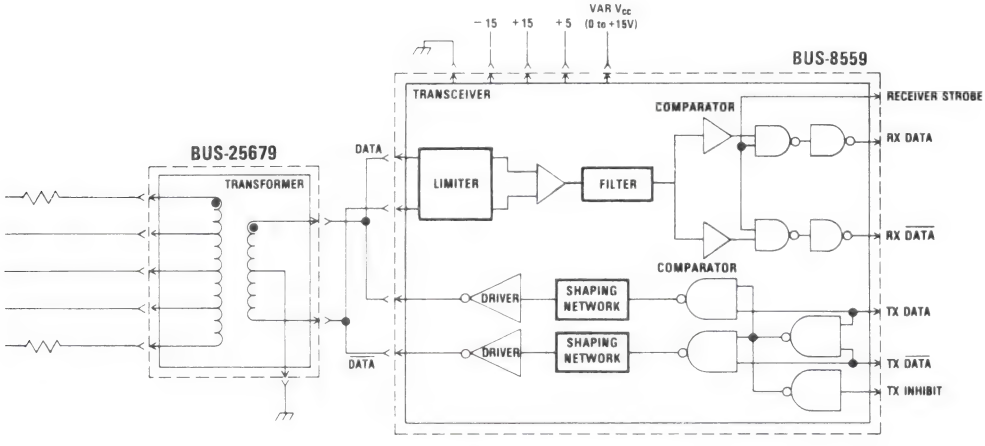


FIGURE 1. BLOCK DIAGRAM

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SPECIFICATIONS-TRANSFORMER AND BUS-8559 HYBRID

PARAMETER	VALUE
RECEIVER	
Input Level	40V p-p differential max
Input Impedance	4 KΩ differential min
Threshold Level	1V p-p nominal, internally set (direct coupled mode)
Output Level	TTL, 10 LS Loads
Outputs:	
V_{OL}	0.6V max
V_{OH}	2.5V min
I_{OL}	4mA max
I_{OH}	−400 μA max
TRANSMITTER	
Input Level	TTL, 2 LS Loads
Inputs:	
V_{ih}	2V min
V_{il}	0.8V max
I_{ih}	80 μA max
I_{il}	−3.2mA max
Output Level	0 to 27V p-p nominal across 145Ω load 0 to 20V p-p nominal (measured at point C, Figure 2)
Rise/Fall Time	130 nsec typical
Output Noise	10mV p-p differential max
Variable Vcc	0 to +15V DC

GENERAL

Power Supply Requirements

P.S.	STDBY	25%	100%
V	mA	mA	mA
+5	25 max	22 max	21 max
+15	30 max	30 max	30 max
-15	30 max	30 max	30 max
V_{cc}	0	70	180

Operating Temperature Range	−55°C to +125°C (case temp.)
Storage Temperature Range	−55°C to +135°C
Size (24pin DDIP hybrid)	1.4 x 0.8 x 0.2 inch (36 x 20 x 5mm)
Weight	0.4 oz typ (11g)

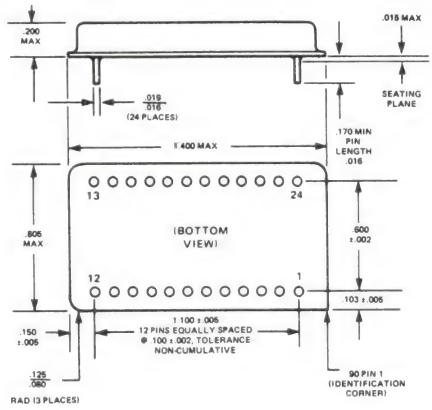
NOTES: (1) Will operate with ±12V P.S.

BUS-8559 PIN CONNECTION TABLE

PIN	FUNCTION
1	TX Data Out
2	TX $\overline{\text{Data}}$ Out
3	GND
4	N.C.
5	N.C.
6	Variable Vcc
7	RX Data Out
8	Strobe
9	GND
10	RX $\overline{\text{Data}}$ Out
11	N.C.
12	N.C.
13	+15V DC
14	N.C.
15	RX Data In
16	RX $\overline{\text{Data}}$ In
17	N.C.
18	GND
19	−15VDC
20	+5VDC
21	TX Inhibit
22	TX Data In
23	TX $\overline{\text{Data}}$ In
24	N.C.

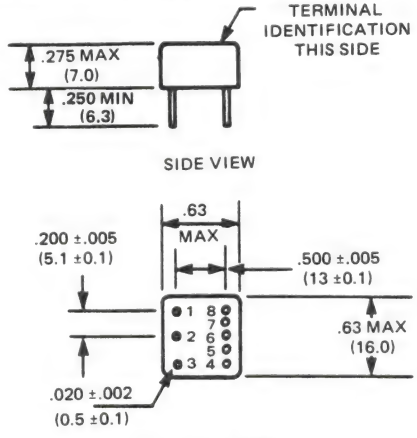
G - ABR

MECHANICAL OUTLINE
24 Pin Double DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within ±.010 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

MECHANICAL OUTLINE
TRANSFORMER (P/N BUS-25679)



NOTES:
1. All dimensions are in inches(millimeters)
2. Pin callouts on bottom view are for reference only

ORDERING INFORMATION

BUS − 8559 − B

Reliability Grade:

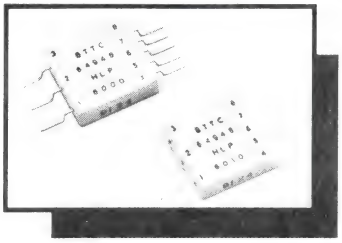
B = Screened to MIL-STD-883 but without QCI testing.
Blank = Standard DDC procedures.

TRANSFORMER: BUS-25679

NOTE: The transceiver and transformer must be ordered as separate parts.

DDC
ILC DATA DEVICE CORPORATION

HLP-6000 SERIES



HERMETICALLY SEALED - LOW PROFILE 0.175 MAX HEIGHT MIL-STD-1553 TRANSFORMERS

DESCRIPTION AND APPLICATIONS

The military data bus specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The HLP-6000 series of transformers provide the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B compliance.

The step up and down ratios that are available with the HLP-6000 series complement DDC's entire MIL-STD-1553 product line and are compatible with competitor's drivers, receivers, and transceivers. These transformers are low profile, modular units that are multi-tapped to accommodate existing system configurations. Both leads and the hermetically sealed case are made of gold plated Kovar, to assure corrosion resistant surfaces. The units are built in accordance with MIL-T-21038, their leads conveniently accommodate printed circuit board mounting. Sinusoidal or trapezoidal waveforms are accurately processed, making the HLP-6000 series of transformers an excellent choice for any MIL-STD-1553A or B application.

FEATURES

- ***Flat Pack***
- ***Surface Mount***
- ***For Use With MIL-STD-1553A and B, MacAir A-3818, A-5690, A-5232, and A-4905***
- ***Ultra - Low Profile***
- ***-55°C to +130°C Operating Temperature Range***
- ***Built and Tested to MIL-T-21038, MIL-STD-202, and MIL-STD-2000***
- ***Designed to meet ESDS Test, MIL-STD-883, Method 3015.3, Category B.***

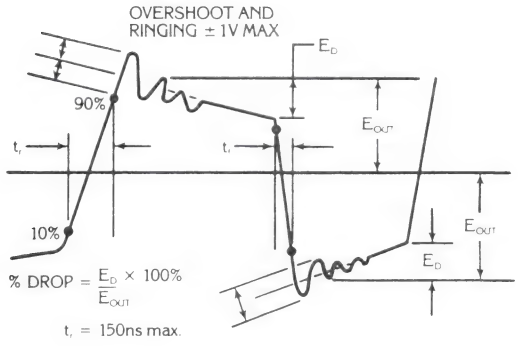


FIGURE 1. WAVEFORM INTEGRITY

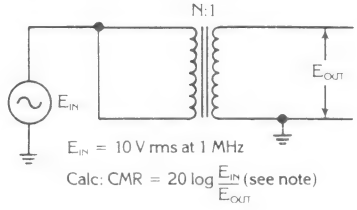


FIGURE 2. CIRCUIT FOR COMMON MODE REJECTION

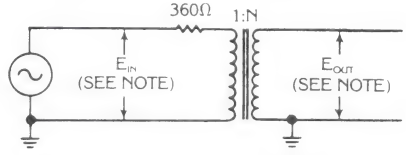

360Ω
1:N
E_{IN}
(SEE NOTE)
E_{OUT}
(SEE NOTE)
E_{IN} = 250 kHz square wave, 27.0 volts peak-to-peak with a rise and fall time no greater than 100 ns.
Calc: Droop = $\frac{E_D}{E_{OUT}} \times 100\%$. (See figure 1 for E_D)

FIGURE 3. CIRCUIT FOR WAVEFORM INTEGRITY

Note: Input to be applied and output to be measured for all dash numbers as shown. N represents highest turn winding in each test.

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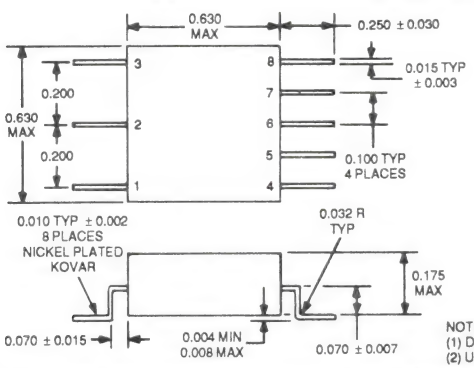
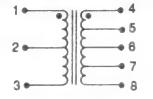
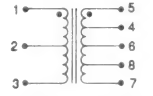
CONFIGURATION A

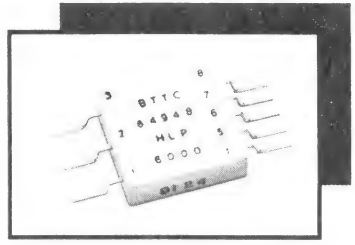




CIRCUIT DIAGRAM FOR HLP-6000, 6001, 6002, 6003, 6004, AND 6006



CIRCUIT DIAGRAM FOR DASH NUMBER HLP-6005

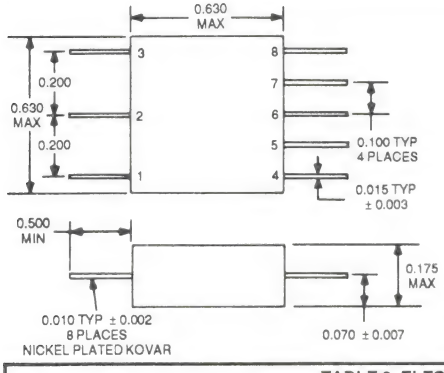


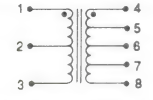
NOTES:
(1) DIMENSIONS ARE IN INCHES
(2) UNLESS OTHERWISE SPECIFIED, TOLERANACE IS ±0.010 INCHES

TABLE 1. ELECTRICAL CHARACTERISTICS — CONFIGURATION A

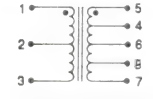
BETA P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCEΩ(max)	IMPEDANCE Ω (min)
HLP-6000	2:5 ±3% 4:7 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 3000
HLP-6001	1:0.83 ±3% 1:0.60 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 3,000
HLP-6002	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 7,200
HLP-6003	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 4,000
HLP-6004	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.2 4-8 3.0	(1-3) 4,000
HLP-6005	2.3:1 ±3% 3.2:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.2 4-8 3.0	(5-7) 3,000
HLP-6006	2.12:1 ±3% 1.5:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.1 4-8 3.0	(4-8) 4,000

CONFIGURATION B

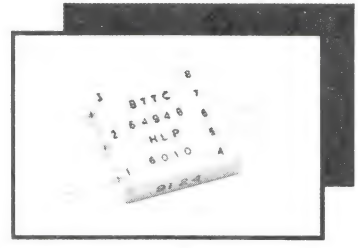




CIRCUIT DIAGRAM FOR HLP-6007, 6008, 6009, 6010, 6011, AND 6013



CIRCUIT DIAGRAM FOR DASH NUMBER HLP-6012



NOTES:
(1) DIMENSIONS ARE IN INCHES
(2) UNLESS OTHERWISE SPECIFIED, TOLERANCE IS ±0.010 INCHES

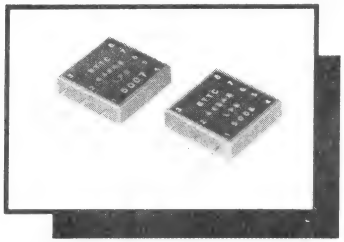
TABLE 2. ELECTRICAL CHARACTERISTICS — CONFIGURATION B

BETA P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCEΩ(max)	IMPEDANCE Ω (min)
HLP-6007	2:5 ±3% 4:7 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 3000
HLP-6008	1:0.83 ±3% 1:0.60 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 3,000
HLP-6009	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 7,200
HLP-6010	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 4,000
HLP-6011	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.2 4-8 3.0	(1-3) 4,000
HLP-6012	2.3:1 ±3% 3.2:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.2 4-8 3.0	(5-7) 3,000
HLP-6013	2.12:1 ±3% 1.5:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.1 4-8 3.0	(4-8) 4,000

B

DDC
ILC DATA DEVICE CORPORATION

LPB-5000 SERIES



ULTRA - LOW PROFILE 0.150 MAX HEIGHT MIL-STD-1553 TRANSFORMERS

DESCRIPTION AND APPLICATIONS

The military data bus specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The LPB-5000 series of transformers provide the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B compliance.

The step up and down ratios that are available with the LPB-5000 series complement DDC's entire MIL-STD-1553 product line and are compatible with competitor's drivers, receivers, and transceivers. These transformers are low profile, modular units that are multi-tapped to accommodate existing system configurations. Encapsulated in accordance with MIL-T-21038, their tin coated steel leads conveniently accommodate printed circuit board mounting. Sinusoidal or trapezoidal waveforms are accurately processed, making the LPB-5000 series of transformers an excellent choice for any MIL-STD-1553A or B application.

FEATURES

- *FLAT PACK*
- *SURFACE MOUNT*
- *FOR USE WITH MIL-STD-1553A AND B, MACAIR A-3818, A-5690, A-5232, AND A-4905*
- *ULTRA - LOW PROFILE*
- *-55°C TO +130°C OPERATING TEMPERATURE RANGE*
- *BUILT AND TESTED TO MIL-T-21038 AND MIL-STD-202*

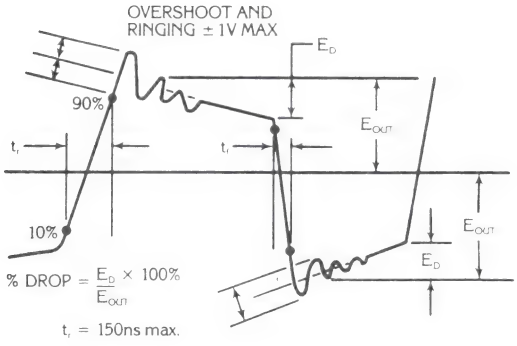


FIGURE 1. WAVEFORM INTEGRITY

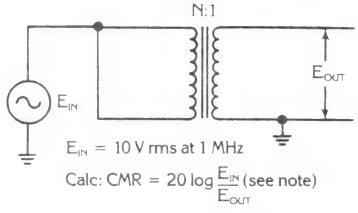
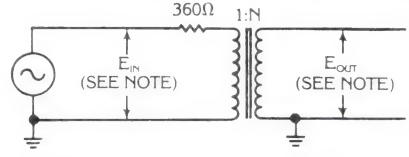


FIGURE 2. CIRCUIT FOR COMMON MODE REJECTION



E_{IN} = 250 kHz square wave, 27.0 volts peak-to-peak with a rise and fall time no greater than 100 ns.

Calc: Droop = $\frac{E_D}{E_{OUT}} \times 100\%$. (See figure 1 for E_D)

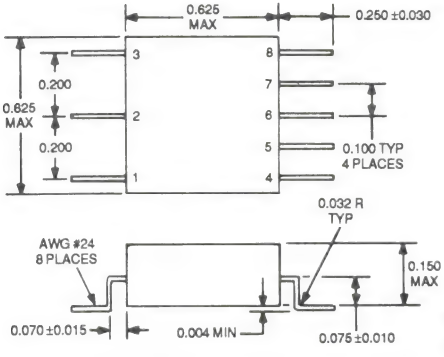
FIGURE 3. CIRCUIT FOR WAVEFORM INTEGRITY

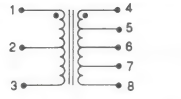
Note: Input to be applied and output to be measured for all dash numbers as shown. N represents highest turn winding in each test.

J

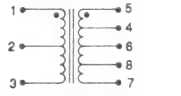
LPB-5000 SERIES

CONFIGURATION A

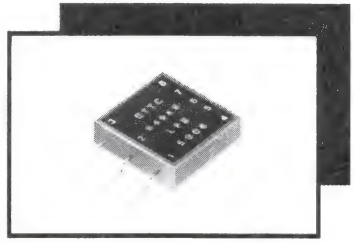




CIRCUIT DIAGRAM FOR LPB-5000, 5001, 5002, 5003, 5004, AND 5006



CIRCUIT DIAGRAM FOR DASH NUMBER LPB-5005

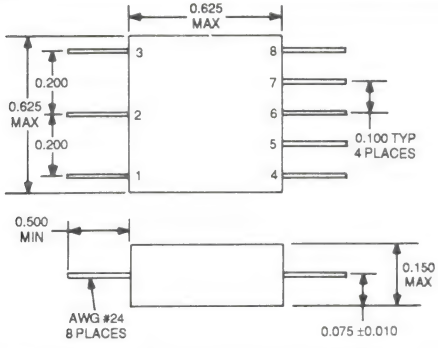


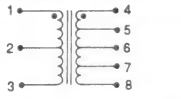
NOTES:
(1) DIMENSIONS ARE IN INCHES
(2) UNLESS OTHERWISE SPECIFIED, TOLERANACE IS ±0.010 INCHES

TABLE 1. ELECTRICAL CHARACTERISTICS — CONFIGURATION A

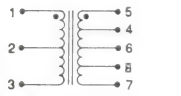
BETA P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω(max)	IMPEDANCE Ω (min)
LPB-5000	2:5 ±3% 4:7 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 3000
LPB-5001	1:0.83 ±3% 1:0.60 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 3,000
LPB-5002	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 7,200
LPB-5003	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 4,000
LPB-5004	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.2 4-8 3.0	(1-3) 4,000
LPB-5005	2.3:1 ±3% 3.2:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.2 4-8 3.0	(5-7) 3,000
LPB-5006	2.12:1 ±3% 1.5:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.1 4-8 3.0	(4-8) 4,000

CONFIGURATION B

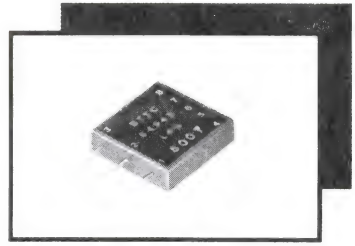




CIRCUIT DIAGRAM FOR LPG-5007, 5008, 5009, 5010, 5011, AND 5013



CIRCUIT DIAGRAM FOR DASH NUMBER LPB-5012



NOTES:
(1) DIMENSIONS ARE IN INCHES
(2) UNLESS OTHERWISE SPECIFIED, TOLERANCE IS ±0.010 INCHES

TABLE 2. ELECTRICAL CHARACTERISTICS — CONFIGURATION B

BETA P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE Ω(max)	IMPEDANCE Ω (min)
LPB-5007	2:5 ±3% 4:7 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 3000
LPB-5008	1:0.83 ±3% 1:0.60 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 3,000
LPB-5009	1.4:1 ±3% 2:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.5 4-8 3.0	(1-3) 7,200
LPB-5010	1:1 ±3% 1:0.707 ±3%	1-3 1-3	4-8 5-7	1-3 3.0 4-8 3.0	(1-3) 4,000
LPB-5011	1.25:1 ±3% 1.66:1 ±3%	1-3 1-3	4-8 5-7	1-3 3.2 4-8 3.0	(1-3) 4,000
LPB-5012	2.3:1 ±3% 3.2:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.2 4-8 3.0	(5-7) 3,000
LPB-5013	2.12:1 ±3% 1.5:1 ±3%	4-8 5-7	1-3 1-3	1-3 1.1 4-8 3.0	(4-8) 4,000

SECTION K
POWER HYBRIDS

PRODUCT SUMMARY TABLE

MODEL	PACKAGE	DESCRIPTION/FEATURES	PAGE
• *MOTOR DRIVERS*			
PWR - 82331	3.0 x 2.1 x 0.390"	SMART POWER 3-PHASE MOTOR DRIVE WITH FLYBACK DIODES AND INTERNAL GATE DRIVE CIRCUITRY. 30A current capability at 200V Vcc. Each input is driven directly from a ground referenced signal with no bias voltage required. Thermal resistance of <0.85°C/W.	K-10
PWR - 82333	3.0 x 2.1 x 0.390"	SMART POWER 3-PHASE MOTOR DRIVE WITH FLYBACK DIODES AND INTERNAL GATE DRIVE CIRCUITRY. 30A current capability at 500V Vcc. Each input is driven directly from a ground referenced signal with no bias voltage required. Thermal resistance of <0.85°C/W.	
PWR - 82340	2.2 x 2.1 x 0.390"	SMART POWER MOTOR DRIVE H-BRIDGE WITH FLYBACK DIODES AND INTERNAL GATE DRIVE CIRCUITRY. 30A current capability at 200V Vcc. Each input is driven directly from a ground referenced signal with no bias voltage required. Thermal resistance of <0.85°C/W .	K-24
PWR - 82342	2.2 x 2.1 x 0.390"	SMART POWER MOTOR DRIVE H-BRIDGE WITH FLYBACK DIODES AND INTERNAL GATE DRIVE CIRCUITRY. 30A current capability at 500V Vcc. Each input is driven directly from a ground referenced signal with no bias voltage required. Thermal resistance of <0.85°C/W .	

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

BACKGROUND INFORMATION

INTRODUCTION

The trend of continuous efforts to achieve a higher degree of integration while maintaining overall reliability of military and aerospace systems resulted in higher power and current densities at chip levels. Hybridization became a major factor in the acceleration of this trend. Designers of hybrid circuits are faced with increasing demands to create unique custom high power hybrid functions which canot be achieved using any other packaging approach. High current and power densities require special consideration related to die size, total chip power, maximum junction temperature, as well as methods of mounting, material thermal characteristics, and type of external cooling. This paper concentrates on a variety of designs and manufacturing techniques and materials used in high reliability power hybrids.

IN RECENT YEARS the increasing limitations on space and weight in military and aerospace systems have increased demands to achieve a higher degree of integration while maintaining overall reliability and performance. Development of complex monolithic integrated circuits, while increasing component density, did not solve this problem, since simultaneously systems became more sophisticated. Today's high performance military equipment is literally packed with electronic systems that must be designed to provide the most efficient volume utilization. As such, these systems require new packaging techniques aimed at higher density of circuit elements and high power dissipation. Hybridization has become a major factor in acceleration of this trend.

As the electronic technology matures, the system complexity grows to include programming of functions to the specific needs of a particular user. Increased operating speed, current, and power levels present new challenges to hybrid designers who are developing new materials, processes and packaging techniques to cope with these factors. This article will take a look at the current technology of custom power hybrid design and fabrication and the materials used in their construction.

The unique requirements of custom power hybrids place special demands on selection of materials, processes, and packaging techniques. They must be constructed to be able to dissipate large amounts of heat, handle high input/output currents with minimal internal losses, be hermetically sealed, and mechanically sound.

Design Philosophy

Fundamentally, hybrid microcircuits result from combining various electronic components, materials, and manufacturing technologies and techniques into miniaturized electronic interconnections and packaging. Normally, chip and discrete components and complex monolithic integrated circuits are mounted and interconnected on a substrate and enclosed in a hybrid package. The successful development and application of a hybrid circuit starts at early

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stages of system design and requires interactions of representatives of several technical disciplines on various management levels. The effects of hybrid packaging upon subsystem performance, size, weight, and reliability must be determined by the systems engineer, while program management must be aware of the impact upon costs, schedules, and overall program goals when selecting hybrid packaging as an alternative to a discrete assembly. The circuit designers must be able to isolate groups of electronic functions within the subsystem to ensure effective performance and efficient packaging. Concurrently hybrid engineers and technologists will select the optimum combination of components, materials, and processing techniques to provide a reliable efficient and cost effective product.

Despite the enormous diversity in requirements for custom power hybrids and their applications, consistency must be maintained relative to the design, manufacture, and test of final products.

The first step in hybrid design is partitioning—the act of dividing an electronic subsystem into clearly defined subfunctions with minimal interconnection interface. For example, if the system is a radar set, the complete function is first partitioned into such sub-units as transmitters, receivers, power supply, data processor, etc. Further partitioning divides each subunit into modules—each in turn identified as a series of complete functions such as power switches, rf oscillators, voltage regulators, logic circuits, dc converters, etc., as shown in Fig. 1.

Final partitioning into hybrid circuits must take into consideration the unique advantages and limitations of hybrid technology.

Once the hybrid has been identified, the following steps must be accomplished:

1. Schematic review by hybrid designer.
2. Determination of worst case power dissipation of all components.
3. For capacitors, specify value, tolerance, dissipation factor, working voltage, and operating frequency.
4. For resistors specify value, tolerance, power dissipation, maximum voltage drop, TCR, VCR, noise and tracking requirements, active trim.
5. For active devices specify type, power dissipation, and maximum junction temperature.
6. For interconnections (wires and conductors) specify low stray capacitance lines, high voltage and high current paths.
7. For hybrid packages specify maximum allowable size, style, and material.
8. For complete hybrid circuit specify maximum operating case temperature.
9. Specify derating conditions.

These nine steps will enable the designer to select the hybrid package, substrate materials, internal construction, and processing technology. As a result, a typical custom power hybrid might consist of several parts as shown in Fig. 2. Low power circuitry is assembled on an alumina substrate (Al_2O_3) using conventional techniques and materials and attached to the case with non-conductive epoxy. High power dissipating elements are eutectically attached and wire bonded using heavy aluminum wire to beryllia (BeO) substrates which are soldered or brazed to a high thermal con- ductivity bottom case with large ($\geq 0.040''$) diameter I/O pins.

Chip Components

The design and operation of hybrid microcircuits depend largely upon the selection and characteristics of the added chip components—both passive and active.

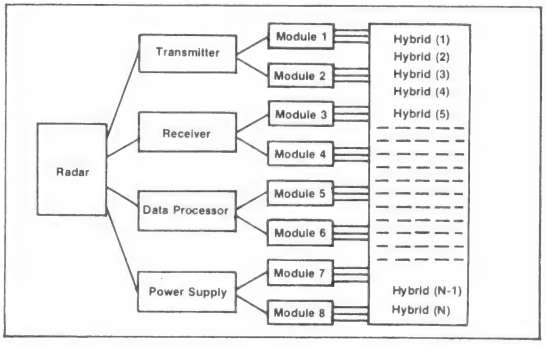

Fig. 1—System partitioning.

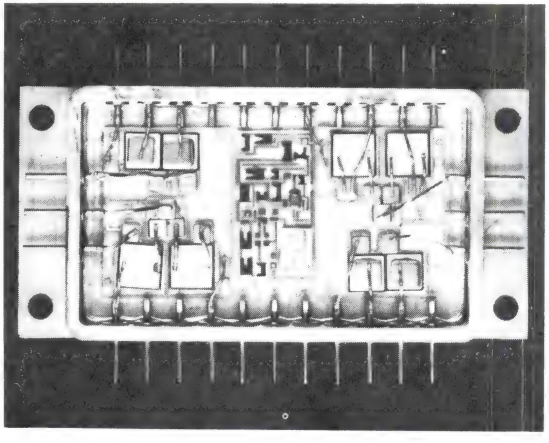

Fig. 2—FET converter/rectifier hybrid. Two power stages on BeO substrates and control circuit on alumina assembled in copper case. Power dissipation 85 W.

Most of the electronics components used in discrete printed circuit board (PCB) assemblies are also available for use in hybrid microcircuits. However, components such as transformers, switches, and large electrolytic capacitors are normally not included in hybrids because of size limitations.

The passive devices used in custom power hybrids include resistors, capacitors, and inductors.

Resistors, either thin-film or thick-film are used in chip form whenever application requirements do not exceed their maximum ratings such as: Power ≤ 250 mW; Current ≤ 0.4 A; Voltage ≤ 150 V.

In more demanding applications in power hybrids the resistors are formed directly on an alumina or beryllia substrate or are used as chips mounted on heat spreaders. Thick-film resistor inks have sheet resistivity values varying from 0.2 ohm per square to 10 megohms per square and can be trimmed to tolerances of $\pm 0.1\%$. Very low value power resistors can be manufactured exhibiting hot and cold TCRs below 500 ppm/ °C and used in sensing applications where high currents (up to 15 A) and power dissipations (up to 15 W) require good load stability. In high voltage power applications a series of resistive inks are available and are described in Table I.

Table I — Resistive Inks

Manufacturer	Sheet Resistivity Range [ohm/sq]	TCR ppm/° C	VCR ppm/V/mm	Working Voltage V/mm
A	100K-5 meg	<500	<150	400
B	10-10 meg	<300	<200	200
C	100K-1 meg	<100	<50	270

Capacitors used in power hybrids are available in a large variety of types, values, and sizes. Table II summarizes the most popular types and their major characteristics.

Table II — Capacitor Characteristics

Characteristic	NPO	BX/X7R	Solid Electrolyte Tantalum
Capacitance Range	1.0pF-0.033μF	100pF-1μF	0.1μF-100μF
Voltage Rating Range	50V - 500V	50V - 500V	4V - 50V
Size Range Inches	0.05x0.04 to 0.22x0.25	0.05x0.04 to 0.22x0.25	0.050x0.100 to 0.150x0.285

Inductors used in hybrids are in reality miniaturized coils, wound on a ferrite bobbin and molded. They are mounted on a ceramic tab with wrap-around terminals and can be assembled in a hybrid using epoxy, solder, or wire bonds. The current rating of inductors is a function of operating temperature and is determined by the properties of the wire and core material. Typical electrical characteristics of chip inductors are shown in Table III.

Table III — Electrical Characteristics of Chip Inductors

Characteristic	Range of Values
Inductance	0.01μH - 1000μH
Tolerance	10%
Q Factor	25 - 60 (min)
Current Rating	100mA to 1.3A
Size	0.100x0.100" to 0.500x0.500"
Height	0.100" to 0.400"

Active devices used in hybrid circuits essentially cover the whole spectrum of devices manufactured by the semiconductor industry such as diodes, transistors, linear and digital integrated circuits, and complex monolithic circuits.

In this article only the devices that are more frequently used in power stages of custom power hybrids are discussed. Table IV is a short summary and description of such chip components.

Power die are available to hybrid manufacturers with a variety of top and backside metallizations as shown in Table V.

The actual metallization type is determined at the time of hybrid design and strongly depends on materials used and their configuration. For example, if a large (0.25" square) chip must be mounted on a copper heat spreader, only soft solder (Pb-Sn or Pb-In-Ag) may be used for such assembly due to large thermal expansion mismatch of silicon and copper. The use of soft solder in turn limits the backside metallization to Cr/Ni/Ag, Ti/Ni/Ag, or Cr/Ni/Au types.

Table IV — Power Devices Characteristics

Device Type	Chip Size Range [inch]	Power Dissipation Range [W]	Continuous Current [A]
Power Rectifier	0.045x0.045 to 0.400x0.400	100	70
Power Transistor Bipolar	0.050x0.050 to 0.500 dia	150	50
Power Transistor MOSFET	0.045x0.045 to 0.250x0.250	150	40
Transient Suppressor Diodes	0.050 dia to 0.200 dia		100 peak

When a large Schottky rectifier is used in a high current application, a tab must be soldered to the top contact, usually the anode, to allow bonding of a heavy wire and eliminate current crowding. Such construction requires that the top metallization also be Cr/Ni/Ag (or similar).

Table V — Power Device Metallization

Device Type	Top Metal	Back Metal	Assembly Method
Power Rectifier	Cr/Ni/Au	Cr/Ni/Au	Soft solder reflow
	Al	Au	Eutectic braze
	Cr/Ni/Ag	Cr/Ni/Ag	Soft solder reflow
Power Transistor Bipolar	Al	Au	Eutectic braze
	Al	Cr/Ni/Ag	Soft solder reflow
	Al	Ti/Ni/Ag	Soft solder reflow
Power Transistor MOSFET	Al	Cr/Ni/Ag	Soft solder reflow

Materials

Substrates

Alumina ceramic substrates continue to be the most popular material for thick films because their excellent mechanical and electrical properties are retained over a wide range of applications and environmental conditions. Alumina is an inevitable choice whenever a custom power hybrid is subdivided into low and high power stages. Resistive, conductive, and dielectric patterns are screened on the substrate surface to form the required low power circuit.

Higher power densities and large amounts of heat that must be dissipated from semiconductor chips in power stages demand a material with thermal conductivity considerably higher than that of alumina, namely beryllia ceramic. This material is manufactured from beryllium oxide with minor additions (normally less than 0.5%) to promote sintering and to improve flexural strength. Beryllia ceramic requires special handling procedures because its dust, fumes, and dissolved by-products are highly toxic. For this reason cutting, grinding, machining, or abrasive resistor trimming is prohibited unless performed in specially equipped areas. Also, beryllia has a much weaker bond formation with thick film materials than alumina.

A molybdenum-manganese (Mo-Mn) metallization is used on BeO substrates when an improved adhesion is required (e.g., ceramic to metal sealing). The process is as follows: a coating of Mo-Mn is applied to the surface of beryllia ceramic. Next, the ceramic substrate is sintered in a hydrogen atmosphere. During the firing process, the Mo-Mn layer is diffused into BeO to become an integral part of the substrate. Then the metallization is plated with nickel and gold. To achieve good bonding strength, the following plating thickness parameters should be maintained: Mo-Mn: 1000–1500 micro-inches; Nickel: 150–200 micro-inches; Gold: 50 micro-inches min.

Thick Film Inks

Conductive and resistive inks consist of finely divided glass frit, metal oxide, metal powders, and organic vehicles and solvents. Dielectric inks are similar except they do not contain metallic materials. A large variety of thick film materials for use on alumina exists today and can be obtained from different vendors. Interest in beryllia applications in recent years has motivated thick film ink manufacturers to create a number of precious and non-precious material based systems for use on BeO substrates. Though poorer than Mo-Mn metallization in adhesion strength, some of them display satisfactory performance and are used in a variety of applications. Typical conductive materials are described in Table VI.

Table VI — Conductive Thick Film Inks

Manufacturer	Composition	Resistivity milliohm/sq	Application
A	Copper	1.8-2.2	Soft solder reflow Al wire bonding
	Gold	4-5	Al wire bonding
B	Platinum-Silver	3-4	Soft solder reflow
	Platinum-Gold	75-80	High temp braze
	Gold	5-6	Al wire bonding
	Gold	2.5-5	Au wire bonding
	Copper	1.5-2	Soft solder reflow Al wire bonding
C	Platinum-Silver		Soft solder reflow
	Gold	2-4	Au and Al wire bonding
	Platinum-Gold	30-50	High temp braze

Wires

Normally gold and aluminum wires are used in hybrids for electrical interconnections at substrate level and to the package pins. They are available in different sizes. 0.0007″ to 0.002″ diameter for gold and 0.001″ to 0.25″ diameter for aluminum. Final selection of wire material, diameter, and shape depends on current carrying requirements, metallizations compatibility, and type of equipment used for bonding. A trade-off decision must be made at the time of hybrid design on a conductor/wire system. High currents are easily handled by large diameter aluminum wire, but it requires conductors with a hard surface which have high electrical resistivity that might influence the circuit performance. Special applications might require gold ribbon (up to 0.003″×0.010″) or plated copper wire for high current handling with very low losses.

Heat Spreaders

In certain applications, when power dissipation of active components is moderate, the use of a heat spreader placed between the semiconductor chip and the substrate can be sufficient to eliminate the necessity of an expensive beryllia substrate and/or costly header. Heat spreaders are made

from BeO, molybdenum, or copper and provide the designer with a choice of various thermal conductivities. BeO spreaders are used when high thermal conductivity and electrical isolation are required. Molybdenum tabs are used when close thermal expansion matching is desirable and allows hard brazing of the chip. Copper is used alone or in conjunction with molybdenum and provides the most efficient heat transfer.

Solder

Solder is a fusible alloy composition that will go into solution or "wet" two metal surfaces to create a metallurgical joint, when heated above its melting point. Various forms of solder have been used by the electronics industry long before development of hybrid technology. Unfortunately, no standards have been developed for solder used in hybrid microelectronics and each power hybrid manufacturer uses in-house developed guidelines. Since replacement of defective devices in power hybrids is considered essential, several types of solder may be employed in one package. Beryllia substrates can be soldered to the package bottom with a lower melting temperature solder than the power dissipating components. That allows the substrates to be removed and reworked if a failure occurs. The alternative approach is to use a lower melting temperature solder for component assembly so that a defective chip can be removed by localized reflow. For use in power hybrids the solder system is selected on the basis of melting temperature, mechanical strength, and compatibility with soldered materials. Frequently used solders and their characteristics are shown in Table VII.

Packages

Power hybrid packages must provide an efficient thermal transfer from heat generating components to the cooling media. They are required to have high heat capacity, low weight, be compatible with substrate materials, and be capable of handling high currents with low voltage drops across the leads. Obviously it is very difficult to meet all these requirements simultaneously, and therefore a power package often is tailored to a specific design. An overwhelming majority of power packages have a flatpack configuration and vary in material selection, size, shape, plating, etc. Plug-in construction is very inefficient in heat transfer and is basically limited to Kovar as bottom material. Figure 3 shows typical power packages used in hybrid manufacturing. Three main types are:

1. Solid copper machined packages with soldered-in terminals. Heavy gauge solid Kovar or copper cored leads are glass sealed in a low expansion metal tube or brazed to a ceramic sealing ring and later are brazed into the package walls using low temperature braze to avoid annealing of the copper. A sealing ring is brazed to the top of the package to allow parallel seam-welding of the cover.
2. Kovar ring frame with matched glass-to-metal sealed leads brazed to a molybdenum bottom using gold-germanium (356 °C) brazing alloy. Solid Kovar or copper cored leads can be used to handle high currents.
3. Same as 2 with exception that a metallized beryllia substrate is used in place of a molybdenum bottom.

Gold is selected for plating due to good wetting by most solder or braze materials. Other materials such as zirconium-copper or tungsten-copper may be used in power package construction but have not yet gained recognition. It can be noted that the braze material used in two piece configuration does not exceed 356 °C, which limits the choice of solder materials used in hybrid construction.

Table VII — Solder Charateristics

Alloy Composition	Melting Point [°C]	Application
62% Tin, 36% Lead, 2% Silver	177-189	Silver backed die reflow on silver bearing conductors
50% Indium, 50% Lead	180-209	Silver or gold backed die reflow. Good fatigue resistance
63% Tin, 37% Lead	183 (eut)	Soft solder against silver metallizations
95% Tin, 5% Lead	183-222	High strength solder
55% Indium, 45% Lead	215 (eut)	Same as 50-50 composition
96.5% Tin, 3.5% Silver	221 (eut)	Substrate mount in package. Silver backed die flow
92.5% Lead, 5% Tin, 2.5% Silver	280 (eut)	Same
80% Gold, 20% Tin	280 (eut)	Hard braze of gold metallizations
92.5% Lead, 5% Indium, 2.5% Silver	307 (eut)	Very good fatigue resistance, not for use at elevated temperatures
88% Gold, 12% Germanium	356 (eut)	Hybrid case assembly. Eutectic braze of silicon die
98% Gold, 2% Silver	370-940	Eutectic braze silicon die

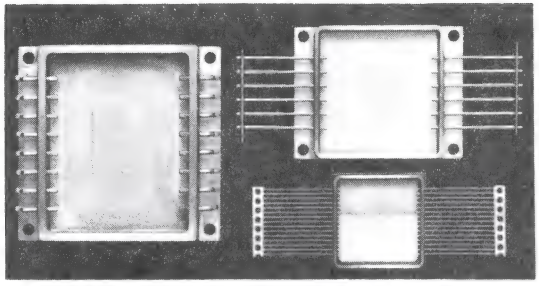

Fig. 3—Typical power packages. (a) Solid machined copper; (b) Molybdenum bottom with Kovar ring frame; (c) BeO bottom with Kovar ring frame.

Thermal Management

Continuing effort to create more sophisticated and reliable systems puts an emphasis on increasing hybrid power densities and improving their thermal characteristics. The useful lifetime of a semiconductor device is related to its junction temperature. The variation of failure rate with temperature is an exponential function. For example, a change of junction temperature from 100 °C to 125 °C will increase the failure rate by a factor of more than 5. Also, the maximum allowable power dissipation in a solid state device is limited by its junction temperature. This mandates two major objectives of thermal management.

First, thermal circuit analysis and thermal fatigue considerations. Initial thermal analysis should identify hot components that have to be thermally partitioned and provide their expected junction temperatures. Figure 4 shows (a) thermal conductivity and (b) thermal expansion as a function of temperature for various materials used in power hybrids. Note a sharp decline in thermal conductivity (almost 3–4 times) for beryllia ceramic in the −55 °C to 125 °C range. When performing thermal analysis, a designer must take such dependence into careful consideration. When a semiconductor device is subjected to a range of temperatures in the course of assembly, environmental testing, and normal operations, the different coefficients of expansion result in stresses on various parts of the device structure. When the stresses are severe enough and are repeated enough times, they can cause the semiconductor device to fail, usually by rupture of the solder joints. For example, large power transistors that operate at very high power levels as pass devices in linear series regulators operate in a mode of high thermal fatigue stress. The average junction temperature T_j of such transistors may be calculated as follows:

$$T_j = T_c + P_{avg}\theta_{jc}$$

where T_c is the case temperature in °C, θ_{jc} is the junction to case thermal resistance in °C/W and P_{avg} is an average dissipated power.

However, the power dissipated in a transistor is nonlinear with respect to the surface and junction temperature,

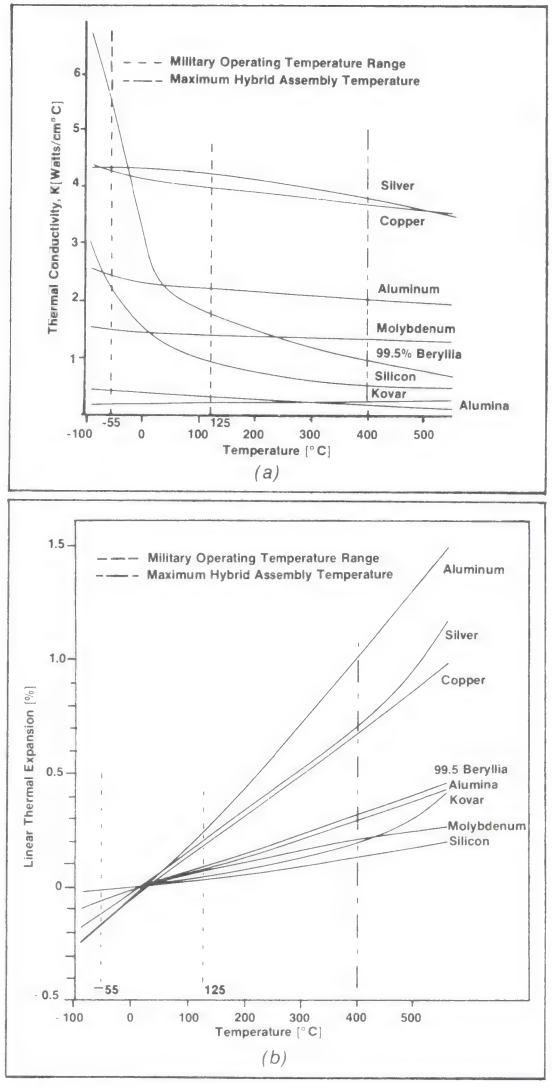

Fig. 4—Thermal properties of typical materials used in power hybrid construction. (a) Thermal Conductivity vs. Temperature; (b) Thermal Expansion vs. Temperature.

and can vary from point to point on the chip as shown in Fig. 5. As a result of current-crowding, a localized thermal runaway may occur and result in permanent damage as shown in Fig. 6. Excessive voiding in the thermal interface will enhance such a process.

The second objective is junction temperature monitoring and process control. The small size of hybrid components makes it impossible to measure the junction temperature using conventional thermocouples and probes.

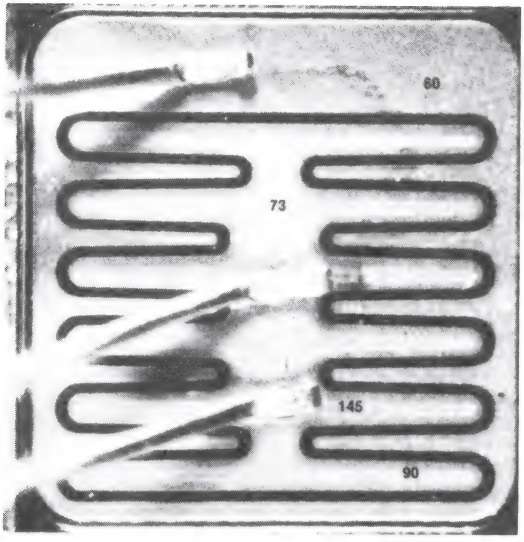

Fig. 5—Thermal gradient distribution on chip surface (°C).

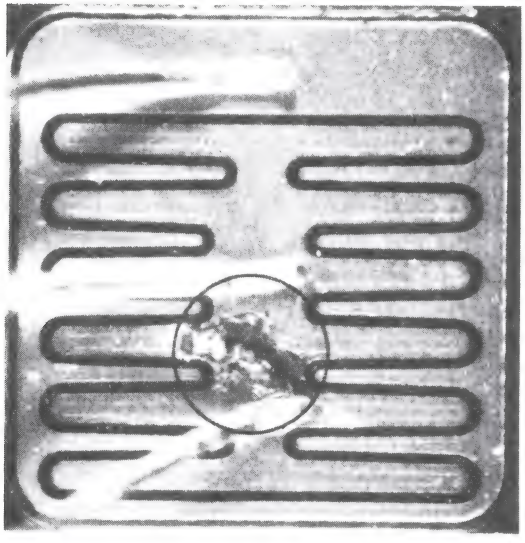

Fig. 6—Transistor thermal overstress. Damage shown in circle.

There are four basic methods of monitoring die attachment integrity, by either indirectly evaluating the quality of the thermal interface of junction to case (die shear, x-ray, thermal transient test) or direct temperature measurement on the chip surface (infrared scanning).

Die Shear: A force is applied to the edge of mounted die for a purpose of either rupturing the joint or fracturing the die. This method is destructive and can be used only on a sample basis.

X-Ray Photography: A die-substrate-header assembly is positioned on top of photographic film and then exposed to a beam of x-rays. This method is expensive, involves subjective interpretation of the picture, and cannot be used with dense and x-ray absorbent materials such as molybdenum and copper.

Thermal Transient: A temperature sensitive parameter (TSP) is monitored before and after application of an electrical power pulse applied to the device under test. The difference in TSP measurements is directly proportional to the junction temperature. Although non-destructive and accurate, this method requires access to a single chip, and is lot and vendor sensitive.

Infrared Scanning: All materials, when heated, emit infrared energy with intensity directly related to the temperature. A lens collects and focuses infrared energy onto a detector. When processed, the information can be read out in °C on a display device. This method provides a non-destructive accurate temperature readout of an entire hybrid or a single chip. However, it is relatively slow for production environment, involves expensive equipment, and can be effectively used only after the hybrid is completely assembled, which eliminates the possibility of die attachment process control.

Power Hybrid Assembly

The assembly of a power hybrid includes mounting of active and passive components onto ceramic substrates (alumina and beryllia), then assembly of substrates in a case, wirebonding and package sealing.

Passive device (chip capacitors, resistors, and inductors) mounting utilizes either solder or conductive and non-conductive adhesives. The adhesive attachments exhibit good strength and are preferred when very low contact resistance is not required.

Active devices are attached using materials and techniques required to meet thermal resistance limits. Typically low power components would be mounted with conductive adhesive. High power dissipating chips may be attached by using either of the following soldering methods: (a) Eutectic solder directly to the substrate metallization or a molytab with subsequent soldering of the tab to the substrate. If eutectic bonding directly to the substrate is used it must be performed before the substrate is assembled into the case. (b) Soft solder directly to the substrate metallization. This method is used mostly when die backside metallization is Ni/Ag and can be performed before or after substrate assembly in the case.

Two main techniques are available for substrate attachment to case, adhesive and solder. Adhesive is a commonly used material and represents a conventional means of substrate mounting. This method doesn't require gold

plating of the package and the backside of the substrate is bare ceramic. Solder is used mostly in applications where low thermal resistance is mandatory. However, gold plating of packages and metallization of the backside of the substrate are required. The use of solder requires very careful process control to eliminate a possibility of voids. The metallization material has to be compatible with the solder system used for reflow so that no leaching of the conductor will take place resulting in void areas.

The reflow techniques and equipment used in power hybrid assembly are as follows:

- Hot plates and heated surfaces. Used for small prototype quantities and must use flux if performed in open air. Requires scrubbing of die.
- Ovens. Poor control and low quality of attachment.
- Vacuum bell jar with induction or infrared heating. Slow method, requires very tight process controls.
- Vapor phase soldering. Used mostly for surface mounted device assembly.
- Belt furnace. Employs nitrogen, forming gas, or pure hydrogen to enhance wetting and prevent oxidation. Excellent quality reflow. Requires large quantities of hybrids to be cost effective. Certain devices and materials might be affected if reflow temperatures exceed 350°C.

The interconnections within a hybrid circuit are made by thermosonic, thermocompression, or ultrasonic techniques. Most low power devices are bonded using thermosonic or thermocompression methods utilizing 1 or 2 mil gold wires. For very small bonding pads 0.7 mil gold wire can be used.

For safe handling of high currents large diameter (up to 25 mil) aluminum wires are ultrasonically bonded to hybrid pins, substrate pads, and power die terminals. During this process two pieces of metal are joined by a form of diffusion bonding. The metals are clamped together and vibrate at ultrasonic frequency. The mechanical vibration breaks the surface oxide film and exposes clean metallic surfaces. The plastic deformation prompted by the mechanical force causes a joint of two crystal lattices creating a strong, bonded monolithic structure at the bond line. A less popular alternative technique for high current handling is parallel-gap welding.

Sealing of the hybrid is performed in a dry nitrogen atmosphere. Packages are hermetically sealed by resistance weldings of the lid to the case. Resistance welding utilizes the resistance of the metal to the flow of electric current to heat the metal in a very small area and create a weld.

Summary

The increasing complexity of power hybrids over the last decade and a trend toward higher reliability at increased power density levels became an incentive for the accelerated development of new techniques, new equipment, and high performance materials. Although much has been done during this period, a better understanding of the relationship of modern technology and materials to the power hybrid mechanical and electrical performance is required.

This article reviewed the latest trends in power hybrid design and manufacturing, discussed the importance of careful selection of materials, and analyzed the methods of thermal measurements and control. We also saw that overstressing of a semiconductor device may lead to its destruction and discussed methods to avoid it. Since thermal properties of metals and ceramics vary significantly with temperature, they should be considered in hybrid design and analysis.

Finally, it should be noted that continuous improvement and development of materials, production techniques and equipment, standards and test methods are vital to successful growth of power hybrid technology.

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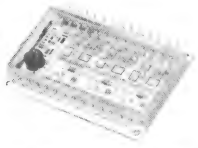
DDC
ILC DATA DEVICE CORPORATION

PWR-82331 and PWR-82333

SMART POWER 3-PHASE MOTOR DRIVES



DESCRIPTION

The PWR-82331 and PWR-82333 are 30A 3-phase motor drive hybrids. The PWR-82331 has a 200V rating and uses MOSFETs in the output stage while the PWR-82333 has a 500V rating and an IGBT output stage. Both types have individual fast recovery diodes internally connected across the output drive transistors to clamp inductive flyback.

This new series of Smart Power Motor Drives has CMOS Schmitt Trigger inputs for high noise immunity. High- and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn on of in-line transistors, thus eliminating a shoot thru condition. The internal logic controls the high- and low-side gate drives for each phase and can operate from 5 to 15V logic levels.

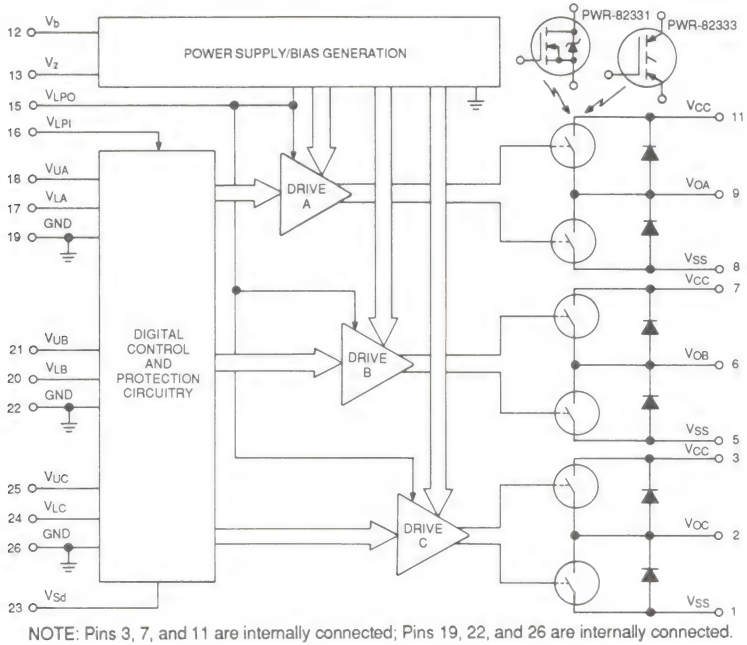
The internal power supply provides a constant voltage source to the floating high-side gate drives. This provides constant output performance for switching frequencies from dc to 50 kHz.

APPLICATIONS

Packaged in small cases, these hybrids are an excellent choice for high-performance, high-reliability motor drives for Military and Aerospace servo-amps and speed controls. Among the many applications are robotics; electro-mechanical valve assemblies; actuator systems for flight control surfaces on military and commercial aircraft; antenna and radar positioning; fan and blower motors for environmental conditioning; thrust and vector position control of mini-subs, drones, and RPV's; compressor motors for cryogenic coolers; and high-power inverters. The PWR-82331/333 hybrids are ideal for harsh military environments where shock, vibration, and temperature extremes are evident, such as missile applications where fin actuator systems control missile direction. The PWR-82331/333 operates over the -55°C to +125°C temperature range and is available with military processing.

FEATURES

- ***Small Size (3.0" x 2.1" x 0.39")***
- ***200V & 500V Capability***
- ***30A Current Capability***
- ***High-Efficiency MOSFET or IGBT Drive Stage***
- ***Direct Drive from Commutation Logic***
- ***6 step Trapezoidal or Sinusoidal Drive***
- ***Four Quadrant Operation***
- ***0.85°C/W θ_{j-c} Max***
- ***Military Processing Available***



NOTE: Pins 3, 7, and 11 are internally connected; Pins 19, 22, and 26 are internally connected.

FIGURE 1. PWR-82331/333 BLOCK DIAGRAM

TABLE 1. ABSOLUTE MAXIMUM RATINGS

(T_C = +25°C unless otherwise specified)

PARAMETER	SYMBOL	PWR-82331 VALUE	PWR-82333 VALUE	UNITS
SUPPLY VOLTAGE	V_{CC}	200	500	V
BIAS VOLTAGE	V_b	50	50	V
LOGIC POWER-IN VOLTAGE	V_{LPI}	18	18	V
INPUT LOGIC VOLTAGE	V_U, V_L, V_{Sd}	V_{LPI}+ 0.5	V_{LPI}+ 0.5	V
OUTPUT CURRENT				
CONTINUOUS	I_o	30	30	A
PULSED	I_{op}	50	50	A
OPERATING FREQUENCY	f_o	50	25	kHz
CASE OPERATING TEMPERATURE	T_C	– 55 to +125	– 55 to +125	°C
CASE STORAGE TEMPERATURE RANGE	T_{CS}	– 55 to +150	– 55 to +150	°C

TABLE 2. PWR-82331 and PWR-82333 SPECIFICATIONS (T_C = +25°C unless otherwise specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	PWR-82331 MIN	PWR-82331 TYP	PWR-82331 MAX	PWR-82333 MIN	PWR-82333 TYP	PWR-82333 MAX	UNIT
OUTPUT									
Output Current Continuous (see figures 19 and 15)	I_o				30			30	A
Supply Voltage	V_{CC}	see note 1		140	200		270	500	V
Output On-Resistance (each FET)(see figure 14A)	R_{on}	I_o=30A			0.1				ohm
Output Voltage Drop (each IGBT)(see figures 14B)	$V_{CE(SAT)}$	I_o=30A						3.8	V
Instant. Forward Voltage (flyback diode)(see figure 13)	V_F	I_p=30A (see note 2)			1.15			1.70	V
Reverse Recovery Time (flyback diode)	t_{rr}	I_f=1A, I_r=1A			50			50	nsec
Reverse Leakage Current at T_C=25°C	I_r	see note 3			10			10	µA
Reverse Leakage Current at T_C=125°C	I_r	see note 3			1			1	mA
BIAS SUPPLY									
Input Bias Voltage (T_C = -55 to +125°C)	V_b		15		50	15		50	V
Quiescent Bias Current (see note 4)(see figure 16)	I_{bq}	V_b = 28V		32			32		mA
Bias Current (T_C = -55 to +125°C)(see figures 17 and 18)	I_b	V_b = 28V,(see note 5)	35		65	35		65	mA
In-rush Current (T_C = -55 to +125°C)	I_{ir}	V_b = 28V			1.4			1.4	A
Logic Power Input Current	I_{LPI}	see note 6			2			2	mA
INPUT SIGNALS (see figure 7)		**Pin Connections**							
Positive Trigger Threshold Voltage	V_P	pin 15 & 16 connected	6.8		10	6.8		10	V
Negative Trigger Threshold Voltage	V_N	pin 15 & 16 connected	4.0		7	4.0		7	V
Positive Trigger Threshold Voltage	V_P	see note 6	2.2		3	2.2		3	V
Negative Trigger Threshold Voltage	V_N	see note 6	0.9		2	0.9		2	V
SWITCHING CHARACTERISTICS		**Test 1 Conditions**							
(see figure 2)		pin 15 & 16 connected							
Upper Drive:		+15V logic							
Turn-on propagation delay	t_d (on)	I_o = 30A peak			440			410	nsec
Turn-off propagation delay	t_d (off)	PWR-82331 V_{CC}= 140V			620			460	nsec
Shut-down propagation delay	t_{Sd}	PWR-82333 V_{CC}= 270V			400			410	nsec
Turn-on Rise Time	t_r				125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec
LowerDrive:									
Turn-on propagation delay	t_d (on)				450			400	nsec
Turn-off propagation delay	t_d (off)				600			470	nsec
Shut-down propagation delay (see figure 9)	t_{Sd}				400			370	nsec
Turn-on Rise Time	t_r				125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec
SWITCHING CHARACTERISTICS		**Test 2 Conditions**							
(see figure 2)		see note 6							
Upper Drive:		+5V logic							
Turn-on propagation delay	t_d (on)	I_o = 30A peak			690			650	nsec
Turn-off propagation delay	t_d (off)	PWR-82331 V_{CC}= 140V			915			750	nsec
Shut-down propagation delay	t_{Sd}	PWR-82333 V_{CC}= 270V			700			450	nsec
Turn-on Rise Time	t_r				125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec

K

TABLE 2. PWR-82331 and PWR-82333 SPECIFICATIONS (continued) (T_C = +25°C unless otherwise specified)

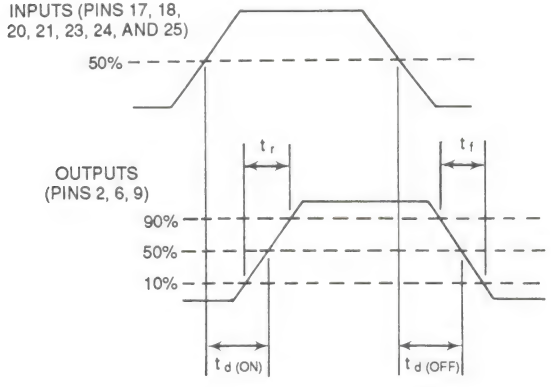
PARAMETERS	SYMBOL	TEST CONDITIONS	PWR-82331 MIN	PWR-82331 TYP	PWR-82331 MAX	PWR-82333 MIN	PWR-82333 TYP	PWR-82333 MAX	UNIT
SWITCHING CHARACTERISTICS (continued)		**Test 2 Conditions**							
LowerDrive:		see note 6							
Turn-on propagation delay	t_d (on)	+5V logic			725			650	nsec
Turn-off propagation delay	t_d (off)	I_o = 30A peak			890			750	nsec
Shut-down propagation delay (see figure 9)	t_{Sd}	PWR-82331 V_{CC}= 140V			700			450	nsec
Turn-on Rise Time	t_r	PWR-82333 V_{CC}= 270V			125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec
DEAD TIME	t_{dt}		400			500			nsec
MINIMUM PULSE WIDTH	t_{pw}		150			175			nsec
THERMAL									
Maximum Thermal Resistance	θ_{j-c}	each transistor			0.85			0.85	°C/W
Maximum Lead Soldering Temp.	T_s	see note 7			250			250	°C
Junction Temperature Range	T_j		-55		150	-55		150	°C
Case Operating Temperature	T_{co}		-55		125	-55		125	°C
Case Storage Temperature	T_{cs}		-55		150	-55		150	°C
WEIGHT					4.9 (140)			4.9 (140)	oz(g)

NOTES:
1. For Hi-Rel applications, derating per MIL-S-19500 should be observed. (Derate V_{CC} by 70%.)
2. Pulse width ≤ 300 µs, duty cycle ≤ 2%.
3. For PWR-82231 V_{CC}=140V, V_U,V_L= logic '0' and for PWR-82233 V_{CC}=350V, V_U,V_L= logic '0'.
4. V_U, V_L = logic '0' on pins 17, 18, 20,21,24, and 25.
5. For PWR-82231 f_o = 30kHz and for PWR-82233 f_o = 10kHz.
6. Pin 16 connected to external +5V supply.
7. Solder 1/8" from case for 5 seconds maximum.

TECHNICAL INFORMATION

Introduction

The 3 phase PWR-82331 & PWR-82333 are 30A motor drive hybrids rated at 200V and 500V respectively. The PWR82331 uses a MOSFET output stage and the PWR-82333 has an IGBT output stage for high-speed, high-current, and high-efficiency operation. The PWR-82333 also offers high-voltage performance of an IGBT for use in 270V systems. These motor drives are ideal for use in high-performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, Multi-axis systems requiring multiple drive stages can benefit from the small size of these power drives.



(REFERENCE TABLE 1 ALSO.)

FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS.

The PWR-82331/333 can be driven directly from the commutation logic, DSP, or a custom ASIC that supplies digital signals to control the upper and lower transistors of each phase. These highly integrated drive stages have Schmitt trigger digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition, by preventing simultaneous turn-on of both the upper and lower transistors. The logic controls the high- and low-side gate drivers. Operation from 5 to 15V logic levels can be programmed by applying the appropriate voltage to pin 16 (V_{LPI}). The PWR-82331/333 has a ground referenced low-side gate drive. An internal dc-dc converter supplies a floating output to each of the 3 high-side drives. This provides a continious high-side gate drive even during a motor stall. Pin 15 (V_{LPO}) supplies a 15V output, which can be used to power the internal logic when system useage requires 15V logic. The high- and low-side gate drivers control the N-channel MOSFET or IGBT output stage. The MOSFETs used in the PWR-82331 allow output switching up to 50kHz, while the high-speed IGBTs in the PWR-82333 can switch at 25kHz. A flyback diode parallels each output transistor and controls the regenerative energy produced by the motor. These fast recovery diodes have faster reverse switching times than the intrinsic body diode of the MOSFETs used in the PWR-82331. They also protect the IGBTs used in the PWR-82333 from exceeding their Emitter-to-Collector breakdown voltage. Use of a copper case and solder attachment of the output transistors achieves a low thermal resistance of 0.85°C/W maximum. Care should be taken to adequately heatsink these motor drives to maintain a case temperature of 125°C. Junction temperatures should not exceed 150°C. The PWR-82331/333 do not have internal short-circuit or overcurrent protection. For protection of the output transistors, these features must be added external to the hybrid.

Bias Voltages

The PWR-82331/333 motor drive hybrids require only a single power supply for operation. The hybrid generates three independent, floating supplies, which eliminates the need for external bias voltages for each phase.

In order for the internal power supply to generate these voltages, the input bias voltage (V_b) must be from 15 to 50 Vdc. In most avionic systems this can be accomplished by connecting the V_b pin to the MIL-STD-704D, 28 Volt bus. See figure 3a.

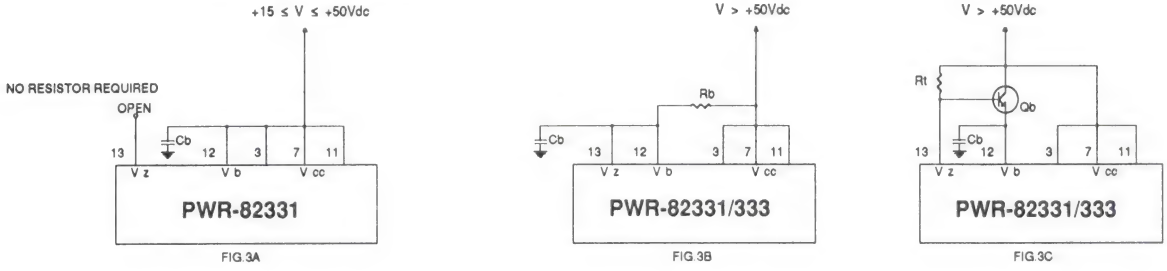
If the system bus voltage is greater than 50 Vdc (and a lower voltage is not available), then the V_b pin and V_z pin can be tied together with an external power resistor (R_b) and connected from these pins to the system power bus. See figure 3b.

See figures 4 and 5 for bias resistor characteristics.

If additional power dissipation in R_b is a concern, figure 3c shows a more efficient design, using a low-power resistor (R_T) and an additional transistor. To determine the proper resistor to use, refer to figure 6.

If there is another voltage available in the system in the 15 to 50 Vdc range, then this voltage can be directly connected to the V_b pin of the hybrid.

In any case, a 0.01 µf decoupling capacitor (C_b) must be connected between V_b (pin 12) and GND.



NOTE: Cb = 0.01uf, 100V, CERAMIC ; FOR PWR-82331, Qb = 200V, 6W TRANSISTOR ; FOR PWR-82333, Qb = 500V, 12W TRANSISTOR

FIGURE 3. CONNECTION TO BUS VOLTAGE TO DEVELOP PROPER INPUT BIAS VOLTAGE.

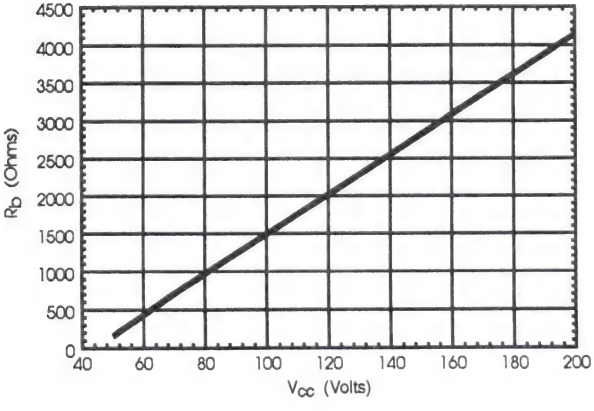


Figure 4a. PWR-82331

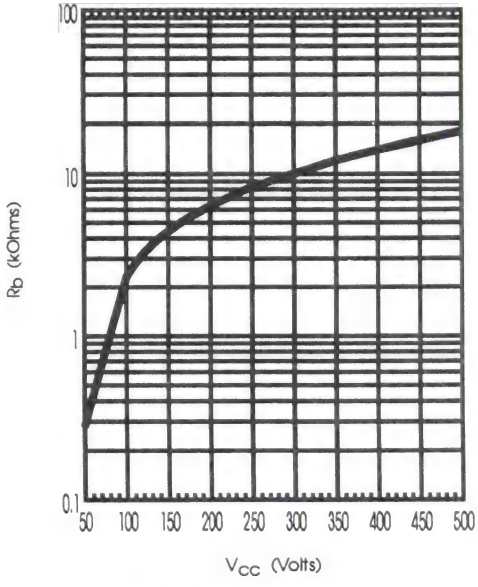


Figure 4b. PWR-82333

FIGURE 4. BIAS RESISTOR VALUE VS. BUS VOLTAGE

K

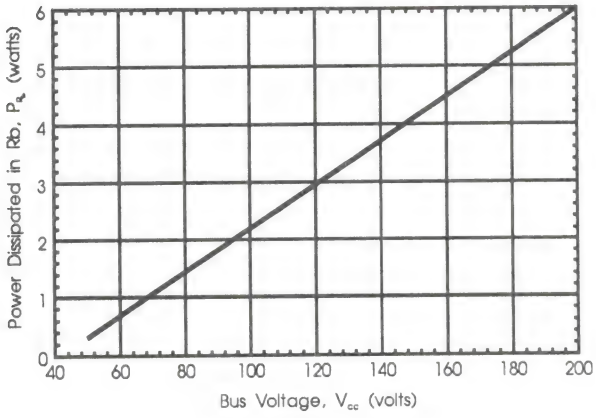


Figure 5a. PWR-82331

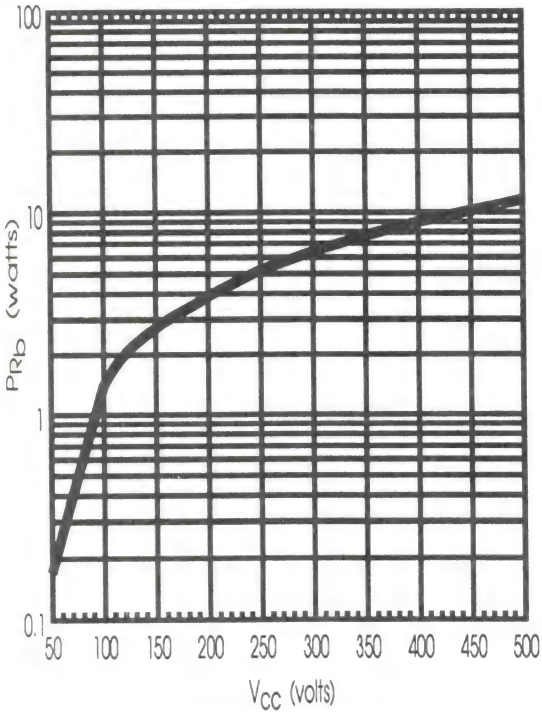


Figure 5b. PWR-82333

FIGURE 5. POWER DISSIPATED IN BIAS RESISTOR (R_b) VS. BUS VOLTAGE

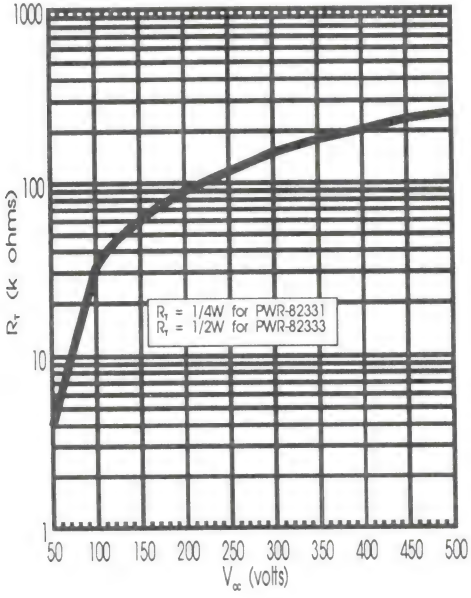


FIGURE 6. R_T RESISTOR VALUE VS. BUS VOLTAGE

Digitally Controlled Inputs

The PWR-82331/333 uses Schmitt triggered digital inputs (with hysteresis) to ensure high-noise immunity. The trigger switches at different points for positive and negative going signals. Hysteresis voltage (V_H) is the difference between the positive going voltage (V_P) and the negative going voltage (V_N) (see figure 7). The digital inputs have programmable logic levels, which allows the hybrid to be used with different types of commutation logic with an input voltage range of 5-15V, such as TTL or CMOS logic. The PWR-82331/333 internal power supply generates a 15Vdc (V_{LPO}) on pin 15. This output can only be used to power the internal digital circuitry within the hybrid. **Do not use this 15V output to power any circuitry external to the hybrid.** Pin 16 is the logic power input (V_{LPI}) for the digital circuitry inside the hybrid. **A 0.01uF, 50V ceramic capacitor must be placed between this pin (16) and GND as close to the hybrid as possible.** When using 15V control circuitry, the logic power input (pin 16) can be connected directly to the logic power output (pin 15) of the hybrid. There is no need for an additional external power supply. **When using 5V control logic, an external 5Vdc supply must be connected between pin 16 of the hybrid, and GND — leave Pin 15 open (N/C).** The commutation/control circuitry can be as simple as discrete logic with PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. The Block Diagram in figure 8 shows a typical interface of the PWR-82331/333 with a motor and commutation logic in a Servo-Amp System.

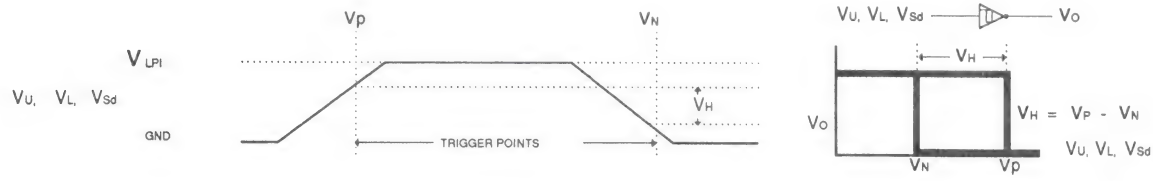
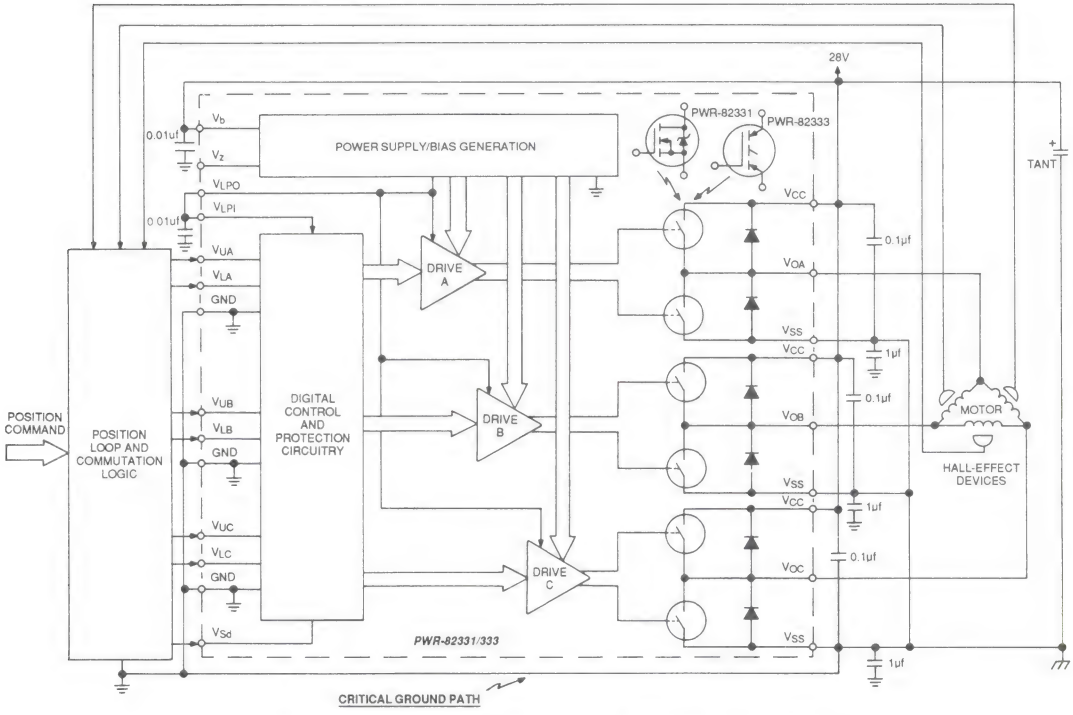


FIGURE 7. HYSTERESIS DEFINITION AND CHARACTERISTICS



To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 19,22,26) and V_{SS} (pins 1,5,8) must not exceed ±3V max, dc or peak.

FIGURE 8. PWR-82331/333 TYPICAL INTERFACE WITH A MOTOR AND COMMUTATION LOGIC.

Shut-Down Input (V_{Sd})

Pin 23(V_{Sd}) provides a digital shut-down input, which allows the user to completely turn off both the upper- and lower-output transistors in all 3 phases. Application of a logic '1' to the V_{Sd} input will latch the Digital Control/Protection circuitry thereby turning off all output transistors. The Digital Control/Protection circuitry remains latched in the off state and will not respond to signals on the V_L or V_U inputs while the V_{Sd} has a logic '1' applied. When the user or the sense circuitry (as in figure 10) returns the V_{Sd} input to a logic '0', and then the user sets the V_L and V_U inputs to a logic '0' the output of the Digital Control/Protection circuitry will clear the internal latch. When the next rising edge (see figure 9) occurs on the V_L or V_U digital inputs, the output transistors will respond to the corresponding digital input. This feature can be used with external current limit or temperature sense circuitry to disable the drive if a fault condition occurs(see figure 10).

Internal Protection Circuitry

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. The circuitry allows only proper input signal patterns to cause output conduction. Figure 9 and Table 3 show these timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR-82331/333. **A dead time of 500nsec minimum should still be maintained** between the signals at the V_U and V_L pins; this ensures the complete turn off of any transistor before turning on its associated in-line transistor.

FIGURE 9. SHUT-DOWN (V_{Sd}) TIMING RELATIONSHIPS.

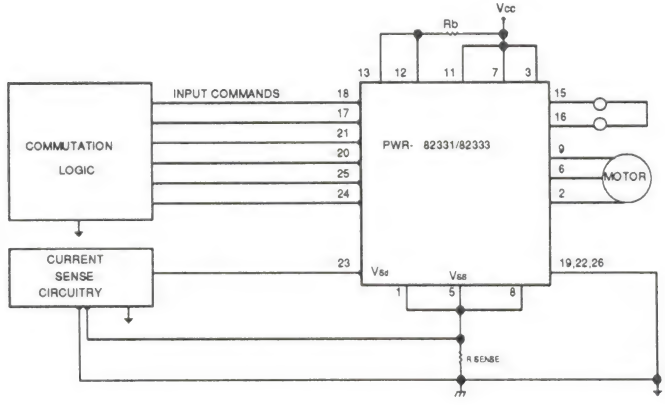


FIGURE 10. FUNCTIONAL SHUT-DOWN INPUT USED WITH CURRENT-SENSING CIRCUITRY.

PWR-82331 Power Dissipation (see figure 11)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

V_{CC} = 140V(Bus Voltage)
I_{OA} = 20A (see figure 11) ; I_{OB} = 30A; (see figure 11)
t_{on} = 20µs (see figure 11); T = 40µs (period)
R_{on} = 0.1 Ω (on-resistance see Table 2, I_o = 30A, T_c = 25°C)
t_{s1} = 250ns (see figure 11); t_{s2} = 250ns (see figure 11)
f_o = 25kHz(switching frequency)
V_f is the diode forward voltage, Table 2, I_o = 30A,T_c = 25°C
V_f(avg) = 1.15V; I_f is the diode forward current

1. Conduction Losses (P_C)

P_C = (I motor rms)^2 x R_{on}

$$\text{I motor rms} = \sqrt{\left(I_{OB}^2 - I_{OB}(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^2}{3}\right)\left(\frac{t_{on}}{T}\right)}$$

$$\text{I motor rms} = \sqrt{\left(30^2 - 30(30 - 20) + \frac{(30 - 20)^2}{3}\right)\left(\frac{20}{40}\right)}$$

$P_C = (17.80A)^2$ x (0.1 Ω)
P_C = 31.68 Watts

2. Switching Losses (P_S)

$P_S = [V_{CC}(I_{OA}(t_{s1}) + I_{OB}(t_{s2}))f_o]/2$
$P_S = [140(20\ (250ns) + 30(250ns))25k]/2$
P_S = 21.88 Watts

3. Flyback diode loses (P_{df})

$P_{df} = I_f$ (avg) x V_f (avg)
I_f (avg) = $[(I_{OB} + I_{OA})/2]/2 = [(30 + 20)/2]/2$ = 12.5A
P_{df} = 12.5A x 1.15V
P_{df} = 14.38 Watts

Transistor Power Dissipation (P_Q)

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference figure 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

Total Hybrid Power Dissipation (P_{Total})

To calculate Total Power dissipated in the hybrid use:

$$P_{Total} = \sum_{i=1}^{6} [P_{Qi} + P_{dfi}]$$ where i = each transistor or diode.

PWR-82333 Power Dissipation (see figure 11)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

V_{CC} = 270V(Bus Voltage)
I_{OA} = 20A (see figure 11) ; I_{OB} = 30A; (see figure 11)
t_{on} = 50µs (see figure 11); T = 100µs (period)
$V_{CE(SAT)}$ = 3.8 V (see Table 2, I_o = 30A, T_c = 25°C)
t_{s1} = 300ns (see figure 11); t_{s2} = 300ns (see figure 11)
f_o = 10kHz(switching frequency)
V_f is the diode forward voltage, Table 2, I_o = 30A,T_c = 25°C
V_f(avg) = 1.70V; I_f is the diode forward current

1. Conduction Losses (P_C)

P_C = (I motor rms) x $V_{CE(SAT)}$

$$\text{I motor rms} = \sqrt{\left(I_{OB}^2 - I_{OB}(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^2}{3}\right)\left(\frac{t_{on}}{T}\right)}$$

$$\text{I motor rms} = \sqrt{\left(30^2 - 30(30 - 20) + \frac{(30 - 20)^2}{3}\right)\left(\frac{50}{100}\right)}$$

P_C = (17.80A) x (3.8V)
P_C = 67.64 Watts

2. Switching Losses (P_S)

$P_S = [V_{CC}(I_{OA}(t_{s1}) + I_{OB}(t_{s2}))f_o]/2$
$P_S = [270(20\ (300ns) + 30(300ns))10k]/2$
P_S = 20.25 Watts

3. Flyback diode loses (P_{df})

$P_{df} = I_f$ (avg) x V_f (avg)
I_f (avg) = $[(I_{OB} + I_{OA})/2]/2 = [(30 + 20)/2]/2$ = 12.5A
P_{df} = 12.5A x 1.70V
P_{df} = 21.25 Watts

Transistor Power Dissipation (P_Q)

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference figure 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

Total Hybrid Power Dissipation (P_{Total})

To calculate Total Power dissipated in the hybrid use:

$$P_{Total} = \sum_{i=1}^{6} [P_{Qi} + P_{dfi}]$$ where i = each transistor or diode.

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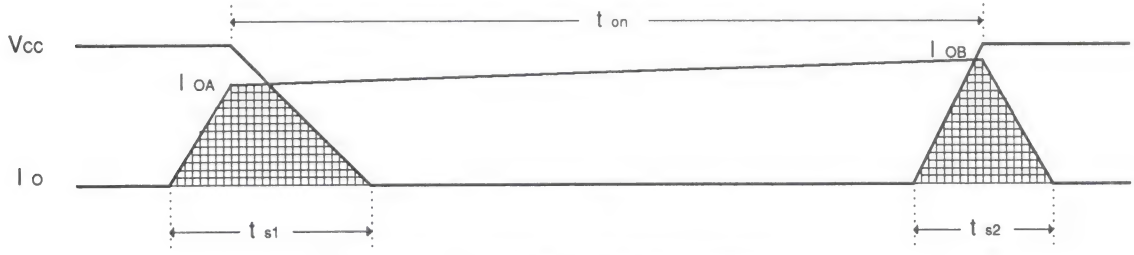

FIGURE 11. OUTPUT CHARACTERISTICS

GROUND CONNECTIONS

Layout & External Components

Important Information - The following layout guidelines and required external components are critical to the proper operation of these motor drives.

External connections can be easily made to the hybrid by any of the following methods:

- Solder a wire around each pin .
- Use pin extenders to raise the height of each pin so a printed circuit board can be mounted on top of the hybrid .
- Use a printed circuit board with a cutout that will enable the printed circuit board to slide over the pins.

Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper operation of the hybrid.

The V_b and logic grounds are on pins 19, 22, and 26 (GND). The V_{ss} connections for the output stage are on pins 1, 5, and 8 (V_{SS}). **To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 19,22,26) and V_{SS} (pins 1,5,8) must not exceed ±3V max, dc or peak.** This includes the combined voltage drop of the associated ground paths and the voltage drop across R_{sense} (see figure 12). For example, a value for R_{sense} of 0.025Ω will give a voltage drop of 1.25V at 50A and allow enough margin for the voltage drop in the ground conductors. Locate R_{sense} 1"-2" maximum from the hybrid. **It is critical that all ground connections be as short, and of lowest impedance, as the system allows.**

C1, C2, and C3 are 1µF, 10V ceramic capacitors that provide a low ac impedance between each V_{ss} pin and GND. You must use 1 capacitor for each Vss pin-to-GND connection (total of 3 capacitors in all), these capacitors are independent of the type of drive scheme used (i.e., Trapezoidal or Sinusoidal drive). Since placement of these capacitors is critical, place these capacitors across the hybrid, if possible. Please note, on figure 12, that C1, C2, and C3 must go directly from terminal-to-terminal on the hybrid — **do not daisy chain along the ground return.**

C4, C5, and C6 are the 0.1 µf ceramic bypass capacitors that suppress high frequency spiking. The voltage rating should be 2x the maximum system voltage. These capacitors should be located as close to the hybrid as possible.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive voltage spiking on the V_{cc} line. Accomplish this by placing a capacitor or clamping diode between V_{cc} and the high-power ground return.

C1,C2,C3 = 1uf, 10V CERAMIC CAPACITORS
C4,C5,C6 = 0.1uf, CERAMIC CAPACITORS
C7 = 0.01uf, 100V CERAMIC CAPACITORS
C8 = 0.01uf, 50V CERAMIC CAPACITORS

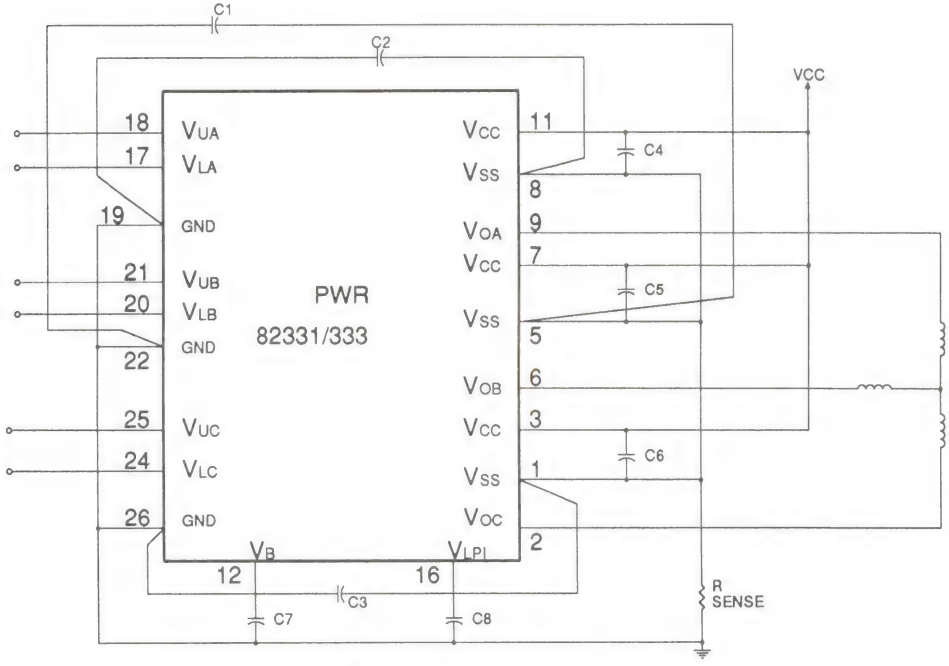

FIGURE 12. PWR-82331/333 GROUND CONNECTIONS

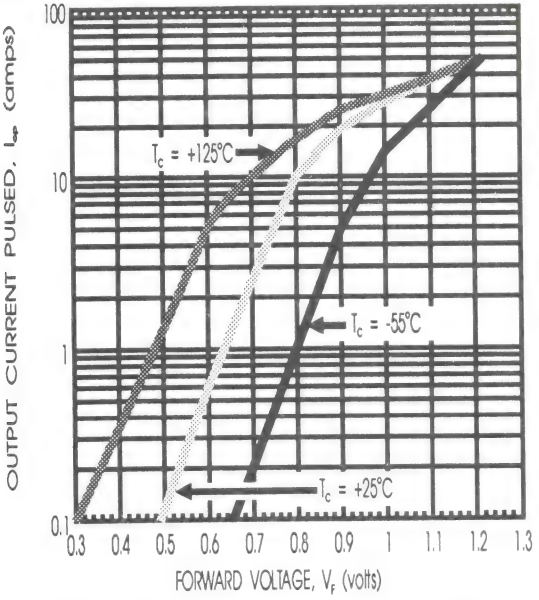

FIGURE 13A. PWR-82331 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES.

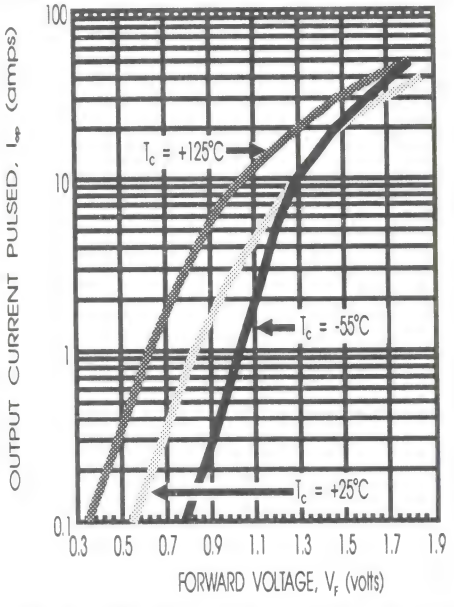

FIGURE 13B. PWR-82333 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES.

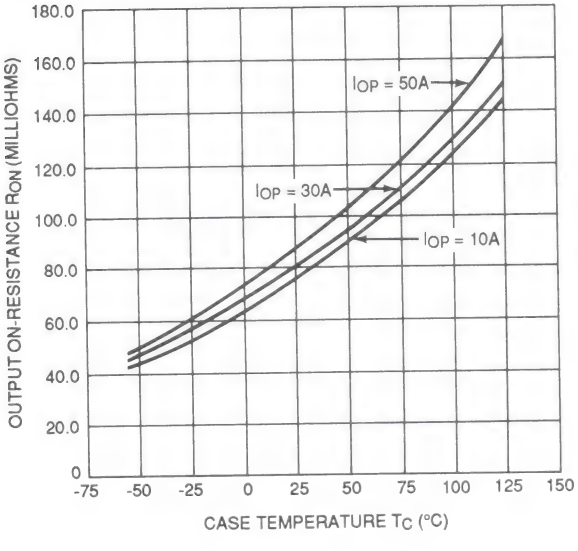

FIGURE 14A. PWR-82331 TYPICAL ON RESISTANCE VARIATION WITH TEMPERATURE.

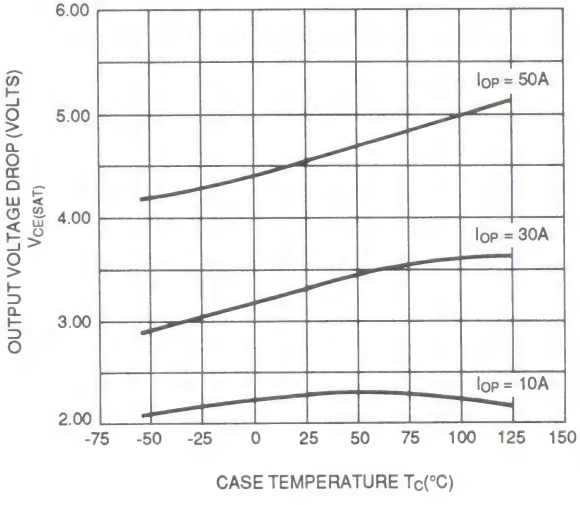

FIGURE 14B. PWR-82333 TYPICAL $V_{CE(SAT)}$ VARIATION WITH TEMPERATURE.

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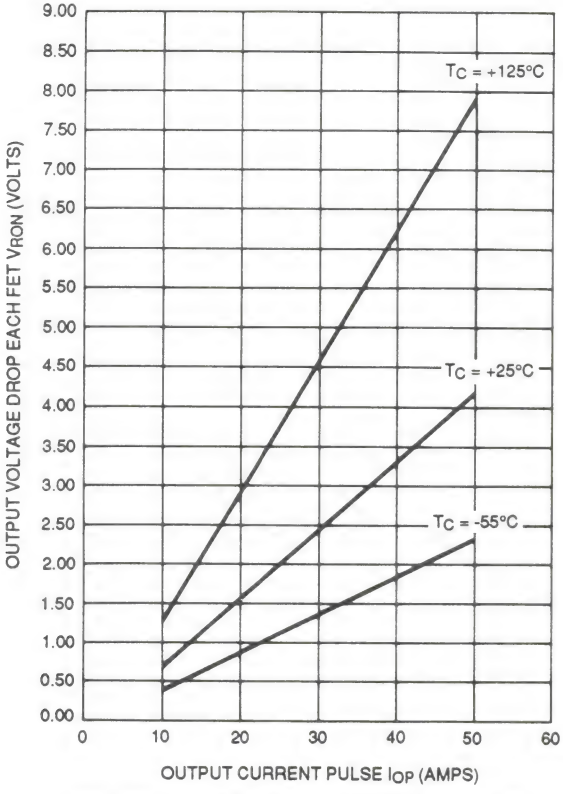

FIGURE 15A. PWR-82331 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT.

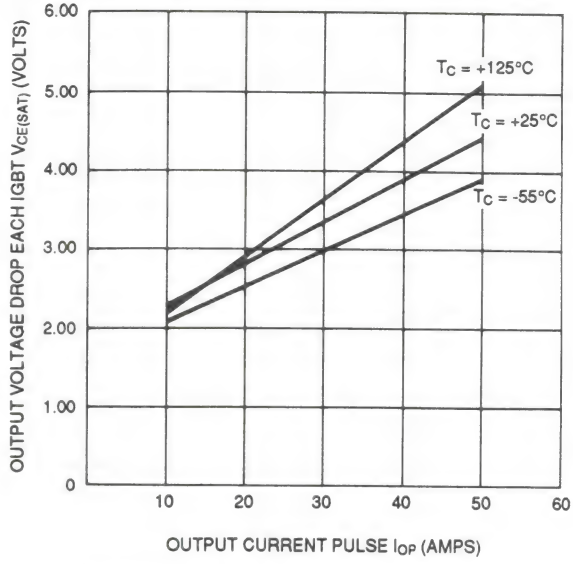

FIGURE 15B. PWR-82333 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT.

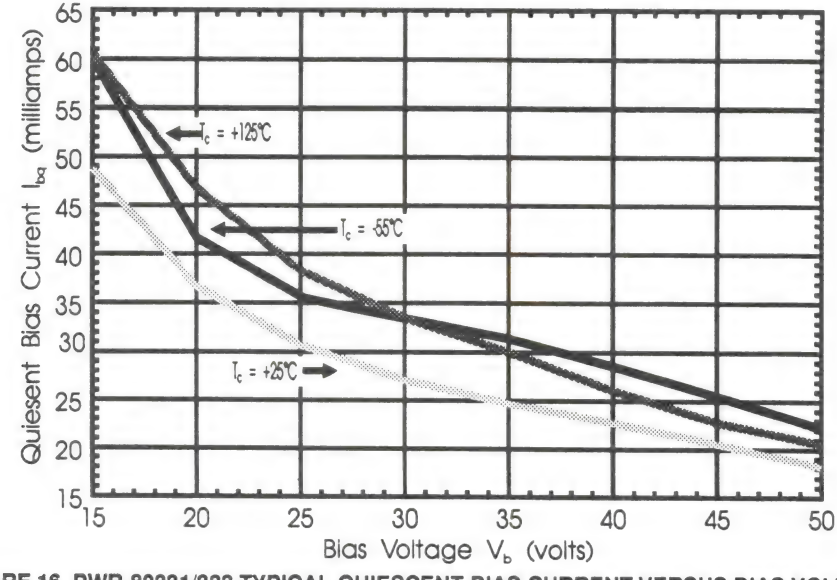

FIGURE 16. PWR-82331/333 TYPICAL QUIESCENT BIAS CURRENT VERSUS BIAS VOLTAGE

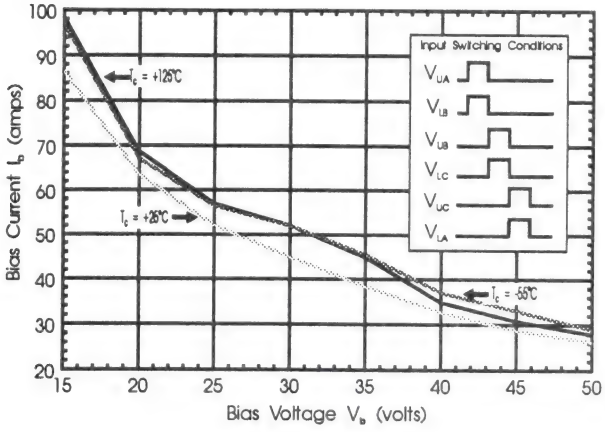

FIGURE 17A. PWR-82331TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE at f_o = 30kHz

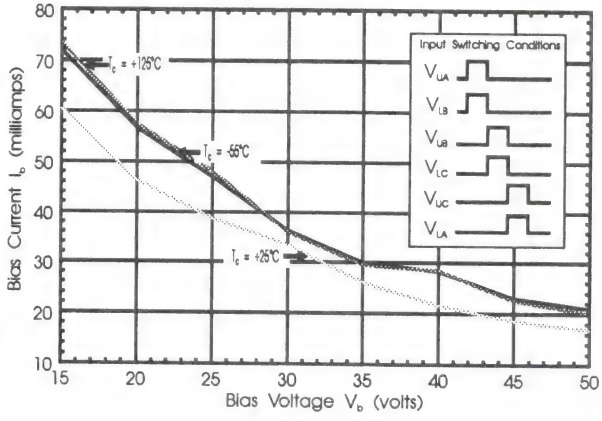

FIGURE 17B. PWR-82333 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE at f_o = 10kHz

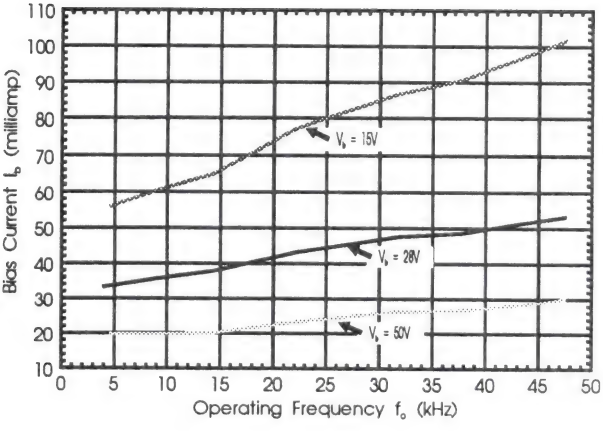

FIGURE 18A. PWR-82331 BIAS CURRENT VERSUS OPERATING FREQUENCY

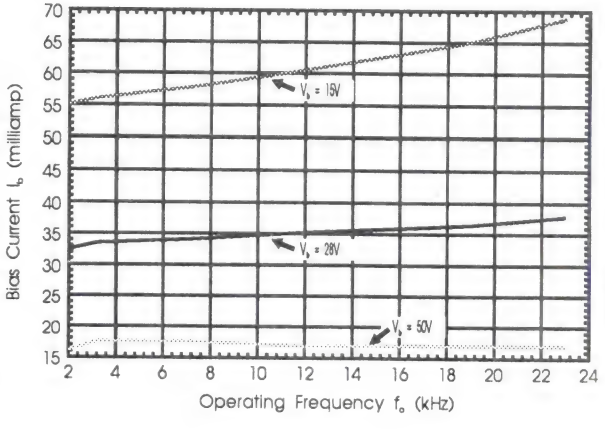

FIGURE 18B. PWR-82333 BIAS CURRENT VERSUS OPERATING FREQUENCY

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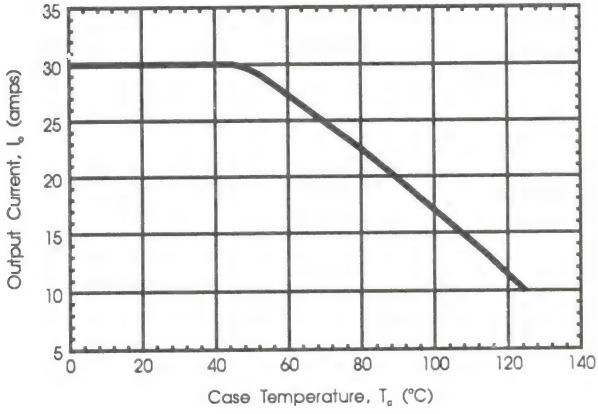

FIGURE 19A. PWR-82331
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE.

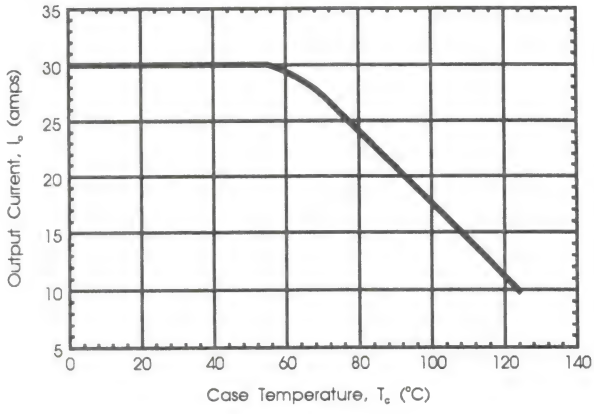

FIGURE 19B. PWR-82333
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE.

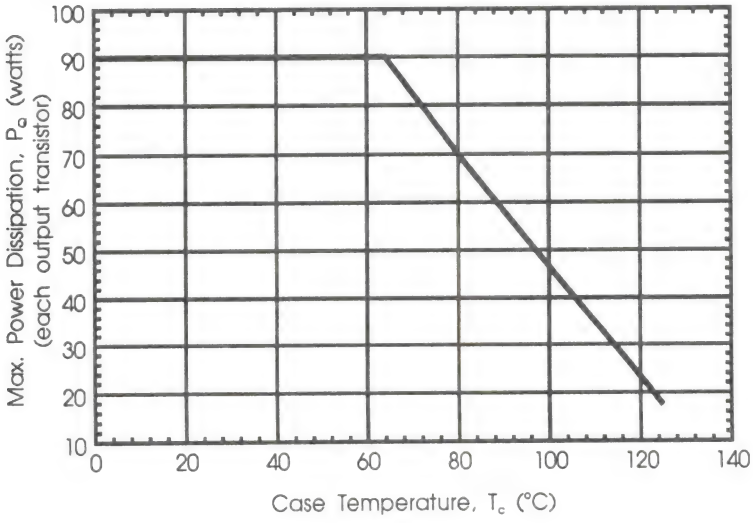

FIGURE 20. PWR-82331/333 MAXIMUM ALLOWABLE POWER DISSIPATION OF EACH OUTPUT TRANSISTOR VERSUS CASE TEMPERATURE.

Mounting

The package bolts to part of the chassis or even the motor assembly itself, depending on system requirements. In applications where this isn't convenient, the hybrid can be mounted to its own heatsink. The heat transfer in a hybrid is from semiconductor junction to the bottom of the hybrid case. The flatness and maximum temperature of this mounting surface are critical to proper performance and reliability, because this is the only method of dissipating the power created in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad. The heatsink should be designed to insure that the case temperature does not exceeded +125°C.

TABLE 3. INPUT-OUTPUT TRUTH TABLE

INPUTS							OUTPUTS		
UPPERS			LOWERS			CONTROL			
V_{UA}	V_{UB}	V_{UC}	V_{LA}	V_{LB}	V_{LC}	VSd	V_{OA}	V_{OB}	V_{OC}
0	0	1	0	1	0	0	Z	L	H
0	0	1	1	0	0	0	L	Z	H
0	0	1	1	1	0	0	L	L	H
0	1	0	0	0	1	0	Z	H	L
0	1	0	1	0	0	0	L	H	Z
0	1	0	1	0	1	0	L	H	L
0	1	1	1	0	0	0	L	H	H
0	1	1	1	0	1	0	L	H	Z
0	1	1	1	1	0	0	L	Z	H
1	0	0	0	0	1	0	H	Z	L
1	0	0	0	1	0	0	H	L	Z
1	0	0	0	1	1	0	H	L	L
1	0	1	0	1	0	0	H	L	H
1	0	1	0	1	1	0	H	L	Z
1	0	1	1	1	0	0	Z	L	H
1	1	0	0	0	1	0	H	H	L
1	1	0	0	1	1	0	H	Z	L
1	1	0	1	0	1	0	Z	H	L
0	0	0	0	0	0	0	Z	Z	Z
0	0	0	1	1	1	0	L	L	L
1	1	1	0	0	0	0	H	H	H
X	X	X	X	X	X	1	Z	Z	Z

H=high level, L=low level, X=irrelavant, Z=high impedance(off)

TABLE 4. PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{SS}	26	GND
2	V_{OC}	25	V_{UC}
3	V_{CC}	24	V_{LC}
4	N/C	23	V_{Sd}
5	V_{SS}	22	GND
6	V_{OB}	21	V_{UB}
7	V_{CC}	20	V_{LB}
8	V_{SS}	19	GND
9	V_{OA}	18	V_{UA}
10	N/C	17	V_{LA}
11	V_{CC}	16	V_{LPI}
12	V_b	15	V_{LPO}
13	V_Z	14	N/C

NOTE: Pins 3, 7, and 11 are internally connected; Pins 19, 22, and 26 are internally connected.

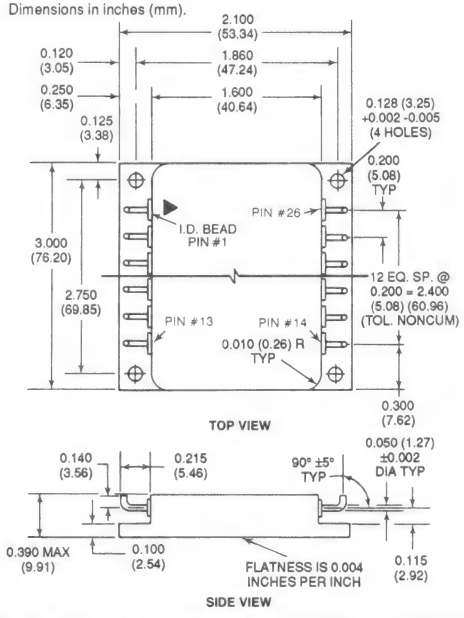

FIGURE 21. PWR-82331/333 MECHANICAL OUTLINE

ORDERING INFORMATION

PWR - 8233X - X X 0

Reliability Grade:
0 = Standard DDC Procedures.
1 = Military processing available.
2 = Military processing available but without QCI testing

Temperature Range:
1 = -55 to 125°C
3 = 0 to 70°C

Rating:
1 = 200V using MOSFETs
3 = 500V using IGBTs

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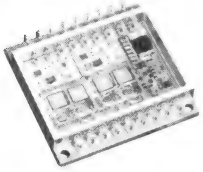
DDC
ILC DATA DEVICE CORPORATION

PWR-82340 and PWR-82342

SMART POWER H-BRIDGE MOTOR DRIVES



DESCRIPTION

The PWR-82340 and PWR-82342 are 30A H-bridge motor drive hybrids. The PWR-82340 has a 200V rating and uses MOSFETs in the output stage while the PWR-82342 has a 500V rating and an IGBT output stage. Both types have individual fast recovery diodes internally connected across the output drive transistors to clamp inductive flyback.

This new series of Smart Power Motor Drives has CMOS Schmitt Trigger inputs for high noise immunity. High- and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn on of in-line transistors, thus eliminating a shoot thru condition. The internal logic controls the high- and low-side gate drives for each phase and can operate from 5 to 15V logic levels.

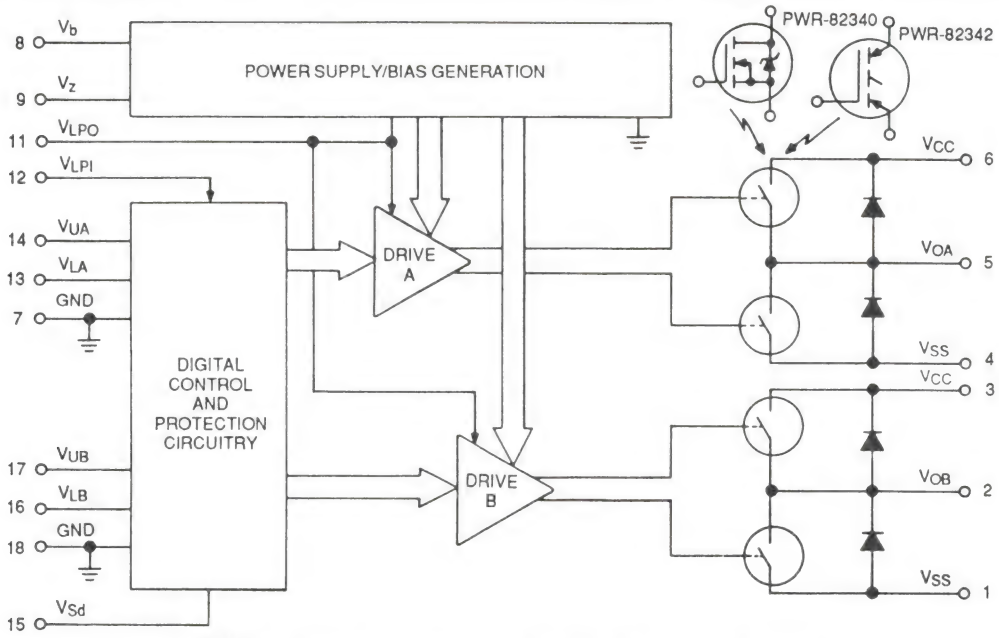
The internal power supply provides a constant voltage source to the floating high-side gate drives. This provides constant output performance for switching frequencies from dc to 50 kHz.

APPLICATIONS

Packaged in small cases, these hybrids are an excellent choice for high-performance, high-reliability motor drives for military and aerospace servo-amps and speed controls. Among the many applications are robotics; electro-mechanical valve assemblies; actuator systems for flight control surfaces on military and commercial aircraft; antenna and radar positioning; fan and blower motors for environmental conditioning; thrust and vector position control of mini-subs, drones, and RPV's; compressor motors for cryogenic coolers; and high-power inverters. The PWR-82340/342 hybrids are ideal for harsh military environments where shock, vibration, and temperature extremes are evident, such as missile applications where fin actuator systems control missile direction. The PWR-82340/342 operates over the -55°C to +125°C temperature range and is available with military processing.

FEATURES

- ***Small Size (2.25" x 2.1" x 0.39")***
- ***200V & 500V Capability***
- ***30A Current Capability***
- ***High-Efficiency MOSFET or IGBT Drive Stage***
- ***Direct Drive from PWM***
- ***Drives Brushless DC or Brush Motors***
- ***Four Quadrant Operation***
- ***0.85°C/W $\theta_{j\text{-}c}$ Max***
- ***Military Processing Available***



NOTE: Pins 3 and 6 are internally connected; Pins 7 and 18 are internally connected.

FIGURE 1. PWR-82340/342 BLOCK DIAGRAM

TABLE 1. ABSOLUTE MAXIMUM RATINGS

(T_C = +25°C unless otherwise specified)

PARAMETER	SYMBOL	PWR-82340 VALUE	PWR-82342 VALUE	UNITS
SUPPLY VOLTAGE	V_{CC}	200	500	V
BIAS VOLTAGE	V_b	50	50	V
LOGIC POWER-IN VOLTAGE	V_{LPI}	18	18	V
INPUT LOGIC VOLTAGE	V_U, V_L, V_{Sd}	V_{LPI}+ 0.5	V_{LPI}+ 0.5	V
OUTPUT CURRENT				
CONTINUOUS	I_o	30	30	A
PULSED	I_{op}	50	50	A
OPERATING FREQUENCY	f_o	50	25	kHz
CASE OPERATING TEMPERATURE	T_C	– 55 to +125	– 55 to +125	°C
CASE STORAGE TEMPERATURE RANGE	T_{CS}	– 55 to +150	– 55 to +150	°C

TABLE 2. PWR-82340 and PWR-82342 SPECIFICATIONS (T_C = +25°C unless otherwise specified)

			PWR-82340			PWR-82342			
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
OUTPUT									
Output Current Continuous (see figures 19 and 15)	I_o				30			30	A
Supply Voltage	V_{CC}	see note 1		140	200		270	500	V
Output On-Resistance (each FET)(see figure 14A)	R_{on}	I_o=30A			0.1				ohm
Output Voltage Drop (each IGBT)(see figures 14B)	$V_{CE(SAT)}$	I_o=30A						3.8	V
Instant. Forward Voltage (flyback diode)(see figure 13)	V_F	I_p=30A (see note 2)			1.15			1.70	V
Reverse Recovery Time (flyback diode)	t_{rr}	I_f=1A, I_r=1A			50			50	nsec
Reverse Leakage Current at T_C=25°C	I_r	see note 3			10			10	µA
Reverse Leakage Current at T_C=125°C	I_r	see note 3			1			1	mA
BIAS SUPPLY									
Input Bias Voltage (T_C = -55 to +125°C)	V_b		15		50	15		50	V
Quiescent Bias Current (see note 4)(see figure 16)	I_{bq}	V_b = 28V		27			27		mA
Bias Current (T_C = -55 to +125°C)(see figures 17 and 18)	I_b	V_b = 28V,(see note 5)	30		40	24		35	mA
In-rush Current (T_C = -55 to +125°C)	I_{ir}	V_b = 28V			1.4			1.4	A
Logic Power Input Current	I_{LPI}	see note 6			2			2	mA
INPUT SIGNALS (see figure 7)		Pin Connections							
Positive Trigger Threshold Voltage	V_P	pin 11 & 12 connected	6.8		10	6.8		10	V
Negative Trigger Threshold Voltage	V_N	pin 11 & 12 connected	4.0		7	4.0		7	V
Positive Trigger Threshold Voltage	V_P	see note 6	2.2		3	2.2		3	V
Negative Trigger Threshold Voltage	V_N	see note 6	0.9		2	0.9		2	V
SWITCHING CHARACTERISTICS		Test 1 Conditions							
(see figure 2)		pin 11 & 12 connected							
Upper Drive:		+15V logic							
Turn-on propagation delay	t_d (on)	I_o = 30A peak			440			410	nsec
Turn-off propagation delay	t_d (off)	PWR-82340 V_{CC}= 140V			620			460	nsec
Shut-down propagation delay	t_{Sd}	PWR-82342 V_{CC}= 270V			400			410	nsec
Turn-on Rise Time	t_r				125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec
LowerDrive:									
Turn-on propagation delay	t_d (on)				450			400	nsec
Turn-off propagation delay	t_d (off)				600			470	nsec
Shut-down propagation delay (see figure 9)	t_{Sd}				400			370	nsec
Turn-on Rise Time	t_r				125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec
SWITCHING CHARACTERISTICS		Test 2 Conditions							
(see figure 2)		see note 6							
Upper Drive:		+5V logic							
Turn-on propagation delay	t_d (on)	I_o = 30A peak			690			650	nsec
Turn-off propagation delay	t_d (off)	PWR-82340 V_{CC}= 140V			915			750	nsec
Shut-down propagation delay	t_{Sd}	PWR-82342 V_{CC}= 270V			700			450	nsec
Turn-on Rise Time	t_r				125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec

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TABLE 2. PWR-82340 and PWR-82342 SPECIFICATIONS (continued) (T_C = +25°C unless otherwise specified)

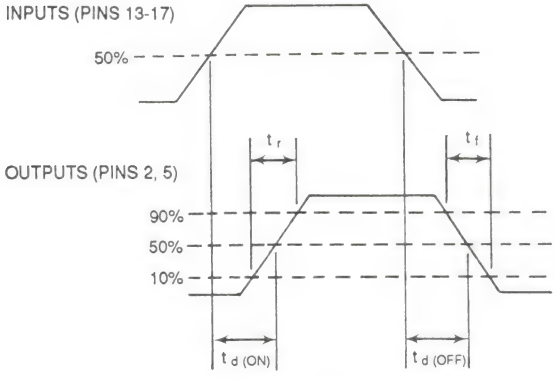
PARAMETERS	SYMBOL	TEST CONDITIONS	PWR-82340 MIN	PWR-82340 TYP	PWR-82340 MAX	PWR-82342 MIN	PWR-82342 TYP	PWR-82342 MAX	UNIT
SWITCHING CHARACTERISTICS (continued)		Test 2 Conditions							
LowerDrive:		see note 6							
Turn-on propagation delay	t_d (on)	+5V logic			725			650	nsec
Turn-off propagation delay	t_d (off)	I_o = 30A peak			890			750	nsec
Shut-down propagation delay (see figure 9)	t_{Sd}	PWR-82340 V_{CC}= 140V			700			450	nsec
Turn-on Rise Time	t_r	PWR-82342 V_{CC}= 270V			125			100	nsec
Turn-off Fall Time	t_f				125			150	nsec
DEAD TIME	t_{dt}		400			500			nsec
MINIMUM PULSE WIDTH	t_{pw}		150			175			nsec
THERMAL									
Maximum Thermal Resistance	θ_{j-c}	each transistor			0.85			0.85	°C/W
Maximum Lead Soldering Temp.	T_s	see note 7			250			250	°C
Junction Temperature Range	T_j		-55		150	-55		150	°C
Case Operating Temperature	T_{co}		-55		125	-55		125	°C
Case Storage Temperature	T_{cs}		-55		150	-55		150	°C
WEIGHT					3.88 (110)			3.88 (110)	oz (g)

NOTES:
1. For Hi-Rel applications, derating per MIL-S-19500 should be observed. (Derate V_{CC} by 70%.)
2. Pulse width ≤ 300 µs, duty cycle ≤ 2%.
3. For PWR-82340 V_{CC}=140V, V_U,V_L= logic '0' and for PWR-82342 V_{CC}=350V, V_U,V_L= logic '0'.
4. V_U, V_L = logic '0' on pins 13 to 17.
5. For PWR-82340 f_o = 30kHz and for PWR-82342 f_o = 10kHz.
6. Pin 12 connected to external +5V supply.
7. Solder 1/8" from case for 5 seconds maximum.

TECHNICAL INFORMATION

Introduction

The PWR-82340 & PWR-82342 are 30A motor drive hybrids rated at 200V and 500V respectively. The PWR-82340 uses a MOSFET output stage and the PWR-82342 has an IGBT output stage for high-speed, high-current, and high-efficiency operation. The PWR-82342 also offers high-voltage performance of an IGBT for use in 270V systems. These motor drives are ideal for use in high-performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, Multi-axis systems requiring multiple drive stages can benefit from the small size of these power drives.



(REFERENCE TABLE 2 ALSO.)

FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS.

The PWR-82340/342 can be driven directly from a PWM, DSP, or a custom ASIC that supplies digital signals to control the upper and lower transistors of each phase. These highly integrated drive stages have Schmitt trigger digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition, by preventing simultaneous turn-on of both the upper and lower transistors. The logic controls the high- and low-side gate drivers. Operation from 5 to 15V logic levels can be programmed by applying the appropriate voltage to pin 12 (V_{LPI}). The PWR-82340/342 has a ground referenced low-side gate drive. An internal dc-dc converter supplies a floating output to each of the 2 high-side drives. This provides a continious high-side gate drive even during a motor stall. Pin 11 (V_{LPO}) supplies a 15V output, which can be used to power the internal logic when system useage requires 15V logic. The high- and low-side gate drivers control the N-channel MOSFET or IGBT output stage. The MOSFETs used in the PWR-82340 allow output switching up to 50kHz, while the high-speed IGBTs in the PWR-82342 can switch at 25kHz. A flyback diode parallels each output transistor and controls the regenerative energy produced by the motor. These fast recovery diodes have faster reverse switching times than the intrinsic body diode of the MOSFETs used in the PWR-82340. They also protect the IGBTs used in the PWR-82342 from exceeding their Emitter-to-Collector breakdown voltage. Use of a copper case and solder attachment of the output transistors achieves a low thermal resistance of 0.85°C/W maximum. Care should be taken to adequately heatsink these motor drives to maintain a case temperature of 125°C. Junction temperatures should not exceed 150°C. The PWR-82340/342 do not have internal short-circuit or overcurrent protection, which if required, must be added externally to the hybrid.

Bias Voltages

The PWR-82340/342 motor drive hybrids require only a single power supply for operation. The hybrid generates two independent, floating supplies, which eliminates the need for external bias voltages for each phase.

In order for the internal power supply to generate these voltages, the input bias voltage (V_b) must be from 15 to 50 Vdc. In most avionic systems this can be accomplished by connecting the V_b pin to the MIL-STD-704D, 28 Volt bus. See figure 3a.

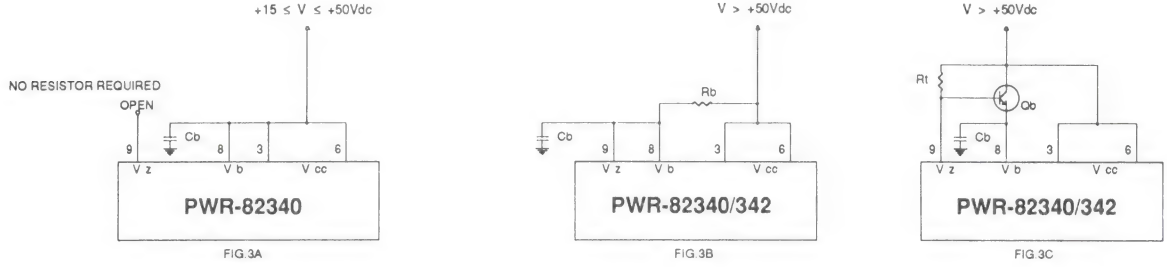
If the system bus voltage is greater than 50 Vdc (and a lower voltage is not available), then the V_b pin and V_z pin can be tied together with an external power resistor (R_b) and connected from these pins to the system power bus. See figure 3b.

See figures 4 and 5 for bias resistor characteristics.

If additional power dissipation in R_b is a concern, figure 3c shows a more efficient design, using a low-power resistor (R_T) and an additional transistor. To determine the proper resistor to use, refer to figure 6.

If there is another voltage available in the system in the 15 to 50 Vdc range, then this voltage can be directly connected to the V_b pin of the hybrid.

In any case, a 0.01 µf decoupling capacitor (C_b) must be connected between V_b (pin 8) and GND.



NOTE: Cb = 0.01uf, 100V, CERAMIC ; Qb = 200V, 6W TRANSISTOR FOR PWR-82340 ; Qb = 500V, 12W TRANSISTOR FOR PWR-82342

FIGURE 3. CONNECTION TO BUS VOLTAGE TO DEVELOP PROPER INPUT BIAS VOLTAGE.

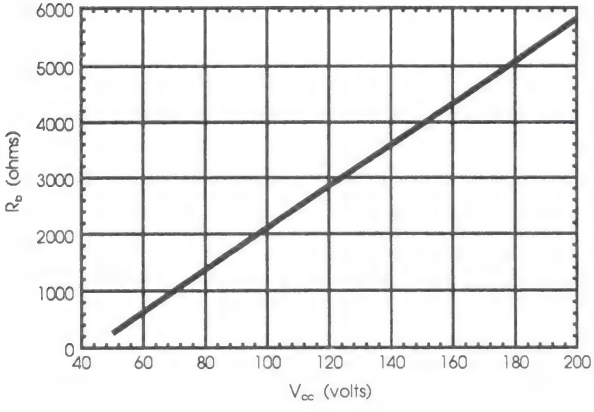


Figure 4a. PWR-82340

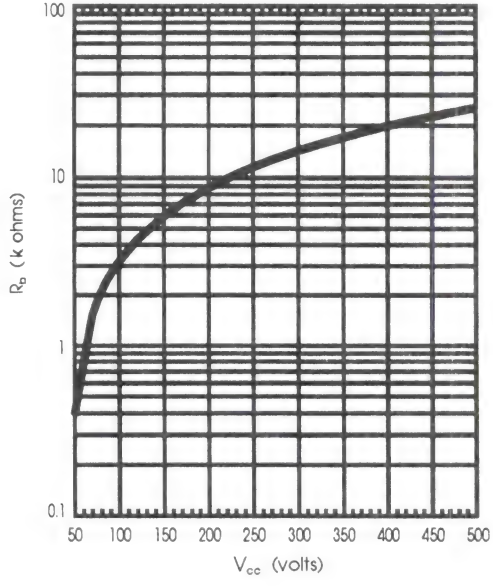


Figure 4b. PWR-82342

FIGURE 4. BIAS RESISTOR VALUE VS. BUS VOLTAGE

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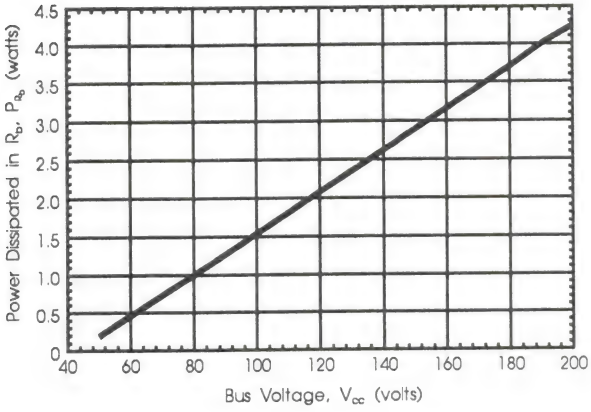


Figure 5a. PWR-82340

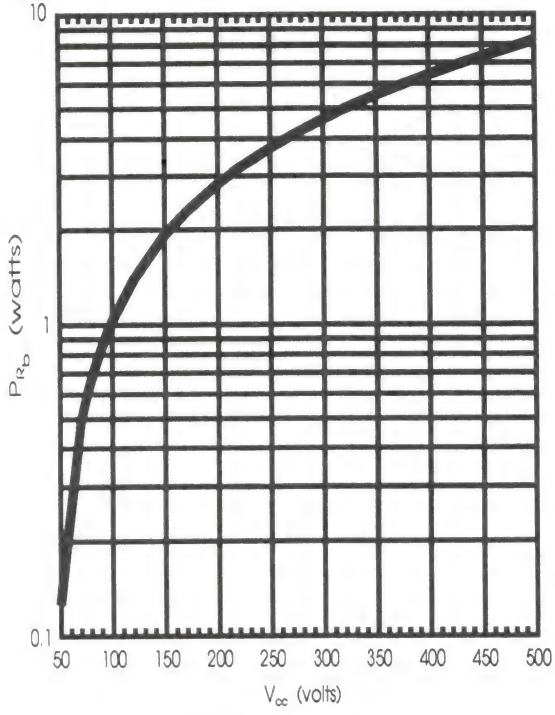


Figure 5b. PWR-82342

FIGURE 5. POWER DISSIPATED IN BIAS RESISTOR (R_b) VS. BUS VOLTAGE

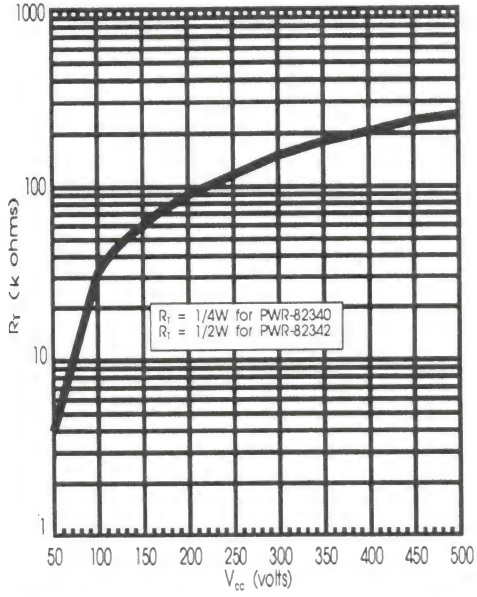


FIGURE 6. R_T RESISTOR VALUE VS. BUS VOLTAGE

Digitally Controlled Inputs

The PWR-82340/342 uses Schmitt triggered digital inputs (with hysteresis) to ensure high-noise immunity. The trigger switches at different points for positive and negative going signals. Hysteresis voltage (V_H) is the difference between the positive going voltage (V_P) and the negative going voltage (V_N) (see figure 7). The digital inputs have programmable logic levels, which allows the hybrid to be used with different types of control logic with an input voltage range of 5-15V, such as TTL or CMOS logic. The PWR-82340/342 internal power supply generates a 15Vdc (V_{LPO}) on pin 11. This output can only be used to power the internal digital circuitry within the hybrid. **Do not use this 15V output to power any circuitry external to the hybrid.** Pin 12 is the logic power input (V_{LPI}) for the digital circuitry inside the hybrid. **A 0.01uF, 50V ceramic capacitor must be placed between this pin (12) and GND as close to the hybrid as possible.** When using 15V control circuitry, the logic power input (pin 12) can be connected directly to the logic power output (pin 11) of the hybrid. There is no need for an additional external power supply. **When using 5V control logic, an external 5Vdc supply must be connected between pin 12 of the hybrid, and GND — leave Pin 11 open (N/C).** The control circuitry can be as simple as a PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. The Block Diagram in figure 8 shows a typical interface of the PWR-82340/342 with a motor and control logic in a Servo-Amp System.

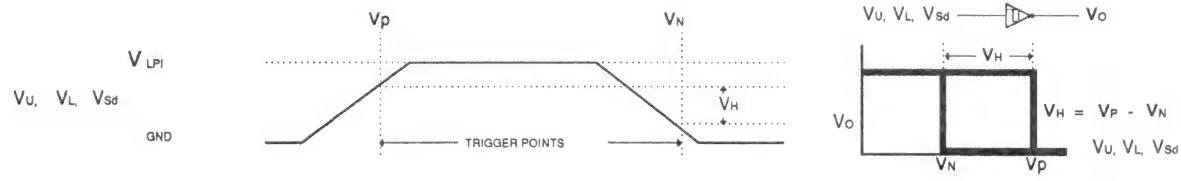
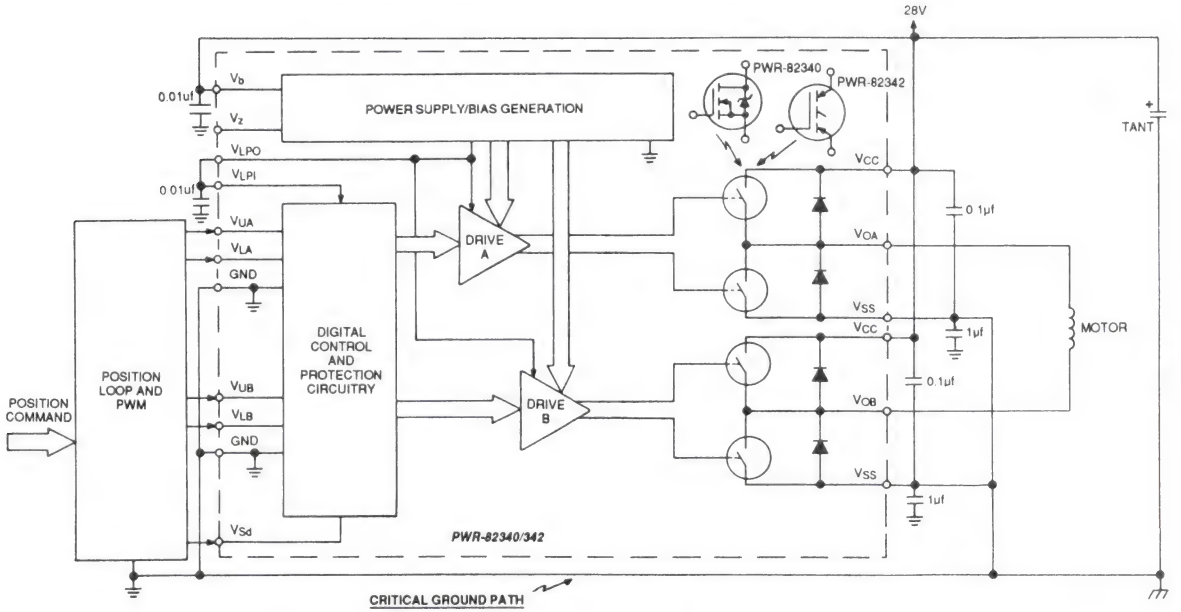


FIGURE 7. HYSTERESIS DEFINITION AND CHARACTERISTICS



To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 7, 18) and V_{SS} (pins 1, 4) must not exceed ±3V max, dc or peak.

FIGURE 8. PWR-82340/342 TYPICAL INTERFACE WITH A MOTOR AND PWM.

Shut-Down Input (V_{Sd})

Pin 15(V_{Sd}) provides a digital shut-down input, which allows the user to completely turn off both the upper- and lower-output transistors in both phases. Application of a logic '1' to the V_{Sd} input will latch the Digital Control/Protection circuitry thereby turning off all output transistors. The Digital Control/Protection circuitry remains latched in the off state and will not respond to signals on the V_L or V_U inputs while the V_{Sd} has a logic '1' applied. When the user or the sense circuitry (as in figure 10) returns the V_{Sd} input to a logic '0', and then the user sets the V_L and V_U inputs to a logic '0' the output of the Digital Control/Protection circuitry will clear the internal latch. When the next rising edge (see figure 9) occurs on the V_L or V_U digital inputs, the output transistors will respond to the corresponding digital input. This feature can be used with external current limit or temperature sense circuitry to disable the drive if a fault condition occurs(see figure 10).

Internal Protection Circuitry

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. The circuitry allows only proper input signal patterns to cause output conduction. Figure 9 and Table 3 show these timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR-82340/342. **A dead time of 500nsec minimum should still be maintained** between the signals at the V_U and V_L pins; this ensures the complete turn off of any transistor before turning on its associated in-line transistor.

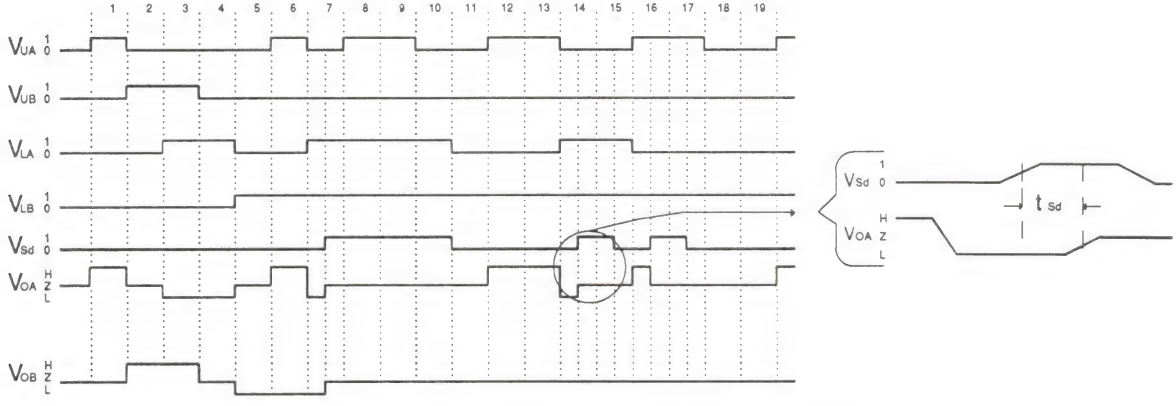


FIGURE 9. SHUT-DOWN (V_{Sd}) TIMING RELATIONSHIPS.

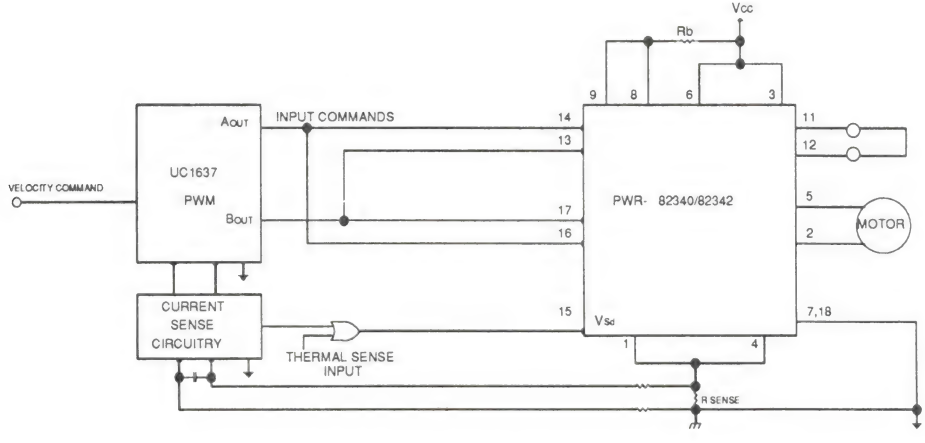


FIGURE 10. FUNCTIONAL SHUT-DOWN INPUT USED WITH CURRENT-SENSING CIRCUITRY.

PWR-82340 Power Dissipation (see figure 11)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

V_{CC} = 140V(Bus Voltage)
I_{OA} = 20A (see figure 11) ; I_{OB} = 30A; (see figure 11)
t_{on} = 20µs (see figure 11); T = 40µs (period)
R_{on} = 0.1 Ω (on-resistance see Table 2, I_o = 30A, T_c = 25°C)
t_{s1} = 250ns (see figure 11); t_{s2} = 250ns (see figure 11)
f_o = 25kHz(switching frequency)
V_f is the diode forward voltage, Table 2. I_o = 30A,T_c = 25°C
V_f(avg) = 1.15V
I_f is the diode forward current

1. Conduction Losses (P_C)

P_C = (I motor rms)^2 x R_{on}

$$\text{I motor rms} = \sqrt{\left(I_{OB}{}^2 - I_{OB}\,(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^2}{3} \right)\left(\frac{t_{on}}{T}\right)}$$

$$\text{I motor rms} = \sqrt{\left(30^2 - 30\,(30 - 20) + \frac{(30 - 20)^2}{3} \right)\left(\frac{20}{40}\right)}$$

$P_C = (17.80A)^2$ x (0.1 Ω)
P_C = 31.68 Watts

2. Switching Losses (P_S)

$P_S = [V_{CC}(I_{OA}(t_{s1}) + I_{OB}(t_{s2}))f_o]/2$
$P_S = [140(20\ (250ns) + 30(250ns))25k]/2$
P_S = 21.88 Watts

3. Flyback diode loses (P_{df})

$P_{df} = I_f$ (avg) x V_f (avg)
I_f (avg) = $[(I_{OB} + I_{OA})/2]/2$ = $[(30 + 20)/2]/2$ = 12.5A
P_{df} = 12.5A x 1.15V
P_{df} = 14.38 Watts

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference figure 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

To calculate Total Power dissipated in the hybrid use:

$$P_{Total} = \sum_{i=1}^{4} [P_{ci} + P_{si} + P_{dfi}]$$ where i = each transistor or diode.

PWR-82342 Power Dissipation (see figure 11)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

V_{CC} = 270V(Bus Voltage)
I_{OA} = 20A (see figure 11) ; I_{OB} = 30A; (see figure 11)
t_{on} = 50µs (see figure 11); T = 100µs (period)
$V_{CE(SAT)}$ = 3.8 V (see Table 2, I_o = 30A, T_c = 25°C)
t_{s1} = 300ns (see figure 11); t_{s2} = 300ns (see figure 11)
f_o = 10kHz(switching frequency)
V_f is the diode forward voltage, Table 2, I_o = 30A,T_c = 25°C
V_f(avg) = 1.70V
I_f is the diode forward current

1. Conduction Losses (P_C)

P_C = (I motor rms) x $V_{CE(SAT)}$

$$\text{I motor rms} = \sqrt{\left(I_{OB}{}^2 - I_{OB}\,(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^2}{3} \right)\left(\frac{t_{on}}{T}\right)}$$

$$\text{I motor rms} = \sqrt{\left(30^2 - 30\,(30 - 20) + \frac{(30 - 20)^2}{3} \right)\left(\frac{50}{100}\right)}$$

P_C = (17.80A) x (3.8V)
P_C = 67.64 Watts

2. Switching Losses (P_S)

$P_S = [V_{CC}(I_{OA}(t_{s1}) + I_{OB}(t_{s2}))f_o]/2$
$P_S = [270(20\ (300ns) + 30(300ns))10k]/2$
P_S = 20.25 Watts

3. Flyback diode loses (P_{df})

$P_{df} = I_f$ (avg) x V_f (avg)
I_f (avg) = $[(I_{OB} + I_{OA})/2]/2$ = $[(30 + 20)/2]/2$ = 12.5A
P_{df} = 12.5A x 1.70V
P_{df} = 21.25 Watts

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference figure 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

To calculate Total Power dissipated in the hybrid use:

$$P_{Total} = \sum_{i=1}^{4} [P_{ci} + P_{si} + P_{dfi}]$$ where i = each transistor or diode.

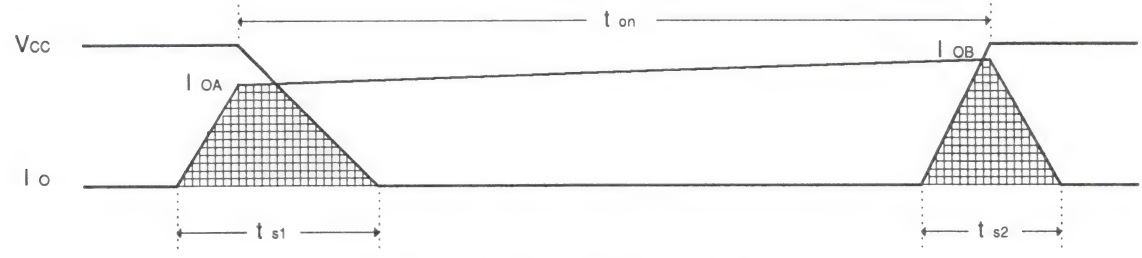


FIGURE 11. OUTPUT CHARACTERISTICS

GROUND CONNECTIONS

Layout & External Components

Important Information - The following layout guidelines and required external components are critical to the proper operation of these motor drives.

External connections can be easily made to the hybrid by any of the following methods:

- Solder a wire around each pin .
- Use pin extenders to raise the height of each pin so a printed circuit board can be mounted on top of the hybrid .
- Use a printed circuit board with a cutout that will enable the printed circuit board to slide over the pins.

Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper operation of the hybrid.

The V_b and logic grounds are on pins 7 and 18 (GND). The V_{ss} connections for the output stage are on pins 1 and 4 (V_{SS}). **To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 7,18) and V_{SS} (pins 1,4) must not exceed ±3V max, dc or peak.** This includes the combined voltage drop of the associated ground paths and the voltage drop across R_{sense} (see figure 12). For example, a value for R_{sense} of 0.025Ω will give a voltage drop of 1.25V at 50A and allow enough margin for the voltage drop in the ground conductors. Locate R_{sense} 1"-2" maximum from the hybrid. **It is critical that all ground connections be as short, and of lowest impedance, as the system allows.**

C1 and C2 are 1µF, 10V ceramic capacitors that provide a low ac impedance between each V_{ss} pin and GND. You must use 1 capacitor for each Vss pin-to-GND connection (total of 2 capacitors in all), these capacitors are independent of the type of drive scheme used. Since placement of these capacitors is critical, place these capacitors across the hybrid, if possible. Please note, on figure 12, that C1 and C2 must go directly from terminal-to-terminal on the hybrid — **do not daisy chain along the ground return.**

C3 and C4 are the 0.1 µf ceramic bypass capacitors that suppress high frequency spiking. The voltage rating should be 2x the maximum system voltage. These capacitors should be located as close to the hybrid as possible.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive voltage spiking on the V_{cc} line. Accomplish this by placing a capacitor or clamping diode between V_{cc} and the high-power ground return.

C1,C2 = 1.00uf, 10V CERAMIC CAPACITORS
C3,C4 = 0.10uf, CERAMIC CAPACITORS
C5 = 0.01uf, 100V CERAMIC CAPACITOR
C6 = 0.01uf, 50V CERAMIC CAPACITOR

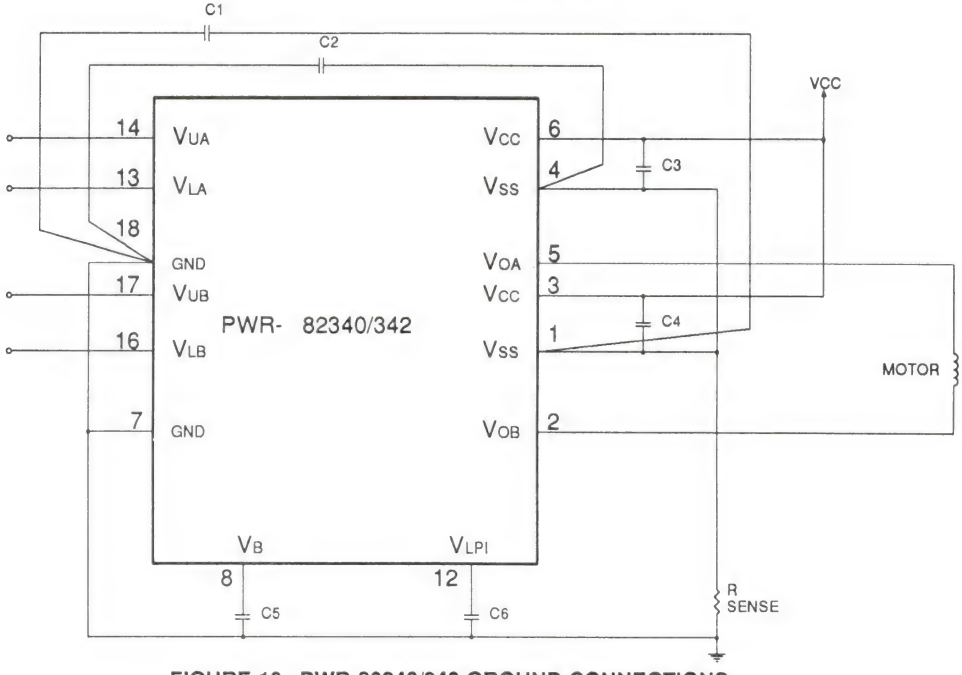


FIGURE 12. PWR-82340/342 GROUND CONNECTIONS

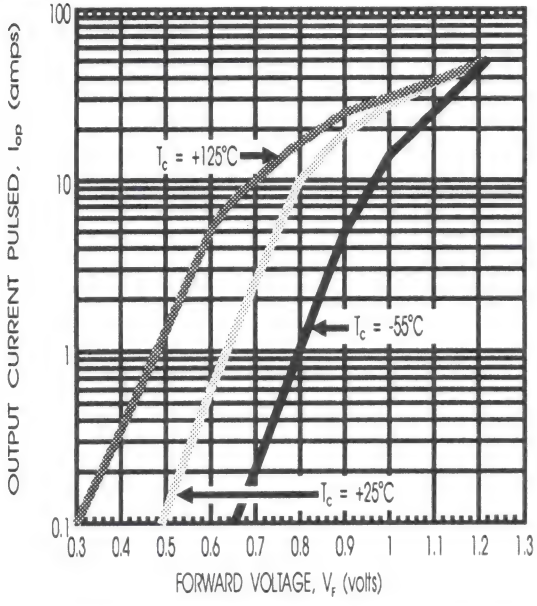


FIGURE 13A. PWR-82340 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES.

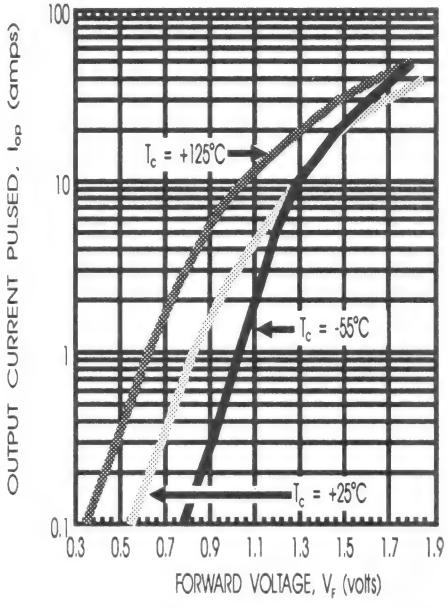


FIGURE 13B. PWR-82342 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES.

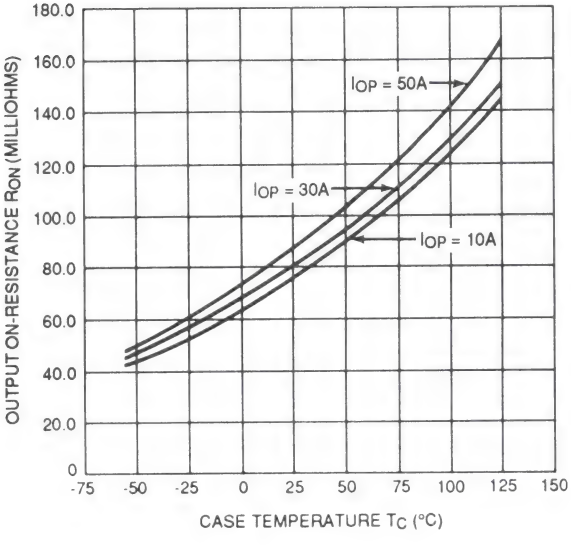


FIGURE 14A. PWR-82340 TYPICAL ON RESISTANCE VARIATION WITH TEMPERATURE.

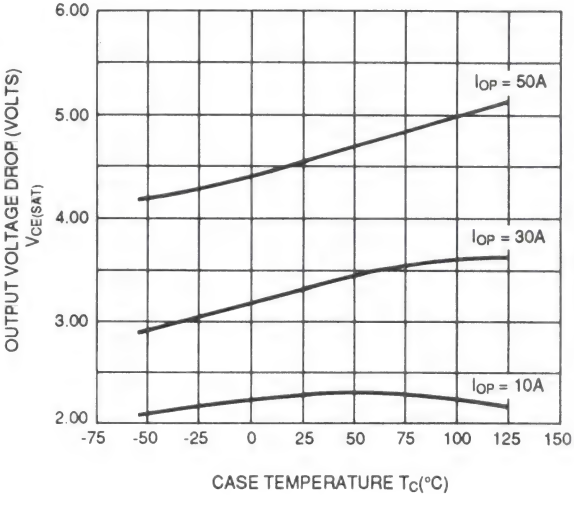


FIGURE 14B. PWR-82342 TYPICAL $V_{CE(SAT)}$ VARIATION WITH TEMPERATURE.

K

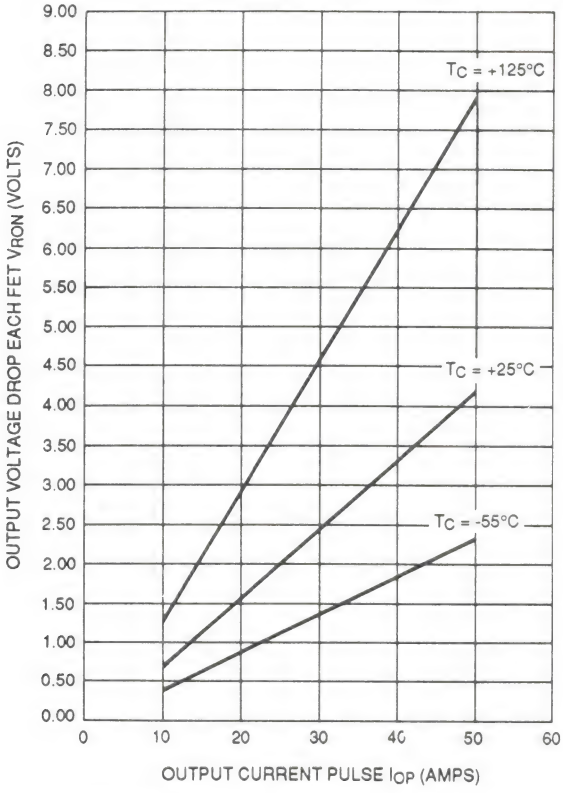


FIGURE 15A. PWR-82340 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT.

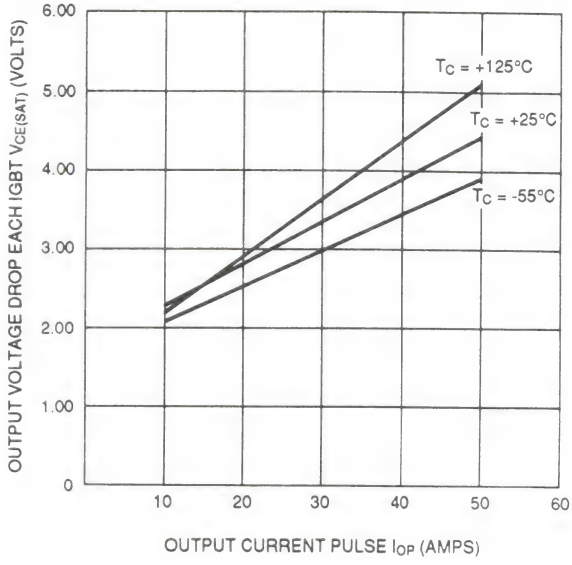


FIGURE 15B. PWR-82342 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT.

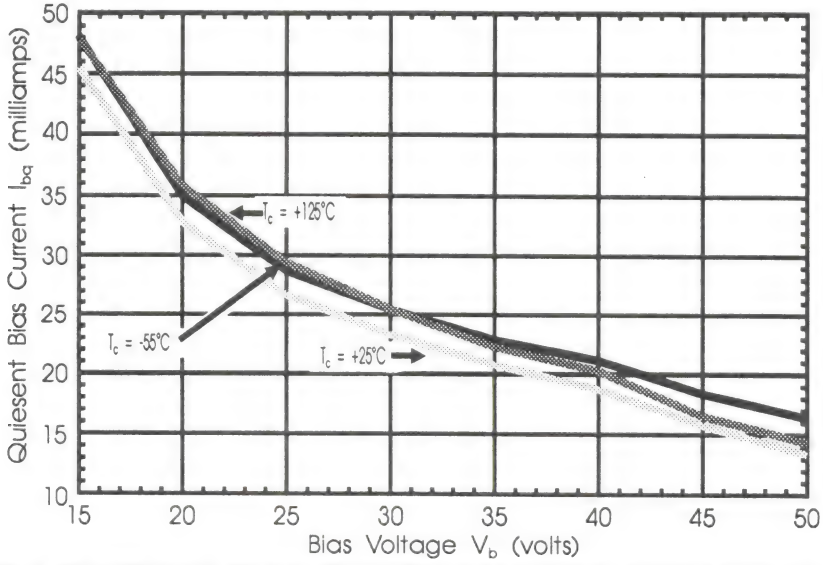


FIGURE 16. PWR-82340/342 TYPICAL QUIESCENT BIAS CURRENT VERSUS BIAS VOLTAGE

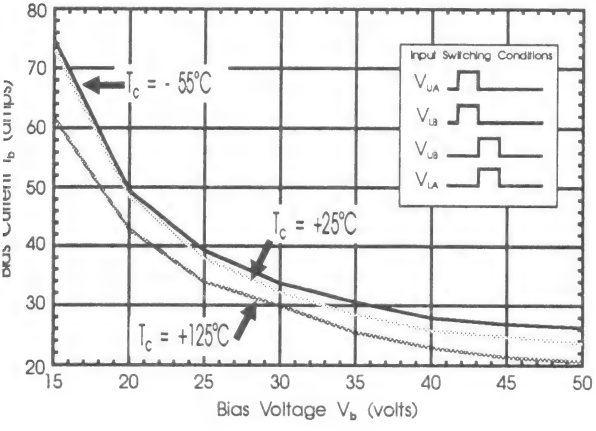


FIGURE 17A. PWR-82340 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE at f_o = 30kHz

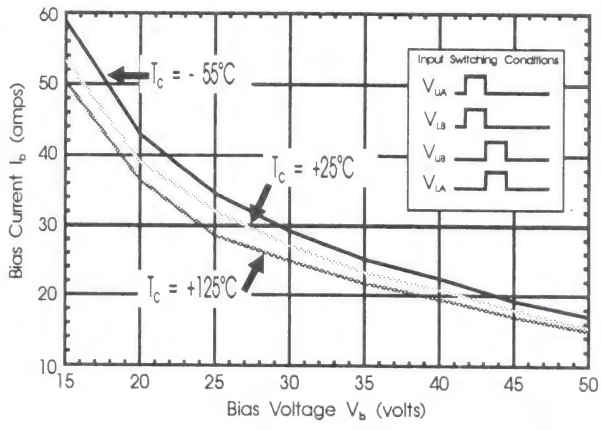


FIGURE 17B. PWR-82342 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE at f_o = 10kHz

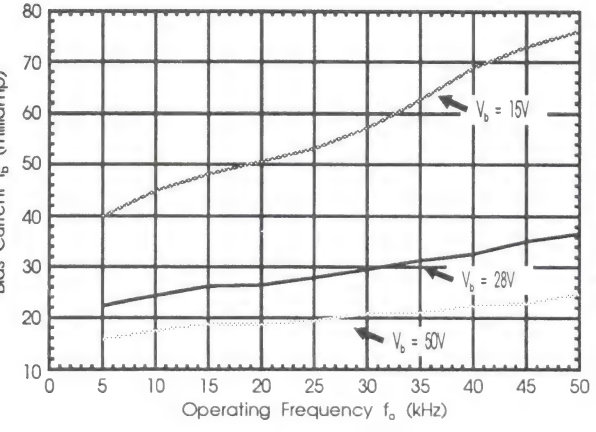


FIGURE 18A. PWR-82340 BIAS CURRENT VERSUS OPERATING FREQUENCY

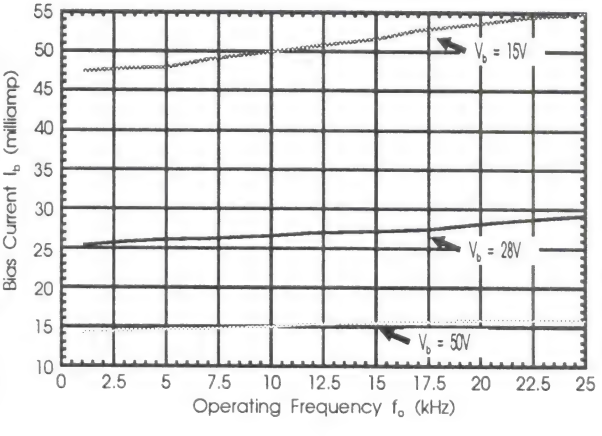


FIGURE 18B. PWR-82342 BIAS CURRENT VERSUS OPERATING FREQUENCY

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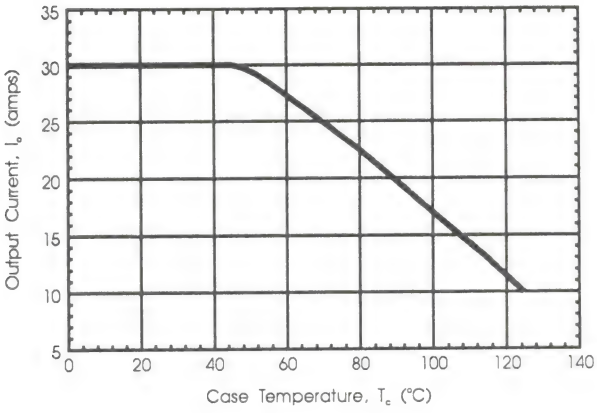

FIGURE 19A. PWR-82340
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE.

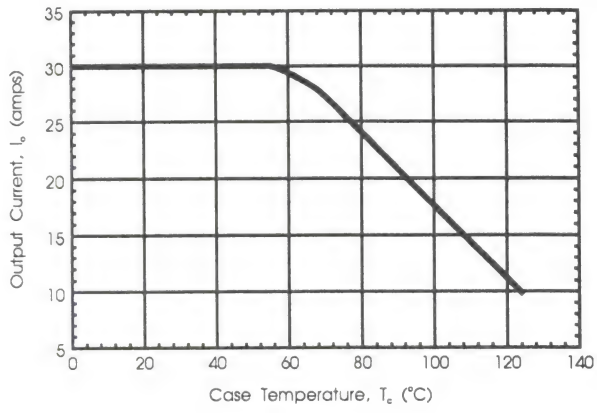

FIGURE 19B. PWR-82342
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE.

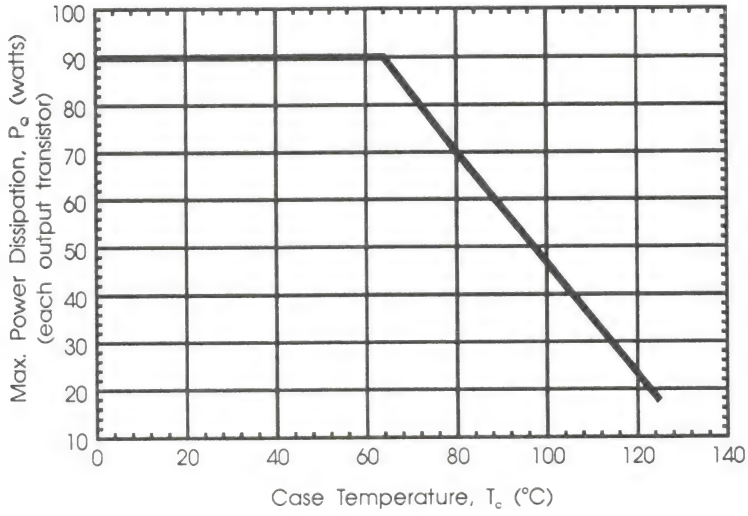

FIGURE 20. PWR-82340/342 MAXIMUM ALLOWABLE POWER DISSIPATION OF EACH OUTPUT TRANSISTOR VERSUS CASE TEMPERATURE.

Mounting

The package bolts to part of the chassis or even the motor assembly itself, depending on system requirements. In applications where this isn't convenient, the hybrid can be mounted to its own heatsink. The heat transfer in a hybrid is from semiconductor junction to the bottom of the hybrid case. The flatness and maximum temperature of this mounting surface are critical to proper performance and reliability, because this is the only method of dissipating the power created in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad. The heatsink should be designed to insure that the case temperature does not exceeded +125°C.

TABLE 3. INPUT-OUTPUT TRUTH TABLE

INPUTS					OUTPUTS	
UPPERS		LOWERS		CONTROL		
V_{UA}	V_{UB}	V_{LA}	V_{LB}	VSd	V_{OA}	V_{OB}
0	0	1	1	0	L	L
0	1	1	0	0	L	H
1	0	0	1	0	H	L
1	1	0	0	0	H	H
1	X	1	X	0	Z	X
X	1	X	1	0	X	Z
0	0	0	0	0	Z	Z
X	X	X	X	1	Z	Z

H=high level, L=low level, X=irrelavant, Z=high impedance(off)

TABLE 4. PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{SS}	18	GND
2	V_{OB}	17	V_{UB}
3	V_{CC}	16	V_{LB}
4	V_{SS}	15	V_{Sd}
5	V_{OA}	14	V_{UA}
6	V_{CC}	13	V_{LA}
7	GND	12	V_{LPI}
8	V_b	11	V_{LPO}
9	V_Z	10	N/C

NOTE: Pins 3 and 6 are internally connected; Pins 7 and 18 are internally connected.

Dimensions in inches (mm).

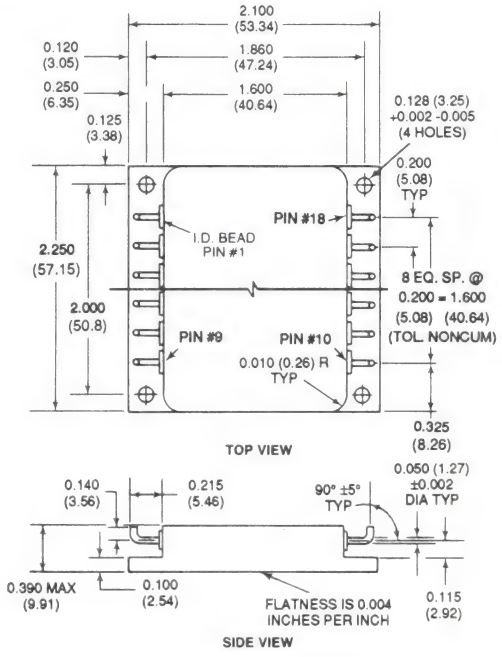

FIGURE 21. PWR-82340/342 MECHANICAL OUTLINE

ORDERING INFORMATION

PWR - 8234X - X X 0

Reliability Grade:
0 = Standard DDC Procedures.
1 = Military processing available.
2 = Military processing available but without QCI testing

Temperature Range:
1 = -55 to 125°C
3 = 0 to 70°C

Rating:
0 = 200V using MOSFETs
2 = 500V using IGBTs

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SECTION L
DC - DC CONVERTERS

PRODUCT SUMMARY TABLE

MODEL	PACKAGE	DESCRIPTION/FEATURES	PAGE
EMI-82470	2.1 x 1.12 x 0.495 5 pin plug-in	MIL-STD-461 EMI filter.	L-2
PWR-82400 /2 SERIES	3.2 x 2.45 x 0.55" 10 pin plug-in with mounting flange	±15V & +5V, ±12V & +5V 60W dc - dc converters. Features include high power density and 80% min operating efficency. Operation over a wide operating temperature range and hermetically sealed.	L-4
PWR-82401/3 SERIES	3.2 x 2.45 x 0.55" 10 pin plug-in with mounting flange	±15V & +5V, ±12V & +5V 60W dc - dc converters. Features include high power density and 80% min operating efficency. Operation over a wide operating temperature range and hermetically sealed.	L-8

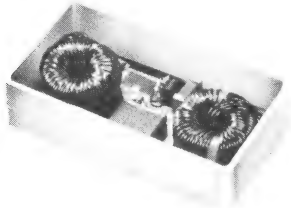
NOTES: Most hybrid products are available with Military Processing (Contact Factory).

* New Product

DDC
ILC DATA DEVICE CORPORATION

EMI-82470

EMI FILTER WITH TRANSIENT SUPPRESSOR



PRELIMINARY

Call for updated data sheet.

DESCRIPTION

The EMI-82470 is designed to reduce the input line reflected ripple current of DDC's PWR-82400 Series, as well as other manufacturers of switch mode dc-dc converters.

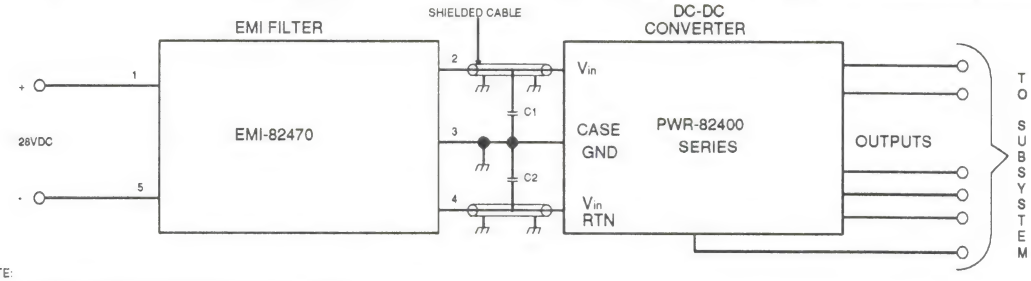
Operating over the full military temperature range, these filters are intended for applications where MIL-STD-461B levels of conducted and radiated noise must be met.

When connected as shown in figure 1, the PWR-82400 Series dc-dc converters and filters will meet the EMI requirements of **MIL-STD-461B, CE01, CE03, CS01, CS06, RE02, RS06**. The input voltage requirements of **MIL-STD-704 B, C, D, E** will also be met with this configuration. **MIL-STD-704A** can be met with an additional transorb (see figure 2).

The small size, high reliability, and military processing availability make these filters ideal for military or aerospace applications.

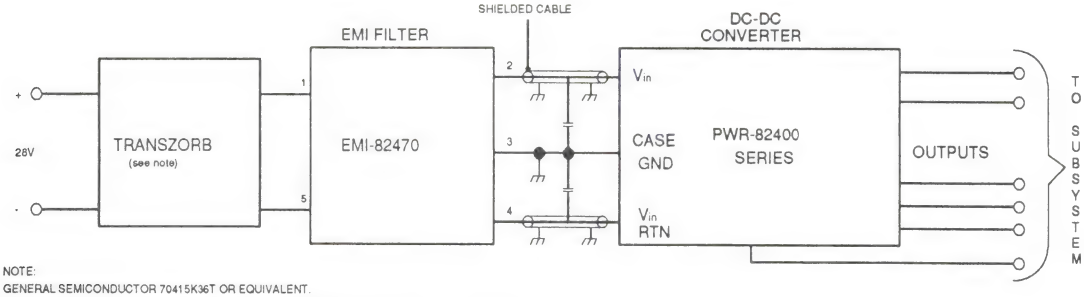
FEATURES

- ***Meets MIL-STD-461B***
- ***Meets MIL-STD-704 B, C, D, E***
- ***Small Size (2.09" x 1.11" x 0.495")***
- ***Operates from -55 to +125°C***
- ***Military Processing Available***



NOTE:
C1 AND C2 ARE REQUIRED FOR CE03 AND RE02 NARROW BAND ONLY
C1 = C2 = 200pf-0.1Uf, 100V CERAMIC. ACTUAL VALUE AND LOCATION DEPENDS ON THE SYSTEM DESIGN AND COMMON-MODE NOISE.

FIGURE 1. EMI FILTER CONNECTION DIAGRAM TO MEET MIL-STD-461B AND MIL-STD-704 B, C, D, E



NOTE:
GENERAL SEMICONDUCTOR 70415K36T OR EQUIVALENT.
(ONLY REQUIRED TO MEET 80 VOLT 100msec SPIKE,NOT REQUIRED FOR 600 VOLT,50usec SPIKE.)

FIGURE 2. EMI FILTER CONNECTION DIAGRAM TO MEET MIL-STD-704A

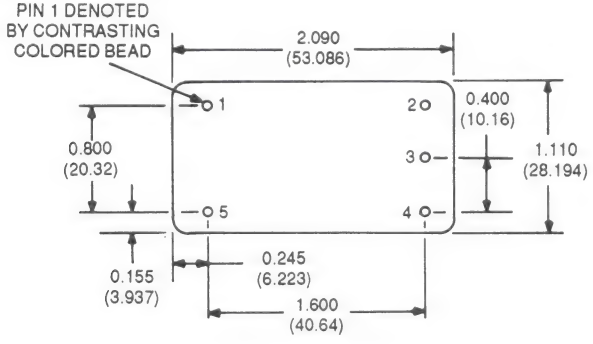
TABLE 1. SPECIFICATIONS

All conditions at +25°C unless otherwise specified.

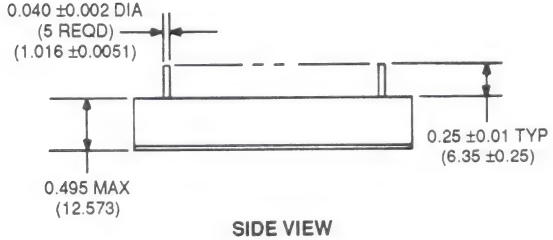
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage	Steady State	0	28	40	Vdc(see note)
Input Current	dc ripple			5 0.7	Amps Amps rms
Input Clamping Voltage	-55 to +125°C	41.5	50	58.5	Vdc
Output Voltage	Steady State		-0.5	-1.4	% of V_{in}
Output Current	Steady State			5	Amps
DC Resistance	Steady State		0.03	0.07	Ohms
Power Dissipation	Max Current		0.7	1	Watt
Noise Reduction	100kHz to 50Mhz	40	50		dB
Capacitance	Any pin-to-case			4000	pF
Isolation	Any pin-to-case (at 500 Vdc)	100			MOhms
Case Operating Temp.		-55		+125	°C
Weight				2.29 65	oz grams

NOTE: - Derate V_{in} linearly to 33 Vdc at +125°C.

Unless otherwise specified, dimensions are in inches ± 0.005 (millimeters ± 0.127).



BOTTOM VIEW



SIDE VIEW

FIGURE 3. MECHANICAL OUTLINE

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by ILC Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.

Specifications are subject to change without notice.

2/92

TABLE 2. PIN ASSIGNMENTS

PIN NUMBER	FUNCTION
1	Vin
2	Vout
3	CASE GND
4	Vout RTN
5	Vin RTN

PROCESSING AND ENVIRONMENTAL SCREENING

All of DDC's EMI-82470 EMI Filters are packaged in a fully hermetic metal case with a parallel seam welded cover and undergo the following standard environmental screening:

- Element evaluation: Per Method 5008 of MIL-STD-883
- Pre-Cap internal visual inspection: Per Method 2017
- Stabilization Bake: 24 hours at 150°C
- Temperature Cycle: 10 times per Method 1010, Cond. B
- Constant Acceleration: 500g per Method 2001
- Gross Leak: Per Method 1014, Cond. C
- Fine Leak: Per Method 1014, Cond. A
- Burn-In: 168 hours at T_c = +125°C (Not performed on -300, -100 units)
- Final Electrical Test: Room, Hot, Cold (Testing at +25°C only for -300 units)
- Final External Visual Inspection: Per Method 2009

ORDERING INFORMATION

(See Processing and Environmental Screening.)

EMI-82470-110

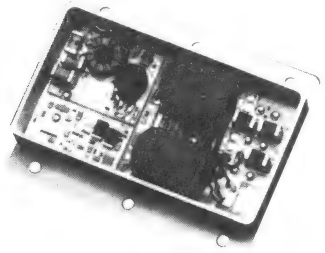
- Reliability Grade:
  - 0= Standard DDC Processing
  - 1= Military processing available*
  - 2= Military processing available but without QCI testing*
- Temperature Range:
  - 1 = -55°C to +125°C
  - 3 = 0°C to +70°C

*Consult factory for details.

L

PWR-82400 SERIES

60 WATT, TRIPLE OUTPUT DC - DC CONVERTERS



DESCRIPTION

The PWR-82400 Series are full mil temperature range 60 watt dc-dc converters. The output is characterized from -55°C to +125°C. Processing includes element evaluation and full environmental screening, thus eliminating the need for complex specification control drawings. Military processing is available.

The PWR-82400/402 are 60 watt triple output, 225 kHz dc-dc converters. The PWR-82400 operates over a wide input range of 16V to 40Vdc and supplies ±15V at 1.33A each and +5V at 4A while the PWR-82402 supplies ±12V at 1.7A each and +5V at 4A. High input-to-output isolation along with separate output returns enables the user to power both sensitive analog circuitry while maintaining isolation from digital signals. The PWR-82400 Series are short circuit protected by using internal pulse by pulse current limit circuitry which monitors the output load. Excellent line and load regulation are achieved by monitoring the +5V output thru o[illegible] coupling. In addition, the output ripp[illegible] is typically 50mVp-p thru the use [illegible] internal output filters.

The PWR-82400 Series dc-dc converters make an excellent choice for distributed power applications with their small size, high power density, and military processing availability .

FEATURES

- ***-55°C To +125°C Electrical Characteristic Operation.***
- ***Military Processing Available***
- ***±15V and +5V or ±12V and +5V Output Operation from 16 to 40Vdc Input Range***
- ***Internal Input Filter***
- ***Meets Shock and Vibration per MIL-STD-883 Method 2007***
- ***2,650,000 Hrs MTBF***
- ***19.4 Watts Per Cubic Inch Power Density***

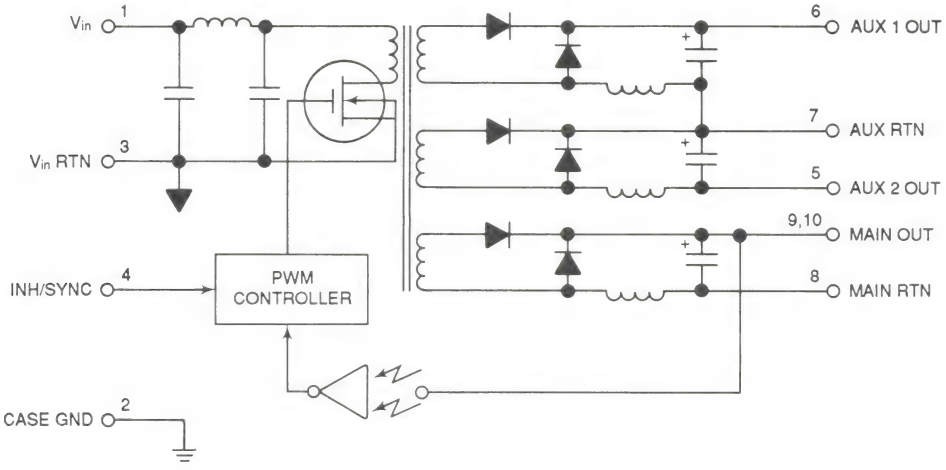


FIGURE 1. PWR-82400 SERIES BLOCK DIAGRAM

TABLE 1. ABSOLUTE MAXIMUM RATINGS	
Input Voltage	16V to 50Vdc
Power Output	Internally limited, 60W
Short Circuit Duration	Indefinite
Temperature Range (See note 1.)	Operating: -55°C to +125°C case
	Storage: -65°C to +150°C
Soldering	250°C for 10 seconds

TABLE 2. SPECIFICATIONS

T_C = -55°C to +125°C, Input voltage range = 16Vdc to 40Vdc unless otherwise specified.

PARAMETER	CONDITIONS	PWR-82400			PWR-82402			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
OUTPUT								
Voltage								
Main	V_{in}=28Vdc, T_C=25°C	4.90	4.95	5.05	4.90	5.00	5.05	Vdc
Aux1	Full Load	15.05	15.30	15.55	11.65	12.00	12.55	Vdc
Aux2		-15.55	-15.30	-15.05	-12.55	-12.00	-11.65	Vdc
Tempco								
Main			50			50		ppm/°C
Aux1			150			150		ppm/°C
Aux2			150			150		ppm/°C
Current								
Main	See note 2.			4.0			4.0	Adc
Aux1				1.33			1.7	Adc
Aux2				-1.33			-1.7	Adc
Ripple								
Main	Full Load		50	85		50	85	mV_{p-p}
Aux1	DC to 1MHz		50	85		50	85	mV_{p-p}
Aux2	V_{in}=28Vdc		50	85		50	85	mV_{p-p}
Power	See notes 1 & 2.			60			60	W
REGULATION								
Line								
Main	V_{in}=19 to 40Vdc		0.05	0.1		0.05	0.1	%
Aux1	Full Load		1.0	1.3		1.0	1.3	%
Aux2			1.0	1.3		1.0	1.3	%
Load								
Main	1% of Full Load to Full Load		0.5	1.0		0.5	1.0	%
Aux1	V_{in}=28Vdc		2.0	3.0		2.0	3.0	%
Aux2			2.0	3.0		2.0	3.0	%
INPUT								
Current	No Load		50	80		50	80	mAdc
	Inhibited		25	35		25	35	mAdc
EFFICIENCY	Full Load, T_C=25°C See figure 3. V_{in}=28Vdc	80	83		80	83		%
I/O ISOLATION	500Vdc	100			100			M Ohm
INHIBIT/SYNC								
P_O sync	Required for sync operation.	4.5			4.5			W
Logic Low				0.8			0.8	Vdc
Logic High		2.0			2.0			Vdc
I_{il} inhibit			0.5	1.0		0.5	1.0	mAdc
I_{ih} inhibit			2.0	2.75		2.0	2.75	mAdc
I_i sync		40			40			mA ac peak
Start-up Time:								
From Inhibit			5	10		5	10	mS
From V_{in}			30	40		30	40	mS
Sync freq	V_{in} = 28Vdc	260		370	260		370	kHz
Sync duty cycle	V_{in} = 28Vdc	50		90	50		90	%
SWITCHING FREQ			225			225		kHz
WEIGHT				160			160	g

NOTES: 1. Above 100°C, derate linearly to 10W at 125°C. (See figure 2.)
2. Below V_{in}=18Vdc, derate linearly to 30W at V_{in}=16Vdc.

INPUT

The PWR-82400 Series accepts an input voltage range of 16V to 40Vdc and uses an internal input Pi filter to limit the input reflected current ripple noise. Full power operation is capable down to 18Vdc. For operation during MIL-STD-704D emergency conditions refer to Figure 4.

INHIBIT/SYNC

The PWR-82400 Series allows for both inhibit or synchronization by applying a TTL signal to Pin 4. For the inhibit feature, Pin 4 is held low thereby disabling the internal PWM and halting operation of the converter. This allows for remote turn on and turn off of the converter with very low quiescent current during the off cycle.

Synchronization is achieved by applying a TTL signal to Pin 4 with a duty cycle from 50 to 90 percent. The external synchronization frequency range is 260 kHz to 370 kHz. This feature allows the user to synchronize the converter with a system clock thus eliminating false triggering from digital and system generated noise. For proper sync operation, the sync pulse input current should be 40mA min., and a minimum load of 4.5W maintained at the output of the converter.

THERMAL MANAGEMENT

The PWR-82400 Series converters operate from -55°C to +125°C case temperature. Full power output is from -55°C to +100°C case with derating to +125°C case as shown in Figure 2. The use of forced air and/or additional heat sinking may be required in high temperature applications.

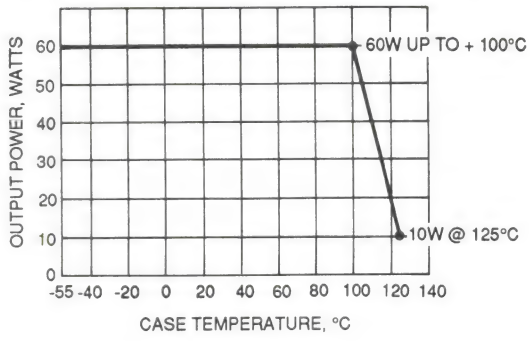


FIGURE 2. OUTPUT POWER VS. CASE TEMPERATURE

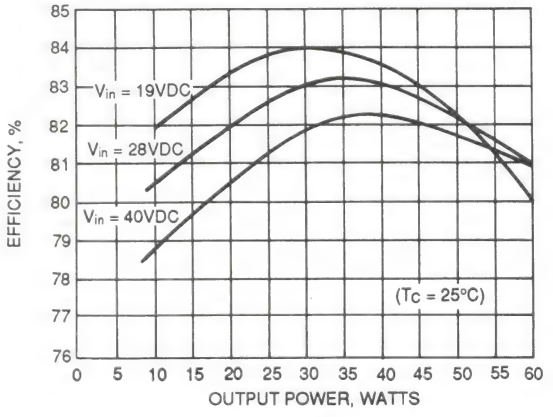


FIGURE 3. TYPICAL EFFICIENCY VS. OUTPUT POWER

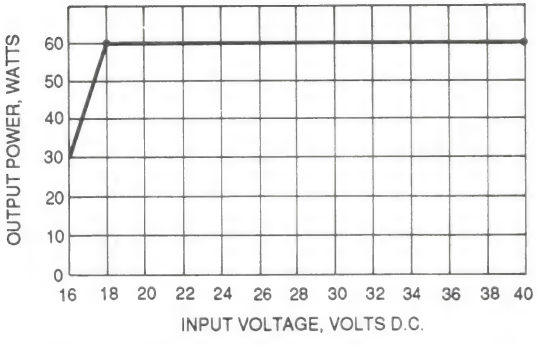


FIGURE 4. OUTPUT POWER VS. INPUT VOLTAGE

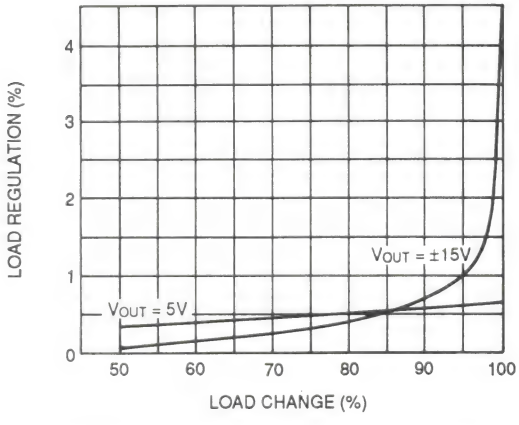


FIGURE 5. LOAD REGULATION VS. %LOAD CHANGE TO FULL LOAD

TABLE 3. PIN ASSIGNMENTS			
PIN #	FUNCTION	PWR-82400	PWR-82402
1	V_{in}		
2	CASE GND		
3	V_{in} RTN		
4	INH/SYNC		
5	AUX 2 OUT	-15V	-12V
6	AUX 1 OUT	+15V	+12V
7	AUX RTN		
8	MAIN RTN		
9	MAIN OUT	+5V	+5V
10	MAIN OUT	+5V	+5V

Dimensions in inches (mm).

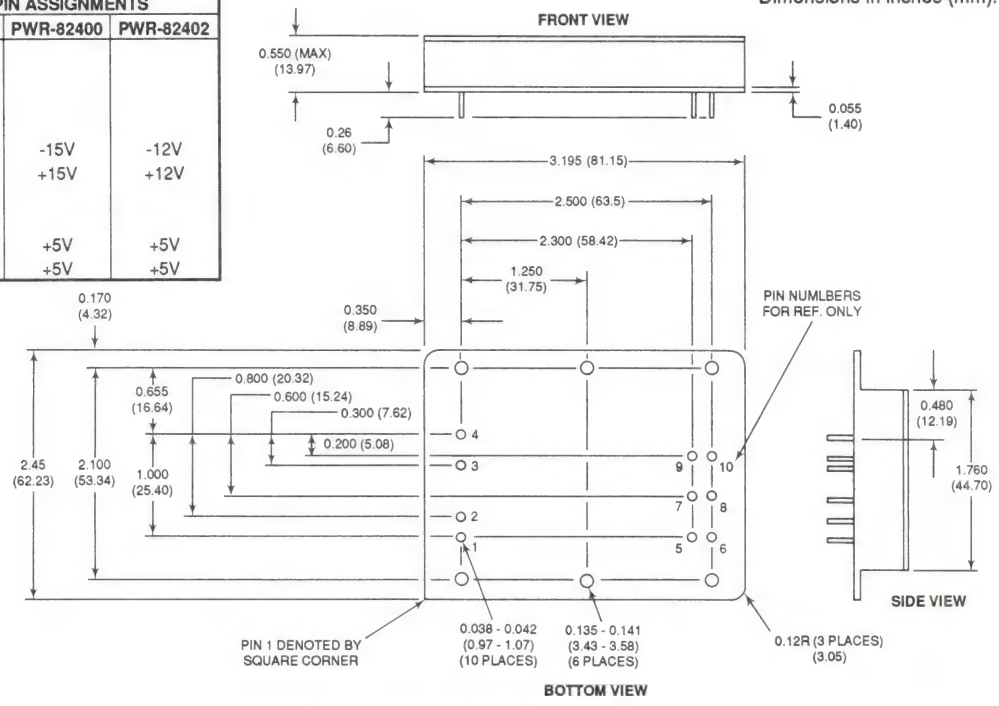


FIGURE 6. MECHANICAL OUTLINE

PROCESSING AND ENVIRONMENTAL SCREENING

All of DDC's PWR-82400 Series DC-DC converters are packaged in a fully hermetic metal case with a parallel seam welded cover and undergo the following standard environmental screening:

- Element evaluation: Per Method 5008 of MIL-STD-883
- Pre-Cap internal visual inspection: Per Method 2017
- Stabilization Bake: 24 hours at 150°C
- Temperature Cycle: 10 times per Method 1010, Cond. B
- Constant Acceleration: 500g per Method 2001
- Gross Leak: Per Method 1014, Cond. C
- Fine Leak: Per Method 1014, Cond. A
- Burn-In: 168 hours at T_c = +100°C (Not performed on -300, -100 units)
- Final Electrical Test: Room, Hot, Cold (Testing at +25°C only for -300 units)
- Final External Visual Inspection: Per Method 2009

Vibration testing in all 3 axes , per MIL-STD-883, Method 2007 Cond. A, can also be performed.

D

ORDERING INFORMATION

(See Processing and Environmental Screening.)

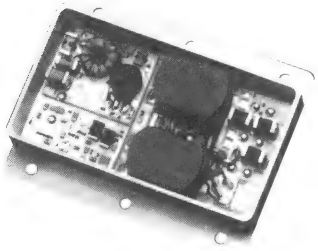
PWR-8240X-110

- Reliability Grade:
  - 0= Standard DDC Processing
  - 1= Military processing available
  - 2= Military processing available but without QCI testing
- Temperature Range:
  - 1 = -55°C to +125°C
  - 3 = 0°C to +70°C
- Auxiliary Outputs:
  - 0 = ±15 Vdc
  - 2 = ±12 Vdc

L

PWR-82401 and PWR-82403

60 WATT, TRIPLE OUTPUT DC - DC CONVERTERS



DESCRIPTION

The PWR-82401/403 are full mil temperature range 60 watt dc-dc converters. The output is characterized from -55°C to +125°C. Processing includes element evaluation and full environmental screening, thus eliminating the need for complex specification control drawings. Military processing is available.

The PWR-82401/403 are 60 watt triple output, 225 kHz dc-dc converters. The PWR-82401 operates over a wide input range of 16V to 40Vdc and supplies ±15V at 1.33A each and +5V at 4A while the PWR-82403 supplies ±12V at 1.7A each and +5V at 4A. High input-to-output isolation along with separate output returns enables the user to power both sensitive analog circuitry while maintaining isolation from digital signals. The PWR-82401/403 are short circuit protected by using internal pulse by pulse current limit circuitry which monitors the output load. Excellent line and load regulation are achieved by monitoring the +5V output thru opto coupling. In addition, the output ripple is typically 50mVp-p thru the use of internal output filters.

The PWR-82401/403 dc-dc converters make an excellent choice for distributed power applications with their small size, high power density, and military processing availability.

FEATURES

- *-55°C To +125°C Electrical Characteristic Operation.*
- *Military Processing Available*
- *Pin Compatable Version with MFW28515T and MFW28512T*
- *±15V and +5V or ±12V and +5V Output Operation from 16 to 40Vdc Input Range*
- *Internal Input Filter*
- *Meets Shock and Vibration per MIL-STD-883 Method 2007*
- *2,650,000 Hrs MTBF*
- *19.4 Watts Per Cubic Inch Power Density*

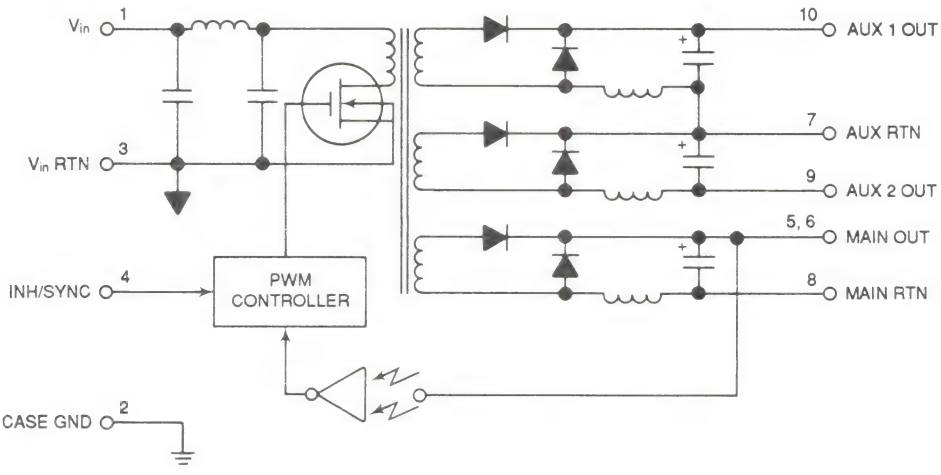


FIGURE 1. PWR-82401/403 BLOCK DIAGRAM

TABLE 1. ABSOLUTE MAXIMUM RATINGS	
Input Voltage	16V to 50Vdc
Power Output	Internally limited, 60W
Short Circuit Duration	Indefinite
Temperature Range (See note 1.)	Operating: -55°C to +125°C case
	Storage: -65°C to +150°C
Soldering	250°C for 10 seconds

TABLE 2. SPECIFICATIONS

T_C = -55°C to +125°C, Input voltage range = 16Vdc to 40Vdc unless otherwise specified.

PARAMETER	CONDITIONS	PWR-82401			PWR-82403			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
OUTPUT								
Voltage								
Main	V_{in}=28Vdc, T_C=25°C	4.90	4.95	5.05	4.90	5.00	5.05	Vdc
Aux1	Full Load	15.05	15.30	15.55	11.65	12.00	12.55	Vdc
Aux2		-15.55	-15.30	-15.05	-12.55	-12.00	-11.65	Vdc
Tempco								
Main			50			50		ppm/°C
Aux1			150			150		ppm/°C
Aux2			150			150		ppm/°C
Current								
Main	See note 2.			4.0			4.0	Adc
Aux1				1.33			1.7	Adc
Aux2				-1.33			-1.7	Adc
Ripple								
Main	Full Load		50	85		50	85	mV_{p-p}
Aux1	DC to 1MHz		50	85		50	85	mV_{p-p}
Aux2	V_{in}=28Vdc		50	85		50	85	mV_{p-p}
Power	See notes 1 & 2.			60			60	W
REGULATION								
Line								
Main	V_{in}=19 to 40Vdc		0.05	0.1		0.05	0.1	%
Aux1	Full Load		1.0	1.3		1.0	1.3	%
Aux2			1.0	1.3		1.0	1.3	%
Load								
Main	1% of Full Load to Full Load		0.5	1.0		0.5	1.0	%
Aux1	V_{in}=28Vdc		2.0	3.0		2.0	3.0	%
Aux2			2.0	3.0		2.0	3.0	%
INPUT								
Current	No Load		50	80		50	80	mAdc
	Inhibited		25	35		25	35	mAdc
EFFICIENCY	Full Load, T_C=25°C See figure 3. V_{in}=28Vdc	80	83		80	83		%
I/O ISOLATION	500Vdc	100			100			M Ohm
INHIBIT/SYNC								
P_O sync	Required for sync operation.	4.5			4.5			W
Logic Low				0.8			0.8	Vdc
Logic High		2.0			2.0			Vdc
I_{il} inhibit			0.5	1.0		0.5	1.0	mAdc
I_{ih} inhibit			2.0	2.75		2.0	2.75	mAdc
I_i sync		40			40			mAac peak
Start-up Time:								
From Inhibit			5	10		5	10	mS
From V_{in}			30	40		30	40	mS
Sync freq	V_{in} = 28Vdc	260		370	260		370	kHz
Sync duty cycle	V_{in} = 28Vdc	50		90	50		90	%
SWITCHING FREQ			225			225		kHz
WEIGHT				160			160	g

NOTES: 1. Above 100°C, derate linearly to 10W at 125°C. (See figure 2.)

2. Below V_{in}=18Vdc, derate linearly to 30W at V_{in}=16Vdc.

INPUT

The PWR-82401/403 accepts an input voltage range of 16V to 40Vdc and uses an internal input Pi filter to limit the input reflected current ripple noise. Full power operation is capable down to 18Vdc. For operation during MIL-STD-704D emergency conditions refer to Figure 4.

INHIBIT/SYNC

The PWR-82401/403 allows for both inhibit or synchronization by applying a TTL signal to Pin 4. For the inhibit feature, Pin 4 is held low thereby disabling the internal PWM and halting operation of the converter. This allows for remote turn on and turn off of the converter with very low quiescent current during the off cycle.

Synchronization is achieved by applying a TTL signal to Pin 4 with a duty cycle from 40 to 98 percent. The external synchronization frequency range is 250 kHz to 400 kHz. This feature allows the user to synchronize the converter with a system clock thus eliminating false triggering from digital and system generated noise.

THERMAL MANAGEMENT

The PWR-82401/403 converters operate from -55°C to +125°C case temperature. Full power output is from -55°C to +100°C case with derating to +125°C case as shown in Figure 2. The use of forced air and/or additional heat sinking may be required in high temperature applications.

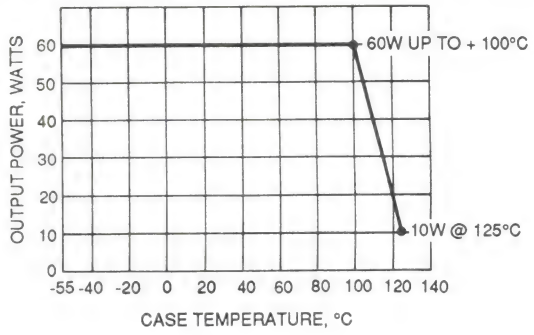


FIGURE 2. OUTPUT POWER VS. CASE TEMPERATURE

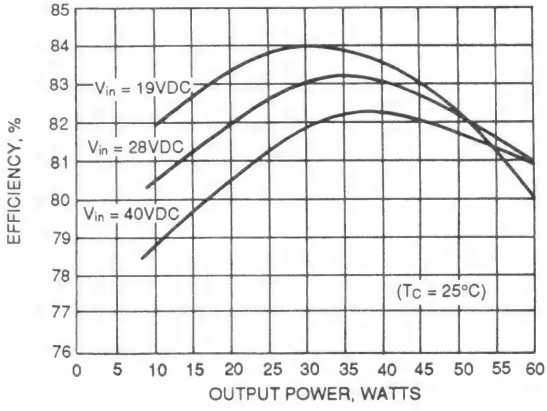


FIGURE 3. TYPICAL EFFICIENCY VS. OUTPUT POWER

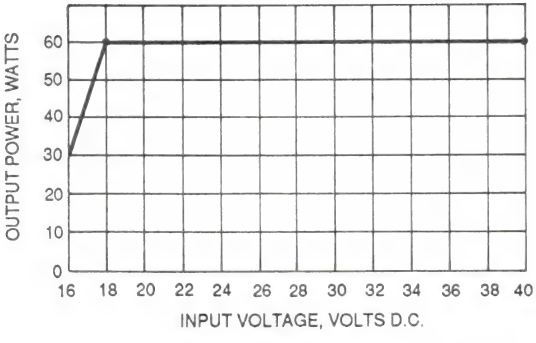


FIGURE 4. OUTPUT POWER VS. INPUT VOLTAGE

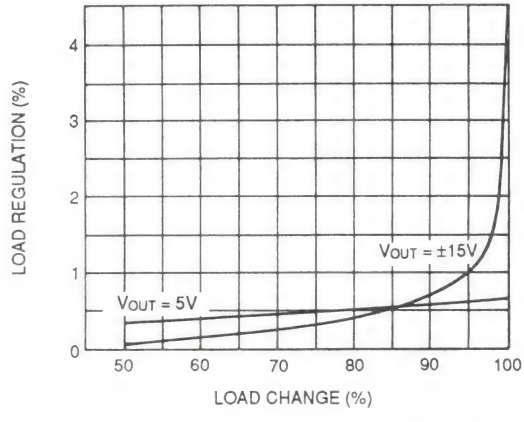


FIGURE 5. LOAD REGULATION VS. %LOAD CHANGE TO FULL LOAD

TABLE 3. PIN ASSIGNMENTS			
PIN #	FUNCTION	PWR-82401	PWR-82403
1	V_{in}		
2	CASE GND		
3	V_{in} RTN		
4	INH/SYNC		
5	MAIN OUT	+5V	+5V
6	MAIN OUT	+5V	+5V
7	AUX RTN		
8	MAIN RTN		
9	AUX 2 OUT	-15V	-12V
10	AUX 1 OUT	+15V	+12V

Dimensions in inches (mm).

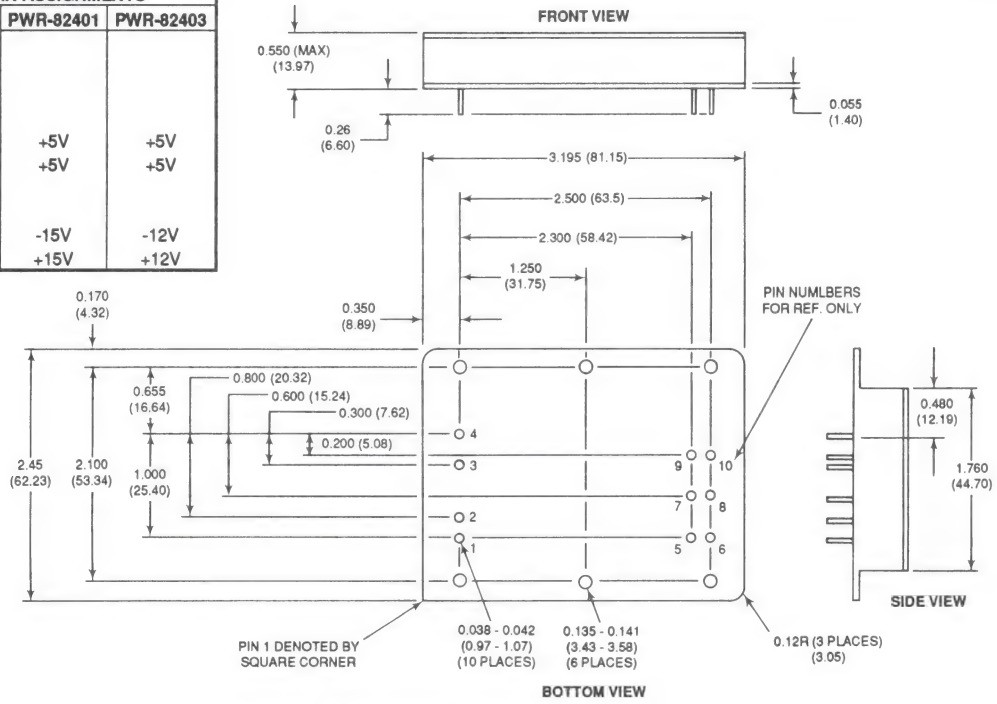


FIGURE 6. MECHANICAL OUTLINE

PROCESSING AND ENVIRONMENTAL SCREENING

All of DDC's PWR-82401/403 DC-DC converters are packaged in a fully hermetic metal case with a parallel seam welded cover and undergo the following standard environmental screening:

- Element evaluation: Per Method 5008 of MIL-STD-883
- Pre-Cap internal visual inspection: Per Method 2017
- Stabilization Bake: 24 hours at 150°C
- Temperature Cycle: 10 times per Method 1010, Cond. B
- Constant Acceleration: 500g per Method 2001
- Gross Leak: Per Method 1014, Cond. C
- Fine Leak: Per Method 1014, Cond. A
- Burn-In: 168 hours at T_c = +100°C (Not performed on -300, -100 units)
- Final Electrical Test: Room, Hot, Cold (Testing at +25°C only for -300 units)
- Final External Visual Inspection: Per Method 2009

Vibration testing in all 3 axes , per MIL-STD-883, Method 2007 Cond. A, can also be performed.

C

ORDERING INFORMATION

(See Processing and Environmental Screening.)

PWR-8240X-110

- Reliability Grade:
  - 0= Standard DDC Processing
  - 1= Military processing available
  - 2= Military processing available but without QCI testing
- Temperature Range:
  - 1 = -55°C to +125°C
  - 3 = 0°C to +70°C
- Auxiliary Outputs:
  - 1 = ±15 Vdc
  - 3 = ±12 Vdc

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SECTION M
SYSTEMS

PRODUCT SUMMARY TABLE

MODEL	PACKAGE	DESCRIPTION/FEATURES	PAGE
6489	Cabinet 48 x 22 x 24"	NATO SINS/GPS RETRANSMISSION SYSTEM provides a complete real-time interface between NATO SINS, NAVSTAR GPS, and existing navigation systems. Automatic selection of NATO SINS or secondary compass. Contains diagnostic computer and LED BIT fault indication at card level.	M-7
6514	Cabinet 78 x 22 x 24"	SOLID-STATE SYNCHRO RETRANSMISSION SYSTEM (SRS) that provides power boosts as well as speed ratio, ratioratio transformation of ships navigation, and attitude synchro information. It has digital implementation and modular partitioning, BITE, fully protected outputs, high reliability, and is expandable.	M-11
6480	Cabinet 67 x 21.6 x 21.6"	SOLID-STATE SYNCHRO RETRANSMISSION SYSTEM (SRS) that provides power boosts as well as speed ratio, ratio transformation of ships navigation, and attitude synchro information. It has digital implementation and modular partitioning, BITE, fully protected outputs, high reliability, and is expandable.	M-13
6322	Cabinet	SOLID-STATE SYNCHRO RETRANSMISSION SYSTEM (SRS) that provides power boosts as well as speed ratio, ratio transformation of ships navigation, and attitude synchro information. It has digital implementation and modular partitioning, BITE, fully protected outputs, high reliability, and is expandable.	M-17
6438 BR	Open frame chassis 20.25 x 23.21 x 13"	Seven channel, Hi - power, digital/synchro drive system.	M-19
DDC-6498/5521	9.96 x 3.96 x 9.875" 2.81 x 3.90 x 7.59" (DDC-5521)	39 channel switchboard synchro panel meter.	M-23
S-SERIES	Euro-Card	Building - block PC cards for SRS, IRS, and Custom system requirements.	M-27

M

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

* New Product

BACKGROUND INFORMATION

Solid-state retransmission system for ships' navigation: flexibility, availability and maintainability

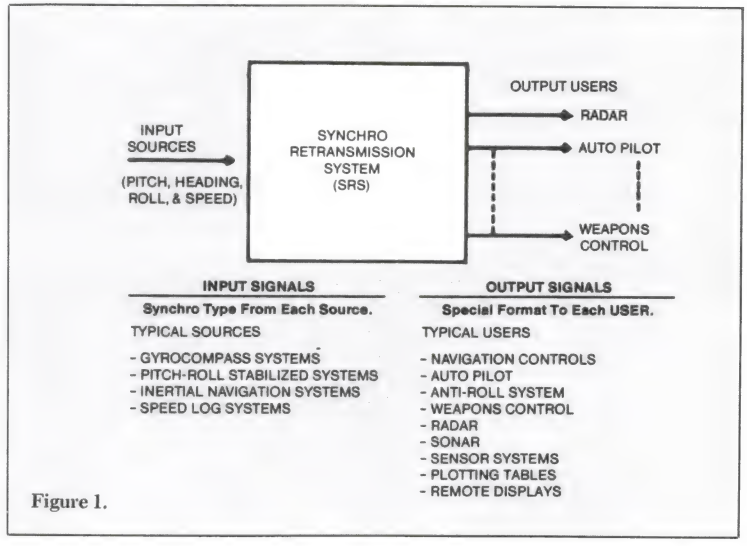

Figure 1.

Accurate distribution of ships navigation and attitude data has been a long standing shipboard requirement. The task of distributing this information, which is usually generated in the form of single speed and multi-speed synchro data, is normally performed by a synchro retransmission system (a typical system is illustrated in Figure 1).

The "distribution" of this data entails more than just a simple physical routing or buffering of the input data. In many cases, the user equipment requires the data in a different format or scale factor than that supplied by the source. For example, heading data as supplied by the compass system may be in the form of multi-speed synchro data at a speed ratio of 1:1 and 1:36. A particular user requiring this heading data may require it as a multi-speed synchro, but at a speed ratio of 1:1 and 1:9, or 1:16, etc. It is even possible that the receiving system requires the heading data in a completely different form, such as a linear (AC or DC) signal or as a digital data word to interface with a computer.

To perform the preceding functions, the retransmission system must first convert the input data to an intermediate form most compatible with all the different output forms which must be generated. That is, the retransmission system must generate a common form of data from which all the output formats can be derived.

Since the data originates as a single shaft position or angle, it is obvious that this format is the least common denominator. Therefore, the first function of the retransmission system is to regenerate the input data (1:1/1:N) synchro signals as a single speed (1:1) angle. This single speed angle may then be used to regenerate the output data, via interface (transducer) devices, as required for each user.

Classic retransmission system implementations

The classic approach to implementing such a system has been an electro-mechanical one. An electro-mechanical retransmission system utilizes a precision follow-up servo loop to reproduce a physical 1:1 speed shaft angle representing the input angle (heading, pitch, roll etc.). This shaft is then geared to various output transducers to generate the required data (see Figure 2). The specific formats of the output data are governed by the output transducers. Synchro outputs are gener-

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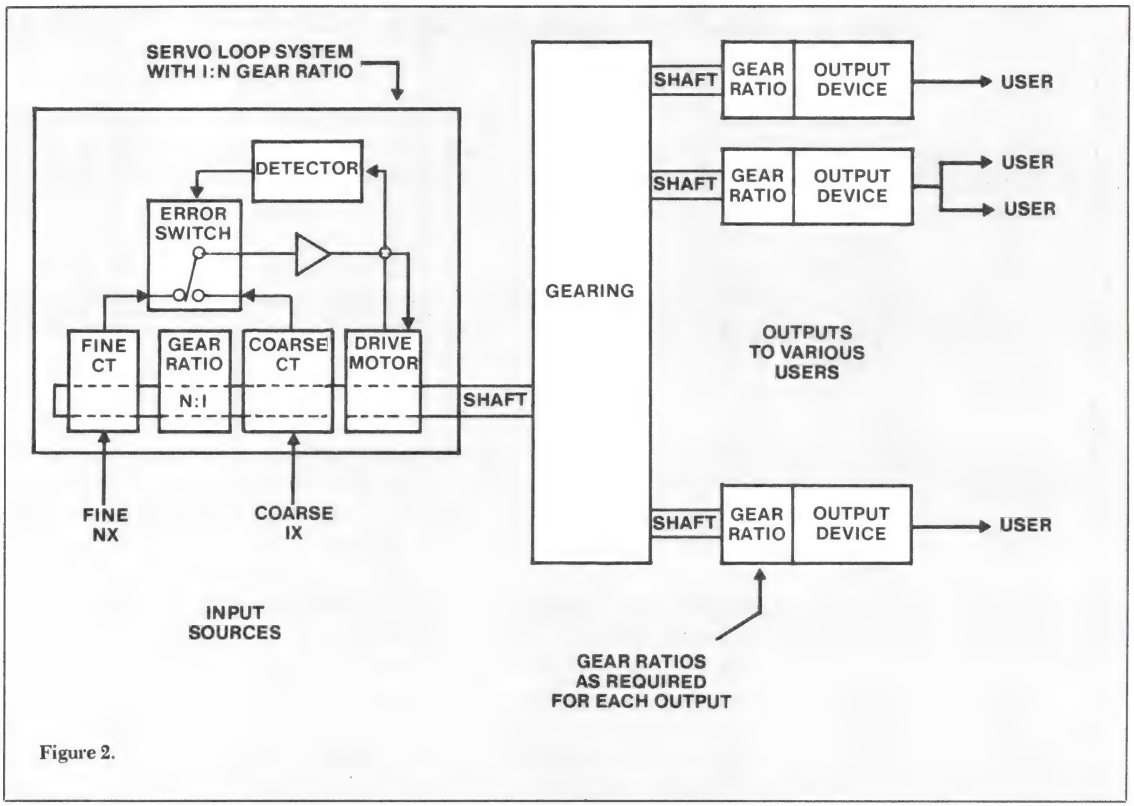


Figure 2.

ated by synchro transmitters, DC and AC outputs by multi-turn potentiometers and digital data, if required, by shaft encoders or via synchros coupled with synchro to digital converters.

The gearing required in such a system must be precision gearing usually employing anti-backlash techniques to achieve the required accuracies. Likewise, the electro-mechanical follow-up loop and its dynamics are critical. The loop dynamics of follow-up servos are sensitive to and determined by physical loading of the shafts and the inertia of the mechanical rotating components involved. These, in turn, are variables that change with age and are subject to physical "wear and tear." Periodic maintenance efforts, to readjust electronic gains and gearing clearances as well as for lubrication and removal of accumulated dirt, are necessary. Failure to keep the electro-mechanical loop so optimized results in either sluggish operation (causing output data to seriously lag input data) or jittering (hunting) due to worn gearing or bearings.

For ships in the Frigate class, where a relatively large number of different equipments may need to be interfaced, the output requirements in terms of channels may run from 40 to 100 interfaces. An electro-mechanical (EM) approach would, therefore, most likely require two to three six-foot equipment racks for such a system.

In addition to the size estimate for the electro-mechanical approach, the next obvious disadvantage can be seen as the lack of flexibility for such a system. Once implemented, such a system would require extensive change or modification to add channels which might require different gear ratios. The central common shaft, being a physical one, is not easily "extended" or "routed." There are many other aspects of EM systems which can be reviewed.

The following is a brief summary of the factors in the electro-mechanical approach:

- Shipboard Space and Weight Requirements
  - Mechanical system is bulky and occupies considerable space
- Initial and Lifetime Costs
  - Higher initial cost
  - Periodic maintenance and adjustments for wear
  - Mechanical repairs cause downtime
- Accuracy and Availability
  - Trim adjustments are required
  - Wear and loading causes inaccuracies
  - BITE fault indication difficult
  - Repair time relatively long
- Flexibility
  - Modifications and additions are very difficult
  - Computer interfacing requires additional electronics
  - Technological obsolescence

Solid-state synchro retransmission unit

Within the past 15 years, solid-state devices equivalent to many electro-mechanical servo components have been developed. These devices, in new applications, have replaced the use of the EM devices. The need for such devices and the majority of their applications came about as more and more systems employing digital computers were developed. These devices, Synchro-to-Digital Converters (S/D) and Digital-to-Synchro Converters (D/S), serve as the signal data converters which link the analog world with the digital world. Very simply, an S/D is a device which is analogous to an input EM follow-up servo loop. Synchro inputs are converted to a digital word which is a "digital shaft angle" as opposed to a physical shaft. Likewise, a D/S converter is directly analogous to the basic output synchro element known as a Control Transmitter (CX). Immediately it can be seen that in a basic system a direct replacement can be made. Synchro inputs are converted to single speed digital shaft angles which are wired to digital to synchro converters which generate the required synchro outputs (see Figure 3).

Note that linear DC and AC analog outputs are generated by the solid-state equivalent of a potentiometer which is a Digital to Analog (D/A) converter. An obvious and very important feature of a solid-state synchro retransmission system becomes apparent when one considers the "flexibility" the digital shaft angle provides as compared to a physical shaft. Remember, the single speed shaft must be modified to effect speed ratio changes and additional outputs. In an EM system this represents a major modification to the system, while in a solid-state system speed changes are accomplished by a few wire changes on a connector and additional outputs are accommodated by the simple addition of more plug-in output printed circuit cards.

The flexibility of a digital solid-state system is only one of many reasons that this type of implementation is the most desirable. Some others are:

- Size is smaller
- Expansion for future requirements is much easier and less costly
- Computer compatibility is built-in
- Reliability and system availability is much higher
- On-Line-Built-In Test (BITE) is easy to accomplish
- Periodic maintenance and calibration are unnecessary
- Fault monitoring and isolation is achievable
- Manual fault isolation and repairs are much easier due to plug-in modular techniques and fault indicators.

One company's basic approach to the implementation of a solid-state synchro retransmission system is an existing system designed for and delivered to the Royal Netherlands for their Standard Frigate Program.

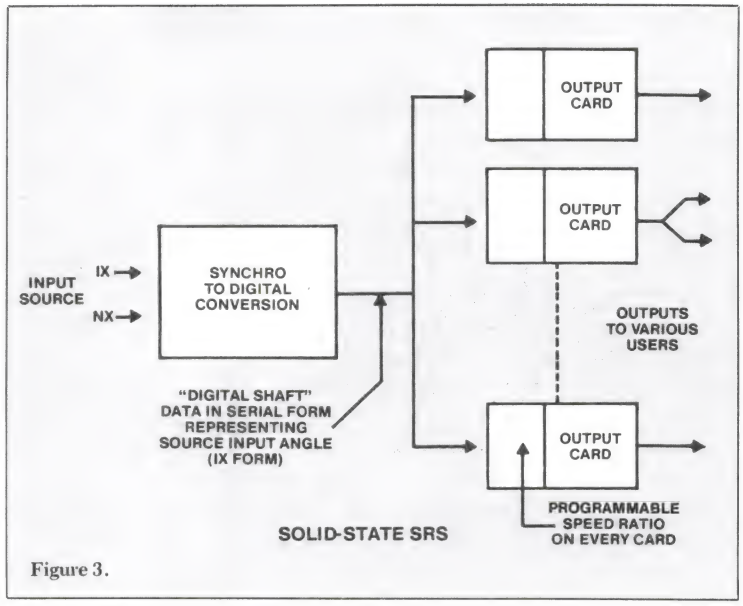


Figure 3.

ILC Data Device Corporation's (DDC) Model 6322 solid-state retransmission system

The RNLN's "S" Class Frigates utilize these systems to consolidate all prime navigation synchro data transformations and distribution. Chosen primarily as the most cost effective solution for the RNLN's requirements, the all solid-state retransmission system also provides bonus features of greatly reduced volume and maintenance requirements as well as increased reliability, system dependability and unprecedented flexibility.

The solid-state synchro retransmission system (SRS) (Figure 4), provides power boost as well as speed ratio transformations of ship's navigation and attitude synchro information. The system then distributes the data in either synchro, DC or AC format to all ship's systems requiring this data. Traditionally these functions had been provided by bulky and expensive electro-mechanical servo systems or on a distributed channel by channel basis as required. This shipboard data handling system is directly applicable to the U.S. Navy submarine and surface ship requirement for synchro signal amplifiers or multi-speed Repeaters which are currently implemented with electro-mechanical systems. The synchro retransmission system actually goes beyond basic synchro signal amplifier capabilities by providing the option of retransmitting the data in any speed ratio on a channel by channel basis

DDC's approach to the SRS design concentrated mainly on building a system which alleviated the problems inherent in the electro-

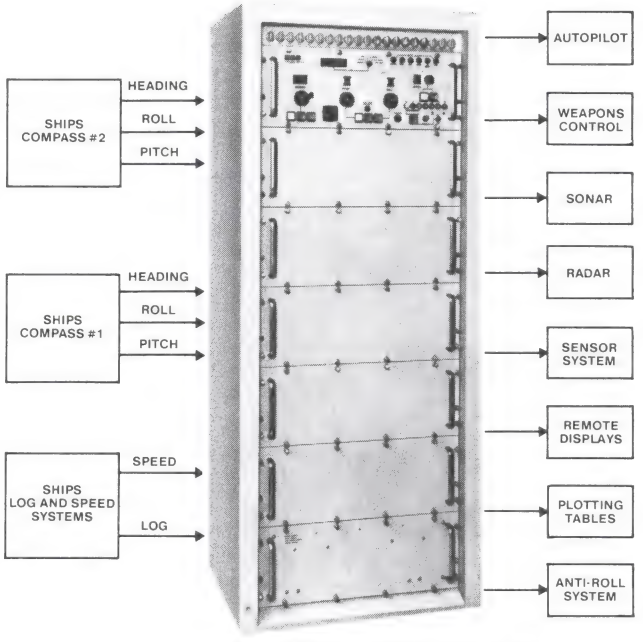


Figure 4.

mechanical approach: namely, lack of flexibility, poor maintainability, requirements for adjustments and size. As an established supplier of all the solid-state servo components necessary, DDC was able to concentrate its full engineering efforts on the system design rather then the detail design of the converters themselves.

Flexibility was achieved by creating functional "building blocks" or "modules" where each function, such as Synchro-to-Digital (S/D) conversion and Digital-to-Synchro (D/S) conversion was designed on Eurosized plug-in printed circuit boards. The heart of this building block concept is at the printed circuit board (PCB) level. That is, the PCBs or cards were functionally partitioned and electronically designed to be stand alone devices. This concept was especially successful in the area of the cards designed to serve as the output transducers. That is, each different type of EM transducer which is being replaced by its solid-state equivalent can be equated to a single card assembly. For example, for a D/S converter output function which is equivalent to a CX transducer, there is one plug-in card to accomplish this function. This permits functions to be added, deleted or changed with a minimum of difficulty.

To further increase flexibility, the output functions were designed incorporating, on the PCB, a programmable Digital Multiplier for the Digital shaft angle input. Output Digital-to-Synchro speed ratios are changed simply by changing a few programming jumpers on the chassis connector into which the card plugs in.

The benefits of this design are:

- All D/S cards are identical; they are programmed for speed ratio when they are plugged into the SRS
- Speed ratio changes are easily accomplished by changing a few jumpers on the chassis connector

Digital-to-Analog output modules were also designed for scale factor programming by the chassis connector wiring.

System availability and maintainability was greatly enhanced by providing On-Line-Built-In-Test (BITE) circuitry on every functional module. If a module malfunctions, a fault indicator (LED) on the module is lighted and a digital fault signal is generated. The fault signal is used to generate a system alarm to indicate a malfunction and the illuminated module LED is used to isolate the fault to a single module function. Repair is easily accomplished, with system power on, by the removal and replacement of the faulty plug-in module. This permits a minimum of training for on-board personnel. The incorporation of BITE on each system module provides the means to greatly increase system availability by automatic switching active redundancy of critical data channels. Information such as ship's heading which is critical to the performance of the ship, normally has two sources, a primary compass and a secondary compass. To achieve active redundancy, the heading synchro information from each compass is converted into a digital serial data word by an S/D converter card and is distributed throughout the SRS on individual serial data buses. Each output function receives the heading information from both compass 1 and compass 2 as opposed to switching prior to the input S/D converter. This method assures that data is transmitted to all outputs even if one of the compass inputs or S/D converters malfunctions. It is important to note that the heading information at the output module is

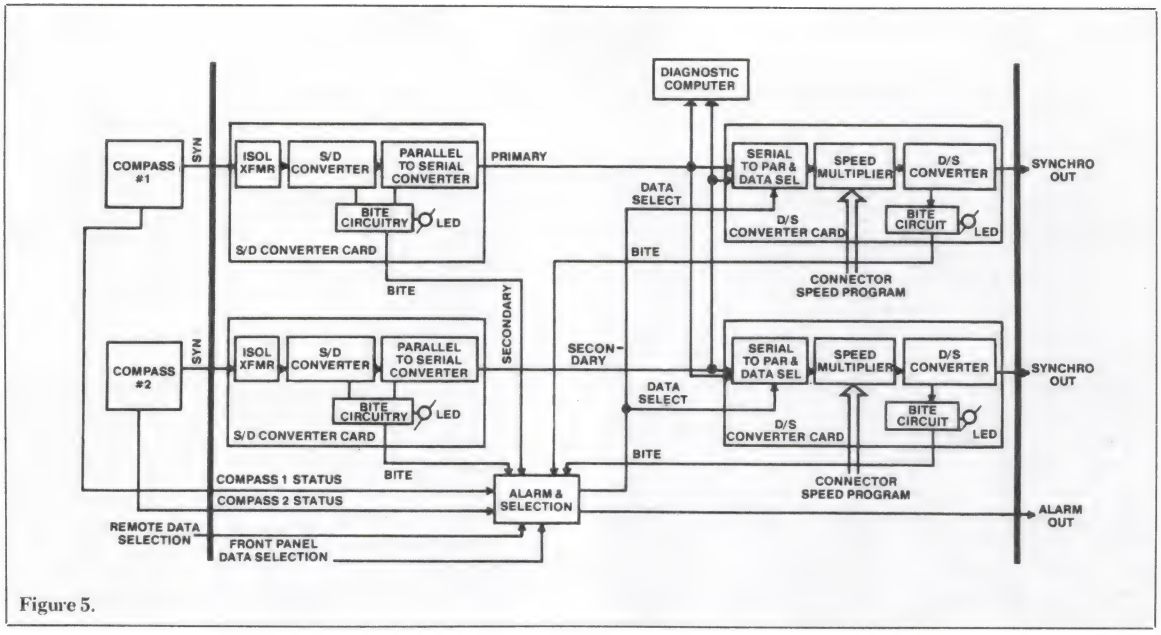


Figure 5.

completely redundant. Selection of compass data being used is controlled in three ways:

1) *Automatic Mode:* Selection is made by the status inputs from the two compasses and the BITE signals from the input S/D converter.

2) *Remote Mode:* Selection is made by a remote digital input, providing both compasses and both input S/D's are valid.

3) *Manual:* Front panel manual selection which overrides both automatic and remote selection.

Primary information, being the most accurate, is selected during normal conditions, but if the input S/D converter module fails or if the primary compass status signal indicates a problem, in the automatic mode, the system automatically switches to secondary heading without loss of information. This feature is self-healing and the system will return to primary information if the malfunction is repaired.

System maintainability was further simplified by incorporating test switches at each input and a front panel decimal display. In the normal mode of operation, input synchro angles can be displayed to check their availability or accuracy. In the test mode, the input data is taken "off line" and fixed accurate synchro angles are substituted. These accurate test angles allow calibration of external systems (users) or trouble shooting of the system using the decimal display. The incorporation of these features eliminates the requirement for special test equipment and greatly aids in system installation.

Another important feature that the solid-state design provides, which is not easily incorporated in an EM approach, is the ability to interface directly with a computer. The basic method of distributing data within the system is to use serial digital data words. These data words are easily formated for data transmission to external users via data buses such as RS232, Stanag 4156, Mil-Std-1553, etc. The computer interfaces are modular in design allowing the interface format and handshaking to be changed by the simple replacement of a printed circuit board.

The modules developed by DDC to be used as building blocks were carefully partitioned such that each new system specification would require a minimum of engineering effort. The following is a listing of major module functions;

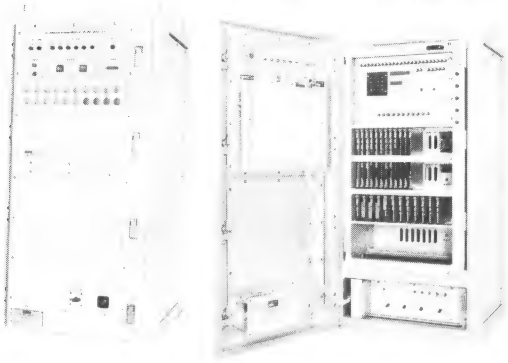
- Synchro-to-Digital Conversion: both one speed and two speed.
- Digital-to-Synchro Conversion: programmable speed output.
- Digital-to-Analog Conversion: programmable scale factor.
- Synchro Booster Amplifier: torque drive output.
- Digital-to-Display: decimal data display.
- Control Differential: summation of two angles.
- Computer Interface: RS232, Stanag 4156, Mil-Std-1553 etc.
- Microprocessor: data processing.
- Alarm and BITE: alarm output.
- Discrete-to-Digital: discrete input interface.

The use of solid-state technology and the adaptation of stand alone module functions has allowed DDC to develop a solid-state retransmission system which has alleviated the problems and disadvantages of the electro-mechanical system. The advanced systems approach provides flexibility for expansion and change, availability in case of failure, ease of maintainability to reduce training and commonality for reduced logistics and spares. □

DDC
ILC DATA DEVICE CORPORATION

MODEL 6489

SINS/GPS INTERFACE RETRANSMISSION UNIT



DESCRIPTION

The Model 6489 SINS/GPS Interface Retransmission Unit (RTU) is designed to furnish a real time communications link for messages between the NATO SINS and NAVSTAR GPS Systems. In addition the RTU provides for data communication between existing ship's navigation equipment and the SINS/GPS. This solid-state retransmission unit is an ideal interface for incorporating NATO SINS and NAVSTAR GPS to existing synchro or digital Navigation Systems. Flexibility in the design of the RTU allows for ease of reprogramming by the use of socket mounted PROM and PAL integrated circuits. ILC Data Device Corporation provides full documentation, field service maintenance, and logistic support for the Model 6489.

FEATURES

- *PROVIDES COMPLETE REAL TIME INTERFACE BETWEEN NATO SINS, NAVSTAR GPS, AND EXISTING NAVIGATION SYSTEM*
- *AUTOMATIC SELECTION OF NATO SINS OR SECONDARY COMPASS*
- *CONTAINS DIAGNOSTIC COMPUTER AND LED BIT FAULT INDICATION AT CARD LEVEL*
- *EUROCARD FORMAT*
- *ALL INPUTS AND OUTPUTS GALVANICALLY ISOLATED*
- *MEETS MIL STANDARDS*
- *FLEXIBILITY THROUGH USE OF FIELD PROVEN BUILDING BLOCKS*
- *PROM PROGRAMMED MICROPROCESSORS FOR COMPLETE FLEXIBILITY OF INTERFACE CONFIGURATION AND PROTOCOL*

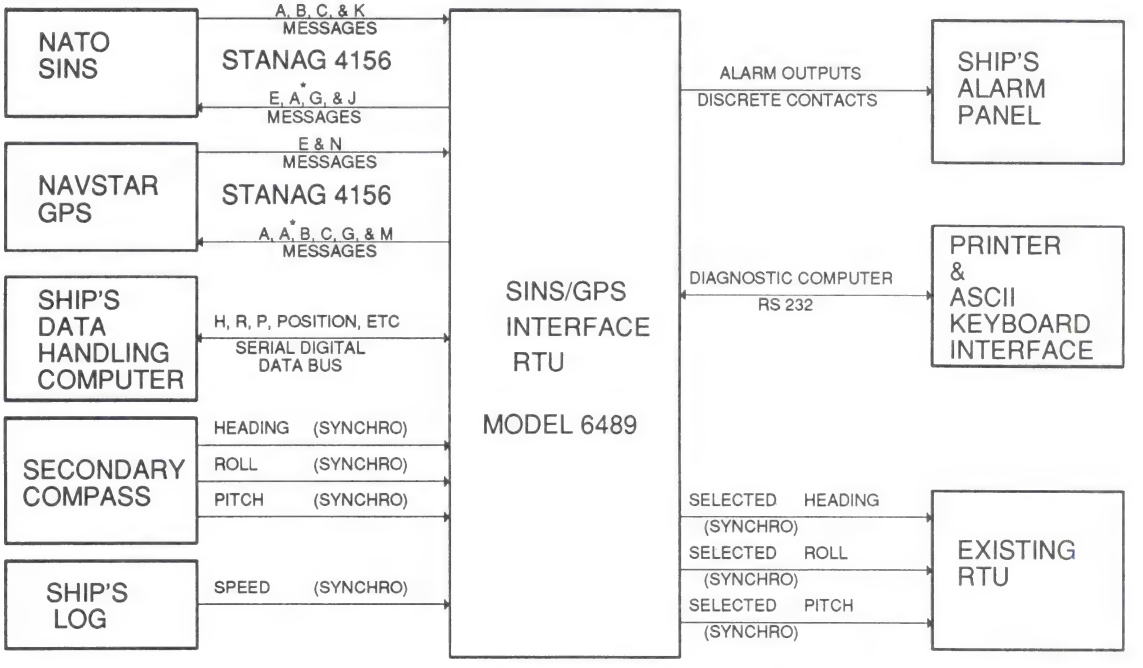


FIGURE 1. SHIPBOARD BLOCK DIAGRAM

M

SINS/GPS INTERFACE RETRANSMISSION UNIT
MODEL 6489
TECHNICAL INFORMATION

INTRODUCTION

The SINS/GPS Interface Retransmission Unit (RTU) consists of RTU subassemblies housed in a hinged, removable card cage subassembly. The card cage is in a shock mounted vibration, EMI, and drip proof welded aluminum cabinet. The SINS/GPS Interface RTU is designed to provide a data path and interface for the NATO SINS and NAVSTAR GPS and existing ship's navigation equipment.

INPUTS AND OUTPUTS

The Interface RTU acts as a real time coupler between the NATO SINS and NAVSTAR GPS for the Stanag 4156 A, B, C, and E Messages. Additional messages required by the NATO SINS and NAVSTAR GPS, such as the A* Message (Secondary Attitude) and G Message (Ship's Velocity) are derived by the RTU from the Ship's Secondary Compass and Ship's Log.

The Interface RTU also accepts all messages between the NATO SINS and NAVSTAR GPS for the processing into a format required by the existing ship navigation equipment.

Attitude information (Heading, Roll, and Pitch) derived from NATO SINS is processed with the Secondary Compass Heading, Roll, and Pitch input to provide selected Heading, Roll, and Pitch Synchro outputs.

The Interface RTU also provides a digital output to supply Attitude, Position, and Velocity information to the Ship's Data Handling Computer. The Digital output can be configured to any format such as RS422, RS232, ICI, etc.

AUTOMATIC SELECTION

The Synchro Heading, Roll, and Pitch outputs from the Interface RTU are automatically selected by the Interface RTU. Under normal conditions the synchro outputs are derived from the NATO SINS, but if the NATO SINS were to malfunction the outputs would automatically be derived from the Secondary Compass. The selection of the NATO SINS or Secondary Heading, Roll, and Pitch can also be made through the front panel. In this case, the Front Panel control will override the other selection processes. The Front Panel selection is basically used for maintenance purposes.

TIME

The Interface RTU accepts and retransmits to the NATO SINS the highly accurate 1 PPS pulse from the NAVSTAR GPS. In the event of a GPS malfunction, the RTU generates automatically the 1 PPS pulse for the NATO SINS. The RTU also generates from the GPS 1 PPS pulse a highly accurate time of day for distribution to the ship's navigation equipment.

DIAGNOSTIC AND SYSTEM ALARMS

Every P.C. card, with the exception of the display card, contains Built-In-Test (BIT). The BIT generates a signal which activates a Hardware Alarm light on the front panel and on the P.C. card itself. A faulty P.C. card can be easily isolated by this indicator light. Each dc power supply voltage is monitored by a window comparator circuit which will cause an alarm indicator to light if the voltage exceeds its upper or lower tolerance.

A Diagnostic Computer contained within the RTU monitors the system for software problems, such as parity errors or interface time outs. The Diagnostic Computer contains a Data Entry Keyboard with both a decimal and binary display to facilitate software troubleshooting and to allow the display of internal data. A software problem activates a Software Alarm Light located on the front panel.

The front panel also contains alarm lights for SINS Alert, SINS Alarm, and SINS power. All alarms activate contact closure outputs to permit remote monitoring.

RELIABILITY AND MAINTAINABILITY

The system utilizes low power Schottky and CMOS components in its design for reduced power consumption and heat dissipation.

Since each P.C. card contains an on-line test circuit with a fault indicator and can be removed and replaced with system power ON, maintenance of the RTU is extremely simplistic. The MTTR is less than 20 minutes. The system also contains a Diagnostic Computer, which monitors and displays status and software errors. The errors are logged, coded, time tagged, and are made available for print-out or display. Special functions can be entered through the front panel keyboard, and diagnostic programs can be entered in an RS232 format.

Additional merits of the system include front panel test/control switches and a master panel fault indicator for the P.C. cards and power supply. A high degree of commonality, to permit interchangeability, improves maintainability of the system.

MECHANICAL CONFIGURATION

The RTU is contained in a rugged, drip-proof aluminum welded cabinet, with dimensions of 48" (1220mm) high x 24.5" (622mm) deep x 24" (609mm) wide. For additional efficiency, the cabinet contains a closed Air Circulation system.

The RTU is designed to meet MIL-STD-901, Type A, grade A Shock and MIL-STD-167-1 Type 1 Vibration requirements.

FLEXIBILITY

The building block design concept used in the Model 6489 allows maximum flexibility for system configuration and reconfiguration, according to requirements. New system requirements, necessitated by new equipment or new users, can easily be accommodated by adding new field proven, Eurocard format, building blocks. Thus, while ship's systems upgrades will entail wholesale changes throughout the ship, the RTU will only require a few changed or additional cards. The signal control function of the RTU is accomplished using microprocessor PROMs and Programmable Array Logic (PAL) cards. This firmware implementation of signal control allows system level changes in function to be accomplished through simple replacement of newly programmed PROM's and PAL's into sockets. Extensive hardware changes are no longer necessary for system control modifications.

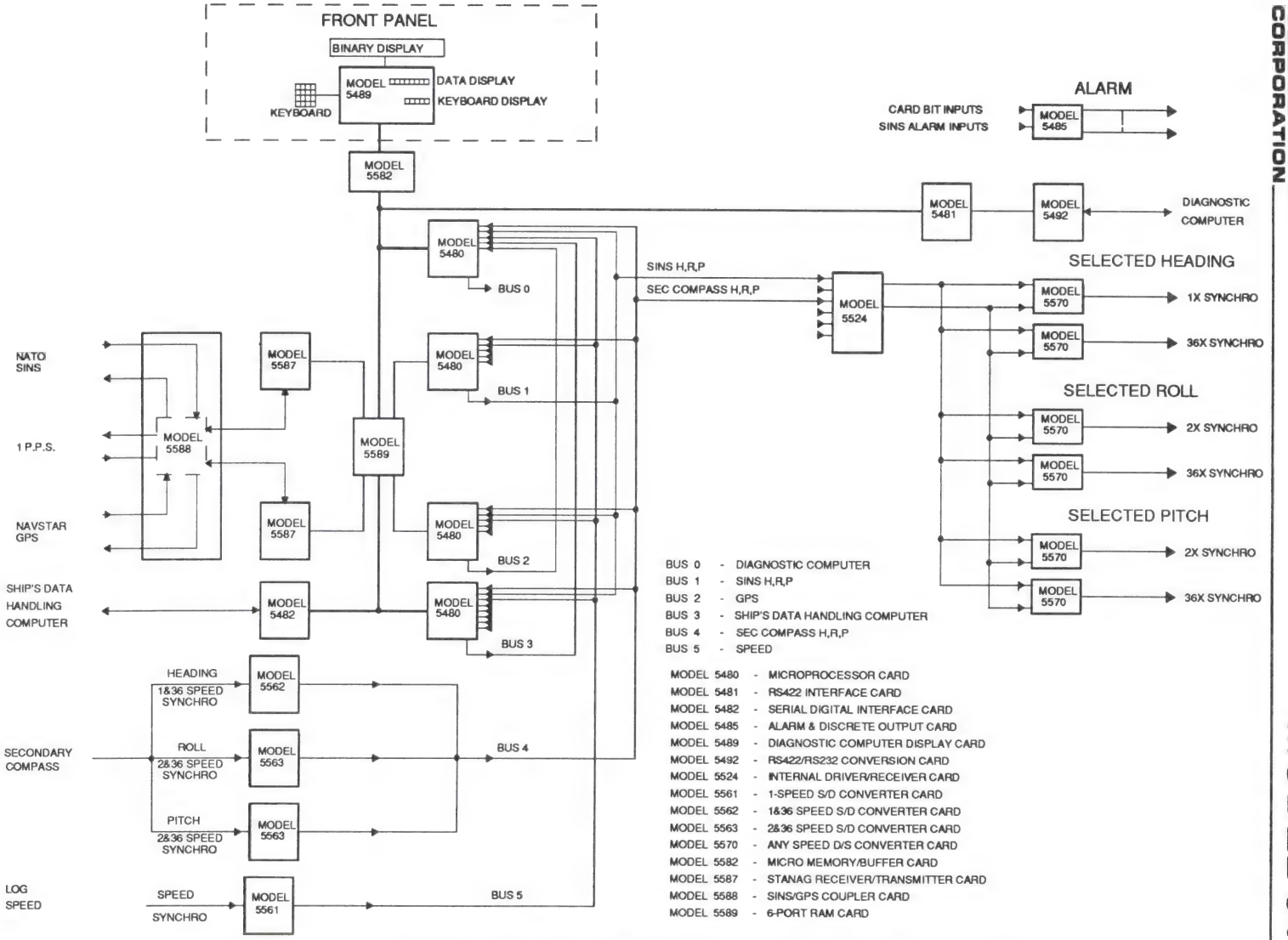


FIGURE 2. SINS/GPS INTERFACE RTU BLOCK DIAGRAM.

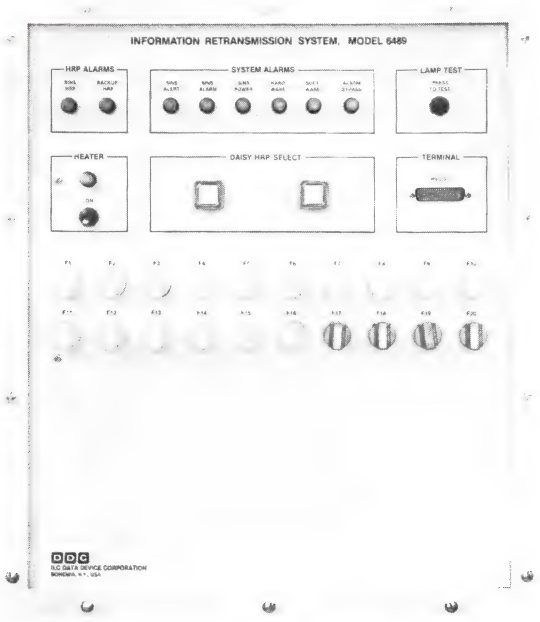


FIGURE 3. EXTERIOR CONTROL PANEL.

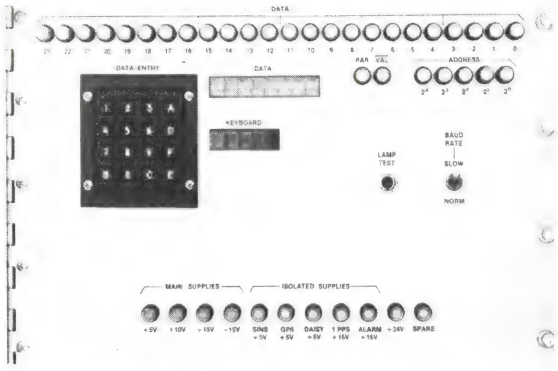


FIGURE 4. INTERIOR CONTROL PANEL.

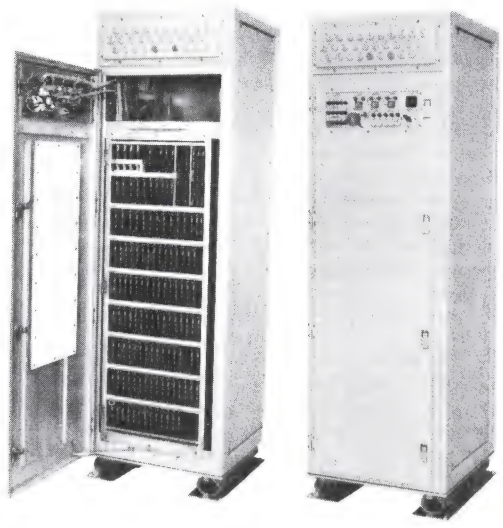
ORDERING INFORMATION:
MODEL 6489

A

DDC
ILC DATA DEVICE CORPORATION

MODEL 6514

RETRANSMISSION UNIT



FEATURES

- *AUTOMATIC SELECTION OF PRIMARY OR SECONDARY INPUT*
- *RELIABLE SOLID STATE DESIGN*
- *MEETS MIL STANDARDS*
- *LED BIT FAULT INDICATION FOR SIMPLE DIAGNOSTICS AT CARD LEVEL*
- *EURO-CARD FORMAT*
- *FLEXIBILITY THROUGH USE OF FIELD PROVEN BUILDING BLOCKS*
- *ALL INPUTS AND OUTPUTS GALVANICALLY ISOLATED*

DESCRIPTION

The Model 6514 retransmission unit (RTU) is designed for surface ships to provide power boost as well as ratio transformations of the ship's navigation and attitude synchro information. The system distributes this data in synchro, resolver, or DC format as required by the applicable loads. This solid state shipboard retransmission system is an ideal replacement for systems using synchro signal amplifiers or multispeed repeaters that are implemented with electromechanical equipment. Flexible in design, the retransmission system provides over 100 outputs, with the option of easily reprogramming speed ratios via the connector wiring of output cards. ILC Data Device Corporation provides full documentation, field servicing, maintenance and logistic support for the Model 6514.

TECHNICAL INFORMATION

INTRODUCTION

The Model 6514 Synchro Retransmission Unit (RTU) consists of RTU subassemblies housed in a hinged, removable card cage subassembly. The card cage is in a shock mounted vibration, EMI, and drip proof welded aluminum cabinet. The Model 6514 receives ship's motion data (heading, pitch, roll, distance and speed) from both the primary and secondary ship's navigational equipment (a MK29 Stabilized Gyro Compass and an SRD-331M Speed Log) in synchro format, converts it to digital form, then reformats the data to accommodate the many speed ratios and power levels required by the shipboard loads. Depending on the many loads to be driven, the RTU supplies data in a wide variety of forms: in identical synchro format, in synchro format with modified speed ratio, in resolver format, or in various scale factored analog formats. Multiple power levels are supplied, as required. Data accuracy is maintained regardless of format.

INPUTS

The inputs which the Model 6514 accepts are in synchro or pulse format. Synchro inputs are from two Gyro Compasses (Heading, Roll and Pitch), Log (Waterspeed) and Simulator Inputs. Log (Distance) is in pulse/nautical mile format. The modular building block approach allows easy adaptability to any required inputs.

OUTPUTS

The Model 6514 RTU has over 100 outputs. These outputs drive the ship's navigation control system, fire control system, anti-roll system, radar system, sonar system, plotting table and signal repeaters. Outputs include status contacts, distance contacts and synchro information for Heading, Roll, Pitch and Speed. The power and flexibility of the RTU allows all navigation data to be collected and processed in a central location for distribution throughout the ship in a consistent, reliable solid state system. Each of the more than 100 outputs is galvanically isolated to prevent single failures from becoming catastrophic to the entire navigation system.

REMOTE OPERATION

The RTU has a remote switch panel to allow operation from remote sites, such as the bridge. The panel contains two switch/indicator assemblies and six indicators. When operating under remote control, selection of operating mode and Primary or Secondary compass source is transferred to this panel. During such operation, the select switches on the main control panel are disabled but the main panel indicators follow those on the remote panel. (During main control panel operation, the remote panel indicators follow those on the main panel and the remote select switches are disabled.)

M

SIMULATION

A simulation input connector is provided on the front panel. The purpose of this input is to permit synchro, validity and distance information to be fed into the system for troubleshooting or training purposes. The simulation input accepts information in the same format as that provided by the Gyro Compass and Log for the ship.

SYSTEM ALARMS

Every P.C. card contains BIT. The BIT circuit generates a signal which activates the alarm lights located on the front face of each PC card, just behind the cabinet door. The fault indication is transmitted to the front panel for additional system safeguard.

RELIABILITY AND MAINTAINABILITY

The all solid state RTU has been designed to meet stringent military specifications. The use of forward located fault indicator lights tripped by internal BIT, as stated above, makes maintenance of the RTU extremely simplistic. Faulty PC cards are removed and replaced when a fault is indicated. The system utilizes low power Schottky and CMOS components in its design for reduced power consumption and heat dissipation.

FLEXIBILITY

The building block design concept used in the Model 6514 allows maximum flexibility for system configuration and reconfiguration, according to requirements. New system requirements, necessitated by new equipment or new users, can easily be accommodated by adding new field proven, Eurocard format building blocks. Thus, while ship's systems upgrades will entail wholesale changes throughout the ship, the RTU will only require a few changed cards. The signal control function of the RTU is accomplished using Programmable Array Logic (PAL) cards. This software implementation of signal control allows system level changes in function to be accomplished through simple replacement of newly programmed PAL's into sockets. Extensive hardware changes are no longer necessary for system control modifications.

MECHANICAL CONFIGURATION

The RTU is contained in a rugged, drip-proof aluminum welded cabinet with dimensions of 78″ (2.0m) high x 22″ (0.56m) deep x 24″ (0.61m) wide. For additional efficiency, the cabinet contains a closed Air Circulation system. The RTU is designed to meet MIL-STD-901, type A, grade A shock and MIL-STD-167-1, type 1 vibration requirements.

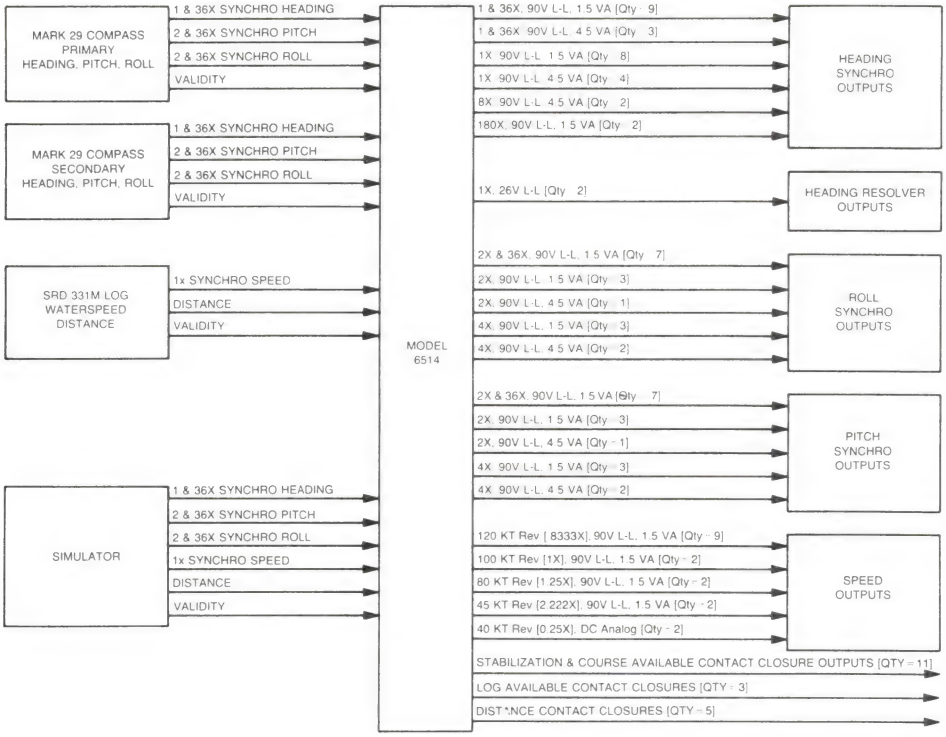
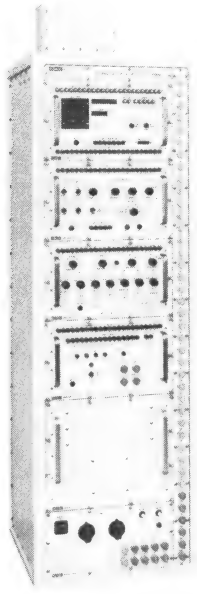

MARK 29 COMPASS PRIMARY HEADING, PITCH, ROLL
1 & 36X SYNCHRO HEADING
2 & 36X SYNCHRO PITCH
2 & 36X SYNCHRO ROLL
VALIDITY
MARK 29 COMPASS SECONDARY HEADING, PITCH, ROLL
1 & 36X SYNCHRO HEADING
2 & 36X SYNCHRO PITCH
2 & 36X SYNCHRO ROLL
VALIDITY
SRD 331M LOG WATERSPEED DISTANCE
1x SYNCHRO SPEED
DISTANCE
VALIDITY
SIMULATOR
1 & 36X SYNCHRO HEADING
2 & 36X SYNCHRO PITCH
2 & 36X SYNCHRO ROLL
1x SYNCHRO SPEED
DISTANCE
VALIDITY
MODEL 6514
1 & 36X, 90V L-L, 1.5 VA [Qty - 9]
1 & 36X, 90V L-L, 4.5 VA [Qty - 3]
1X, 90V L-L, 1.5 VA [Qty - 8]
1X, 90V L-L, 4.5 VA [Qty - 4]
8X, 90V L-L, 4.5 VA [Qty - 2]
180X, 90V L-L, 1.5 VA [Qty - 2]
HEADING SYNCHRO OUTPUTS
1X, 26V L-L [Qty - 2]
HEADING RESOLVER OUTPUTS
2X & 36X, 90V L-L, 1.5 VA [Qty - 7]
2X, 90V L-L, 1.5 VA [Qty - 3]
2X, 90V L-L, 4.5 VA [Qty - 1]
4X, 90V L-L, 1.5 VA [Qty - 3]
4X, 90V L-L, 4.5 VA [Qty - 2]
ROLL SYNCHRO OUTPUTS
2X & 36X, 90V L-L, 1.5 VA [Qty - 7]
2X, 90V L-L, 1.5 VA [Qty - 3]
2X, 90V L-L, 4.5 VA [Qty - 1]
4X, 90V L-L, 1.5 VA [Qty - 3]
4X, 90V L-L, 4.5 VA [Qty - 2]
PITCH SYNCHRO OUTPUTS
120 KT Rev [.8333X], 90V L-L, 1.5 VA [Qty - 9]
100 KT Rev [1X], 90V L-L, 1.5 VA [Qty - 2]
80 KT Rev [1.25X], 90V L-L, 1.5 VA [Qty - 2]
45 KT Rev [2.222X], 90V L-L, 1.5 VA [Qty - 2]
40 KT Rev [0.25X], DC Analog [Qty - 2]
SPEED OUTPUTS
STABILIZATION & COURSE AVAILABLE CONTACT CLOSURE OUTPUTS [QTY - 11]
LOG AVAILABLE CONTACT CLOSURES [QTY - 3]
DISTANCE CONTACT CLOSURES [QTY - 5]

FIGURE 1. RTU BLOCK DIAGRAM

DDC
ILC DATA DEVICE CORPORATION

MODEL 6480

SOLID STATE INFORMATION RETRANSMISSION SYSTEM



FEATURES

- *RELIABLE SOLID STATE DESIGN*
- *MICROPROCESSOR BASED*
- *MEETS MIL STANDARDS*
- *CONTAINS DIAGNOSTIC COMPUTER & COMPLETE BITE*
- *ACTIVE REDUNDANCY OF CRITICAL DATA*
- *EURO-CARD FORMAT*

DESCRIPTION

The Model 6480 Information Retransmission System (IRS) is a microprocessor based information management system. It features active redundancy of critical channels and provides Primary, Secondary and In Port Keep Alive Power. Model 6480 is a smart interface cabinet which processes and formats synchro, frequency and digital information. It integrates the ship's compasses, depth transducers, fire control computer, auto-pilot computer and platform computer (Figure 1). In addition, it supplies digital and synchro information for various displays. One of the unique features of the Model 6480 IRS is its flexibility to have its output data format changed by a simple replacement of a P.C. board. ILC Data Device Corporation provides full documentation, field servicing, maintenance and logistic support for the Model 6480. The P.C. cards contained in the IRS have been assigned NATO stock numbers.

TECHNICAL INFORMATION

INTRODUCTION

The Model 6480 Information Retransmission System (IRS) consists of five drawers and one panel enclosed in a welded aluminum cabinet. Of the five drawers, four drawers contain 74 printed circuit cards (Euro-Card format) and one drawer contains four power supplies which consist of Primary/Secondary Main Power and Primary/Secondary Keep Alive Power. The four signal processing/information management drawers can basically be classified into the following categories: Synchro-to-Digital, Digital-to-Synchro, Frequency-to-Digital/Parallel-to-Serial and Computer Interface.

INPUTS

The inputs which the Model 6480 accepts are in synchro, frequency and digital formats. Synchro inputs are from the Sperry Mark 29 Compass (Heading, Roll and Pitch), Sagem CGM-4 Compass (Heading), Kollmorgen Periscope (Roll, Pitch), Pendulum (Pitch) and E-M Log (Speed). Frequency inputs consist of Propeller Axis Revolutions and Depth Transducer data. Parallel Digital inputs include Echo Sounder (Depth Under Keel) and Status (Sperry and Sagem compasses).

INPUTS AND OUTPUTS

The digital communication between the Model 6480 and the shipboard computers is conducted in a serial bus format. Present design includes 3 specified formats of 1MHz ICI, RS422 and RS232. Additional formats such as Stanag 4156, 1553, etc. can easily be implemented by the exchange of one P.C. card. The serial interface is conducted with the following shipboard control units: GIPSY Computer (Weapons Control), Auto-Pilot Computer (Navigation), Platform Computer (Submarine Controls and Pumps), Mark 29 Computer (Vertical Acceleration and Satellite Navigation Information) and Portable Bridge Control Unit (Manual Piloting).

OUTPUTS

The outputs from the Model 6480 are used for displays and repeaters. Outputs include the Numerical Indicator (precision time, date and processed information) and synchro information for Heading, Speed, Pitch and Depth Repeaters.

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SYSTEM CONVERSIONS AND FUNCTIONS

- Generates Master Time and Date for Ship
  - GMT, Local, Delta
  - Accurate to greater than 1 ppm
- Converts Depth Transducer Frequency to a filtered depth (in meters) and depth rate:
  - Accuracy 3cm, resolution 1.5cm
  - Translated for keel depth
  - Compensated for Roll and Pitch
  - Filtered using vertical acceleration from Mark 29
- Converts Propeller RPM to Speed in Knots
  - Generates speed depending on depth and snorkel position
  - Four speed curves
- Generates rates for critical information
  - Heading, Depth, Pitch, Speed
- Converts:
  - Synchro-to-Digital
  - Digital-to-Synchro (any speed)
  - Digital-to-Analog
  - Binary-to-BCD
  - BCD-to-Binary
  - Parallel-to-Serial
- Generates special Computer Interfaces:
  - ICI: 1MHz serial data bus for Mark 29 and GIPSY Computers
  - RS422: Differential, 19.2K Baud ASCII format for auto-pilot/platform computers, numerical indicator and portable bridge displays
  - RS232: Diagnostic Interface, 19.2K or 300 Baud

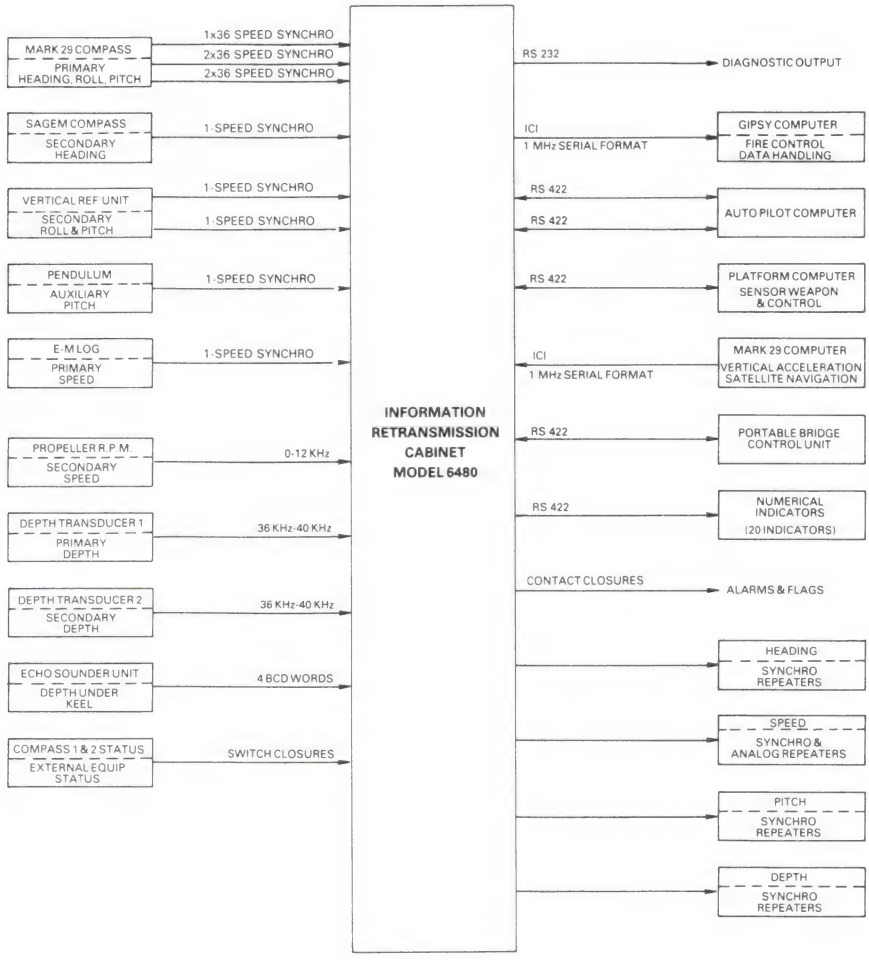


FIGURE 1. IRS BLOCK DIAGRAM

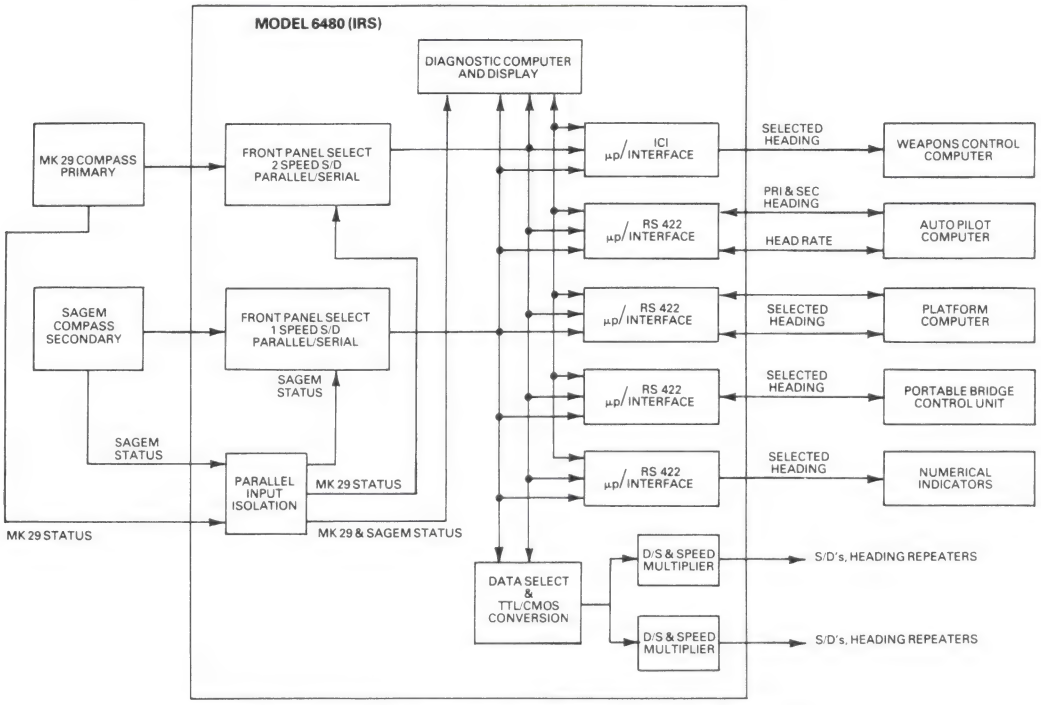


FIGURE 2. FUNCTIONAL DIAGRAM HEADING CHANNEL

CRITICAL CHANNELS

The critical channels are active redundant with automatic selection. They include Heading, Roll, Pitch, Depth, Speed and Time. Figure 2 is a simplified functional diagram of the redundant Heading channel. The actual number of the Internal Serial Bus (ISB) is 17. Each bus is capable of transmitting up to 31 32-bit words (Figure 3). Both the Primary and the Secondary analog inputs are converted into a digital format and distributed by the Primary and Secondary ISB. Each output interface card receives both the primary and secondary inputs. A simplified explanation of the selection of Primary or Secondary Heading is as follows:

A. The Auto-Pilot Computer will normally select the primary or secondary Heading based on the Heading Rate and the Primary and Secondary Heading input it receives. The selected heading will then be distributed to all other channels which require heading data.

B. In the event that the internal Validity bit in the serial word (Figure 3) has been activated due to a "fault", the µP/RS422 interface section of the IRS will select the proper Heading channel.

C. The selection of the Primary or Secondary Heading can also be made through the front panel. In this case, the Front Panel control will override the other selection processes. The Front Panel selection is basically used for maintenance purposes which will force a particular heading (in the test position) onto all the channels.

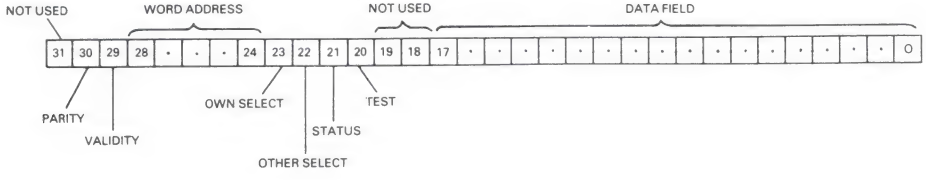

NOT USED
WORD ADDRESS
NOT USED
DATA FIELD
31 30 29 28 · · · 24 23 22 21 20 19 18 17 · · · · · · · · · · · · · · · 0
PARITY
VALIDITY
OWN SELECT
OTHER SELECT
STATUS
TEST

FIGURE 3. DATA WORD FORMAT

DIAGNOSTIC AND SYSTEM ALARMS

Every P.C. card, with the exception of the display cards, contains BITE. The BITE generates a signal which activates the alarm lights located on the D/S drawer (Figure 4). These lights indicate faults in the PRI (Primary), BU (Back-up Secondary), IL (Non-redundant Channel), SW (Software) and TEMP. The fault indication is transmitted to the control room panel for additional system safeguard. The faults which occur in the Primary, Secondary or Non-redundant Channel can be fault-isolated through the indicator lights located on every drawer. Once the proper drawer is pulled out, the problem P.C. card can be located readily by the indicator light located on the individual P.C. card. Software problems can be fault-isolated through the Diagnostic Computer. The Data Entry keyboard located on the Diagnostic Computer and Display drawer facilitates software troubleshooting.

RELIABILITY AND MAINTAINABILITY

The all solid state IRS has been designed to meet stringent military specifications and has a calculated MTBF of 2500 hours. However, because of the active redundant automatic selection system built into the IRS, the mean time between non-operation of the IRS is at least an order of magnitude higher than the MTBF. The system utilizes low power Schottky and CMOS components in its design for reduced power consumption and heat dissipation.

Since each P.C. card contains an on-line test circuit and a fault indicator, the MTTR is only 20 minutes. The system also contains a Diagnostic Computer, which monitors and displays status and software errors. The errors are logged, coded, time tagged and are made available for print-out or display. Special functions can be entered through the front panel keyboard, and diagnostic programs can be entered in an RS232 format.

Additional merits of the system include front panel test/control switches and front panel fault indicators for each P.C. card, power supply and major functional groupings (Primary, Secondary, Non-redundant Channels and Software). A high degree of commonality, to permit interchangeability, improves maintainability of the system.

MECHANICAL CONFIGURATION

The IRS is contained in a rugged, drip-proof aluminum welded cabinet, with dimensions of 67" (1.7m) high x 21.6" (0.55m) deep x 21.6" (0.55m) wide. For additional efficiency, the cabinet contains a closed Air Circulation system. It is designed to meet 20g/100ms shock and MIL-I-983 vibration requirements.

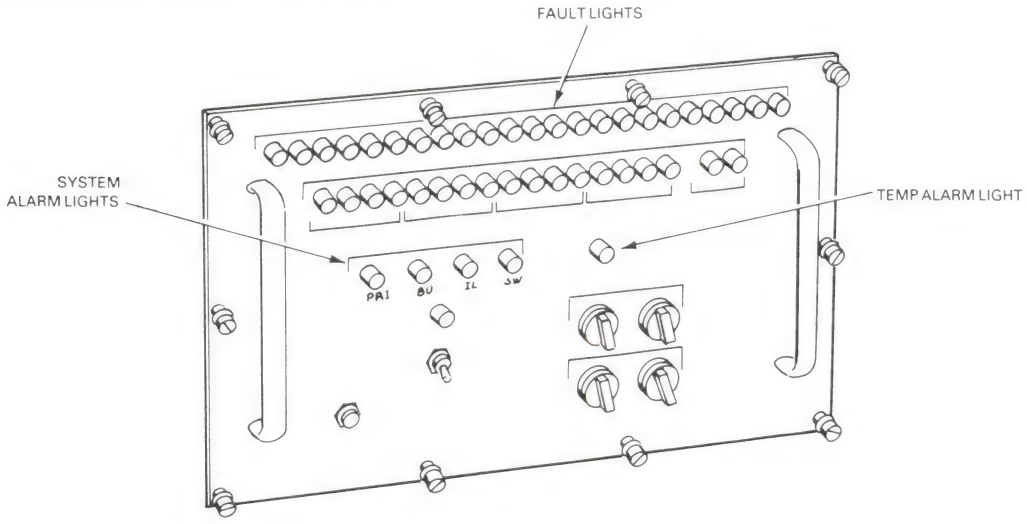


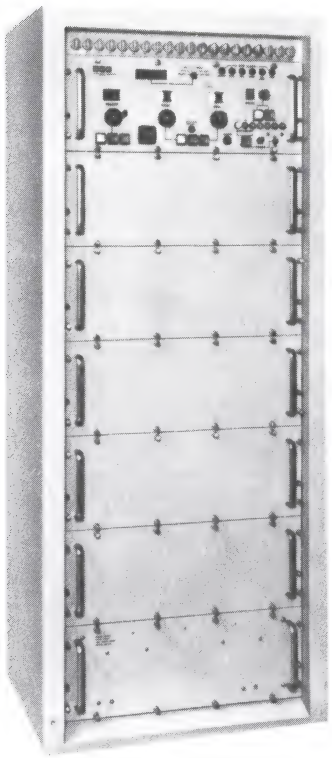
FIGURE 4. D/S DRAWER

A

DDC
ILC DATA DEVICE CORPORATION

MODEL 6322

SOLID STATE SYNCHRO RETRANSMISSION SYSTEM (SRS) (SYNCHRO SIGNAL AMPLIFIER)



MODEL 6322

ILC Data Device Corporation's Model 6322, designed and developed for the Royal Netherlands Navy (RNLN), is now in production. The RNLN's "S" Class Frigate will utilize these systems to consolidate all prime synchro data transformations and distribution. Chosen primarily as the most cost effective solution for the RNLN's requirements, the all-solid state version also provides bonus features of greatly reduced volume and maintenance requirements as well as increased reliability, system dependability and unprecedented flexibility.

As shown in the overall functional block diagram, the solid-state retransmission system provides power boost as well as speed ratio transformations of ship's navigation and attitude synchro information. The system then distributes these data in either synchro, DC or AC format to all other ship's systems requiring these data. These functions had been provided traditionally by bulky and expensive electromechanical servo systems or on a distributed channel-by-channel basis as required. This shipboard data handling system is directly applicable to the U.S. Navy submarine and surface ship requirement for synchro signal amplifiers or multispeed Repeaters which are currently implemented with electromechanical systems. The Synchro Retransmission System (SRS) actually goes beyond basic synchro signal amplifier capabilities by providing the option of retransmitting the data in **any** speed ratio on a channel-by-channel basis.

As presently implemented for the RNLN, the SRS accepts the standard 90V L-L, 400 Hz synchro inputs consisting of single and dual-speed information (1X, 1X/36X and 2X/36X). These data are converted to high resolution digital data for distribution to the various output channel converters. Thereafter, on a channel-by-channel basis, the data may be used to generate single-speed synchro or resolver outputs or any multispeed ratio output or AC or DC linear outputs. The RNLN SRS provides synchro ratios ranging from non-integral (e.g., .3X, .36X, .9X, 3.6X) to any integral ratio (e.g., 8X, 11X, 16X, 32X, 360X). In addition, the outputs can be 50, 60 or 400 Hz. AC and DC outputs are also field programmable to provide various scale factors.

A final example of the SRS's flexibility is the capability to provide synchro outputs which are simply power amplified reproductions of the analog synchro inputs (buffered outputs).

- ALL SOLID-STATE . . . . . Totally replaces existing electromechanical systems and occupies approximately one-third original volume.
- FLEXIBLE . . . . . Digital implementation and modular partioning provide ready adaptability to future requirements. Computer interface easily obtained.
- COST EFFECTIVE . . . . . Lower in initial cost and requires no periodic maintenance for mechanical wear and tear.
- MODULAR . . . . . Only 14 unique printed circuit card assemblies provide all circuit functions. Channel partioning provides quick fault isolation and minimizes down-time.
- BUILT-IN TEST . . . . . B.I.T.E. indicators and alarms on a channel-by-channel basis as well as overall system B.I.T.E.
- FULLY PROTECTED OUTPUTS . . . Short-circuit-proof and overload protected.
- HIGH RELIABILITY . . . . . State-of-the-art thick film hybrid converters.
- DIGITAL IMPLEMENTATION . . . . Enables computer interfacing (serial or parallel) with minor changes to existing design.
- ADVANCED CABINET DESIGN . . . Features closed air circulation cooling.
- EXPANDABLE . . . . . In addition to being field programmable on a channel-by-channel basis, the system features expansion capability to a total of 89 output channels. Power supply capability for a totally expanded system is built-in.

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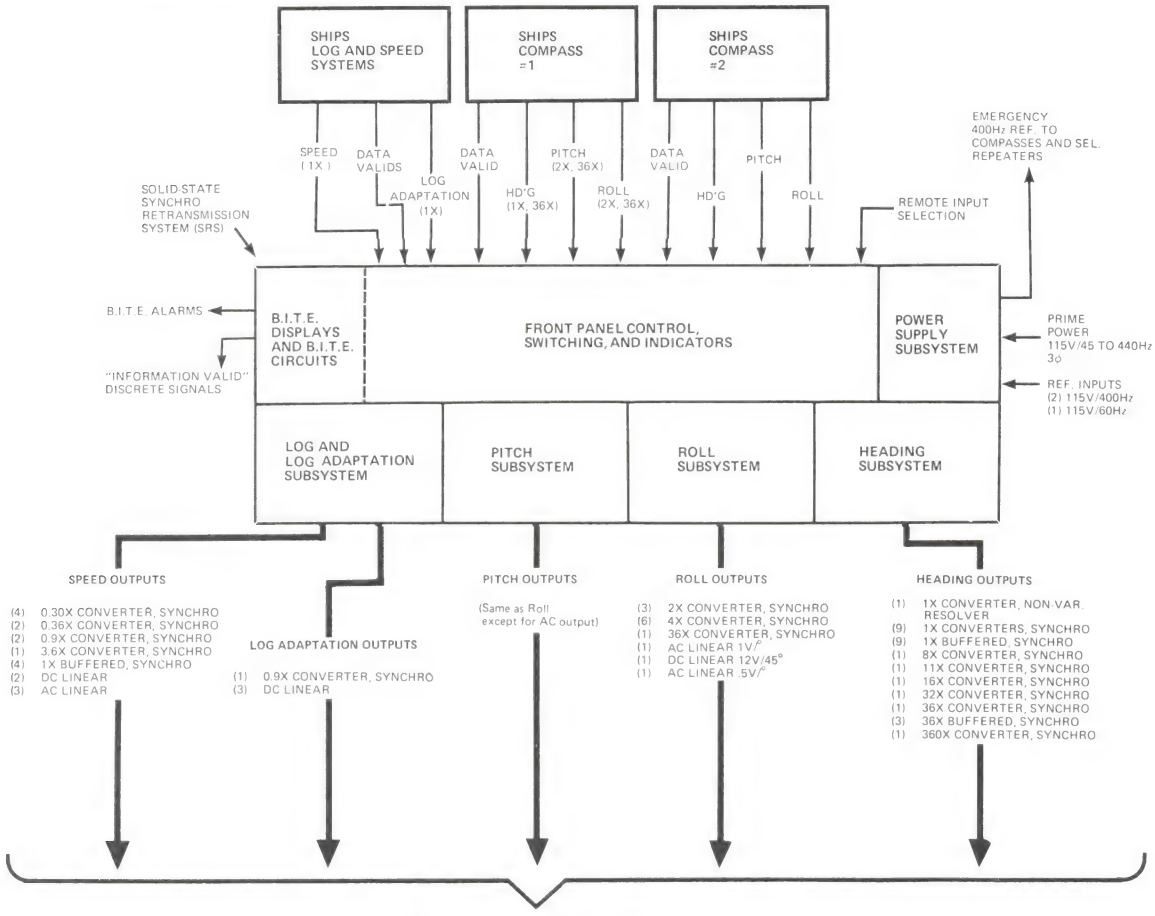
OVERALL FUNCTIONAL BLOCK DIAGRAM
SRS AND SHIP INTERFACES

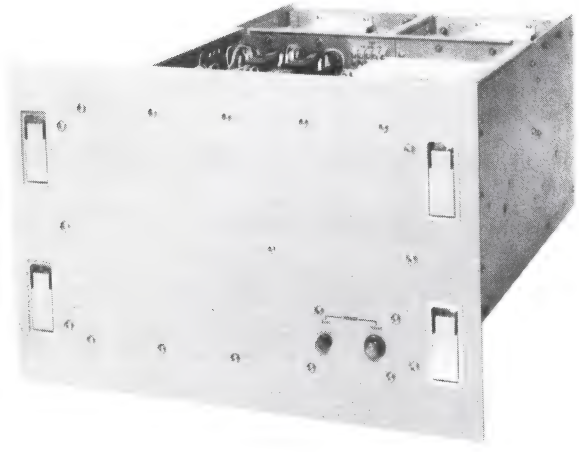


A

DDC
ILC DATA DEVICE CORPORATION

MODEL 6438BR

SEVEN CHANNEL, HI-POWER, DIGITAL/SYNCHRO DRIVE SYSTEM



FEATURES

- *SELF CONTAINED*
- *90V L-L OUTPUT AT 30VA PER CHANNEL*
- *BUILT-IN-TEST CIRCUITS MONITOR TEMPERATURE AND CURRENT*
- *COMPLETELY COMPUTER CONTROLLED*
- *AUTOMATIC OVERLOAD PROTECTION WITH BATTLESHORT EMERGENCY OVERRIDE*

DESCRIPTION

The Model 6438BR is a high power, multi-channel Digital to Synchro converter and drive system. Completely self contained, the Model 6438BR accepts 12 bit differential TTL digital signals and sequentially converts the digital angles to seven channels of 3 wire, 90V L-L synchro output capable of driving torque receiver loads.

The Model 6438BR is operated completely by computer control; only the power supply indicator lights are mounted on the front panel.

Built-In-Test (BIT) circuits in the Model 6438BR include overcurrent and overtemperature monitoring. Battleshort override of an overtemperature condition is selectable with a digital input from the host computer.

The Model 6438BR is constructed with Hi-Rel, military approved parts. The D/S drive systems are currently used to drive 7 torque receivers in 5″ naval guns.

TECHNICAL INFORMATION

INTRODUCTION

The Model 6438BR consists of one, self-contained 20.25 x 23.21 x 13 inch open frame chassis. Designed to be rack mounted, the front panel of the chassis is drip proof and EMI gasketed. Housed within the chassis is a card frame containing 10 circuit cards, seven synchro transformer pairs, seven synchro power buffer assemblies, a 2 pole circuit breaker, a 5V power supply, a ±15V pulsating power supply and two cooling fans.

The Model 6438BR accepts a twelve bit differential TTL input data and sequentially decodes the input to seven channels of high power synchro signals that correspond to the digital input angle. Overtemperature and overcurrent monitoring of the digital to synchro circuits are provided as well as a 45° 'kick' circuit to restart stalled loads on each channel.

Each synchro channel is monitored by a fault monitor card and if a fault is detected, the host system is informed. If the fault lasts longer than one second, kick pulses are generated to free the stalled load. Eventually, if the load is not freed, an overtemperature condition will occur and the D/S channel will shut down. The host system may override an overtemperature shutdown condition with a battleshort command.

All connections to the Model 6438BR (with the exception of chassis ground) are made through four multipin connectors mounted to the rear panel of the chassis. The connectors isolate the AC input, digital input, fault indications and synchro outputs from each other.

INPUTS

The Model 6438BR accepts twelve bit differential TTL data from the host computer in positive logic form. The differential data is converted to single-ended TTL by line receivers located on the

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two Sequencer cards in the card frame. Data bits 1, 2 and 4 through 12 are routed to all seven D/S converter channels. Bit 3 is routed through the Fault Monitor Card to all D/S converters. An externally generated strobe is applied to a line receiver on one Sequencer card to sequence the D/S converter channels. The external strobe will cause the addressed Digital to Synchro converter channel to latch the digital data presented on the internal data bus.

DIGITAL OUTPUTS

The Model 6438BR produces seven differential TTL fault monitoring outputs. Each Digital to Synchro converter channel senses overtemperature and overcurrent conditions and will send the specific fault signal to the host system. An overtemperature condition will cause the D/S channel to shut down, the system may then override the overtemperature condition by issuing a battleshort signal to the Model 6438BR. The Model 6438BR will issue a fault indication for an overcurrent condition, but overcurrent will not cause the D/S channel to shut down.

SYNCHRO OUTPUTS

Each synchro channel consists of a Digital to Synchro converter, a high power buffer and a Synchro to Synchro output transformer. The 115VAC 60Hz input reference signal is fed to a low scale factor variation Digital to Resolver converter where the digital input is converted to +S (sine) and +C (cosine) resolver signals. A triple preamplifier and electronic Scott-T circuit reconfigure

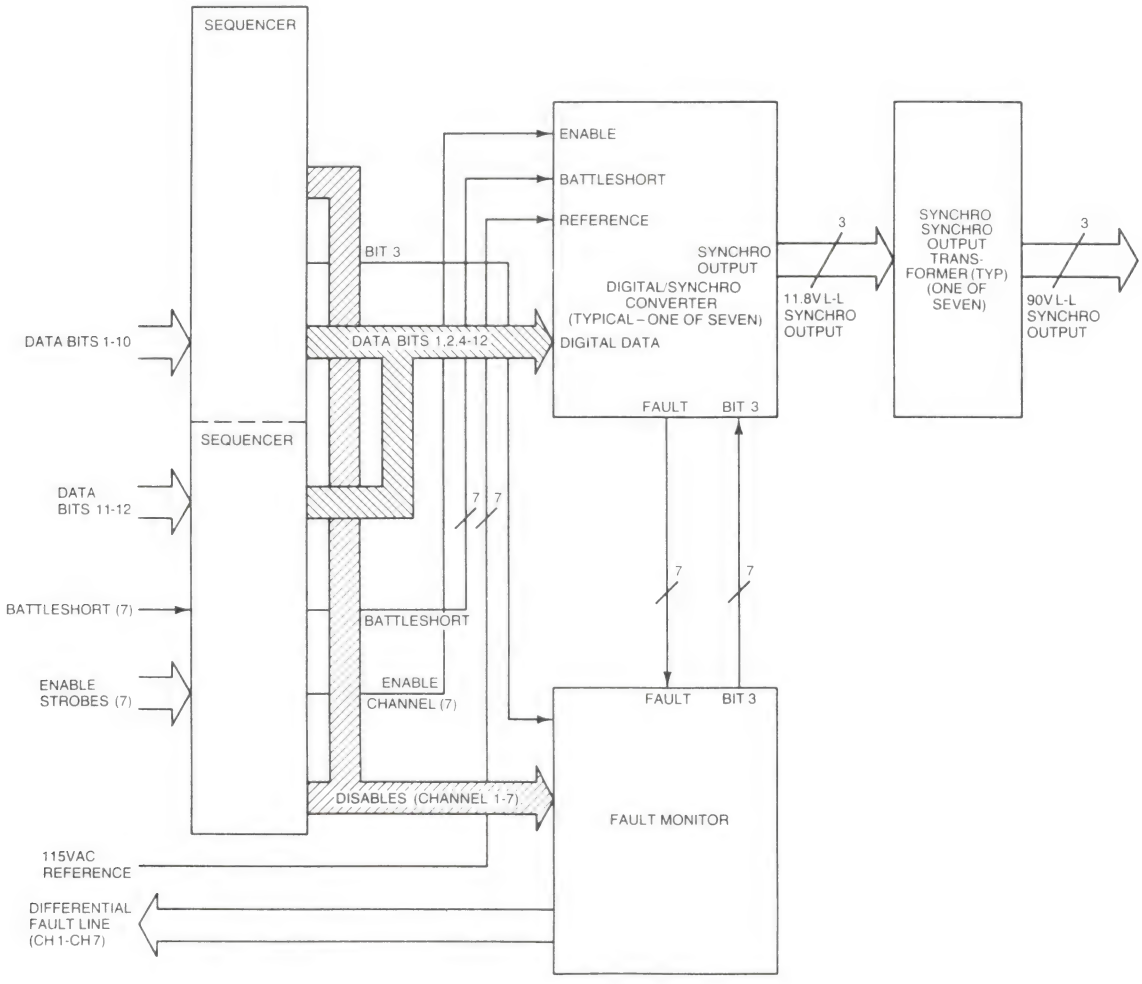

FIGURE 1. SIMPLIFIED BLOCK DIAGRAM

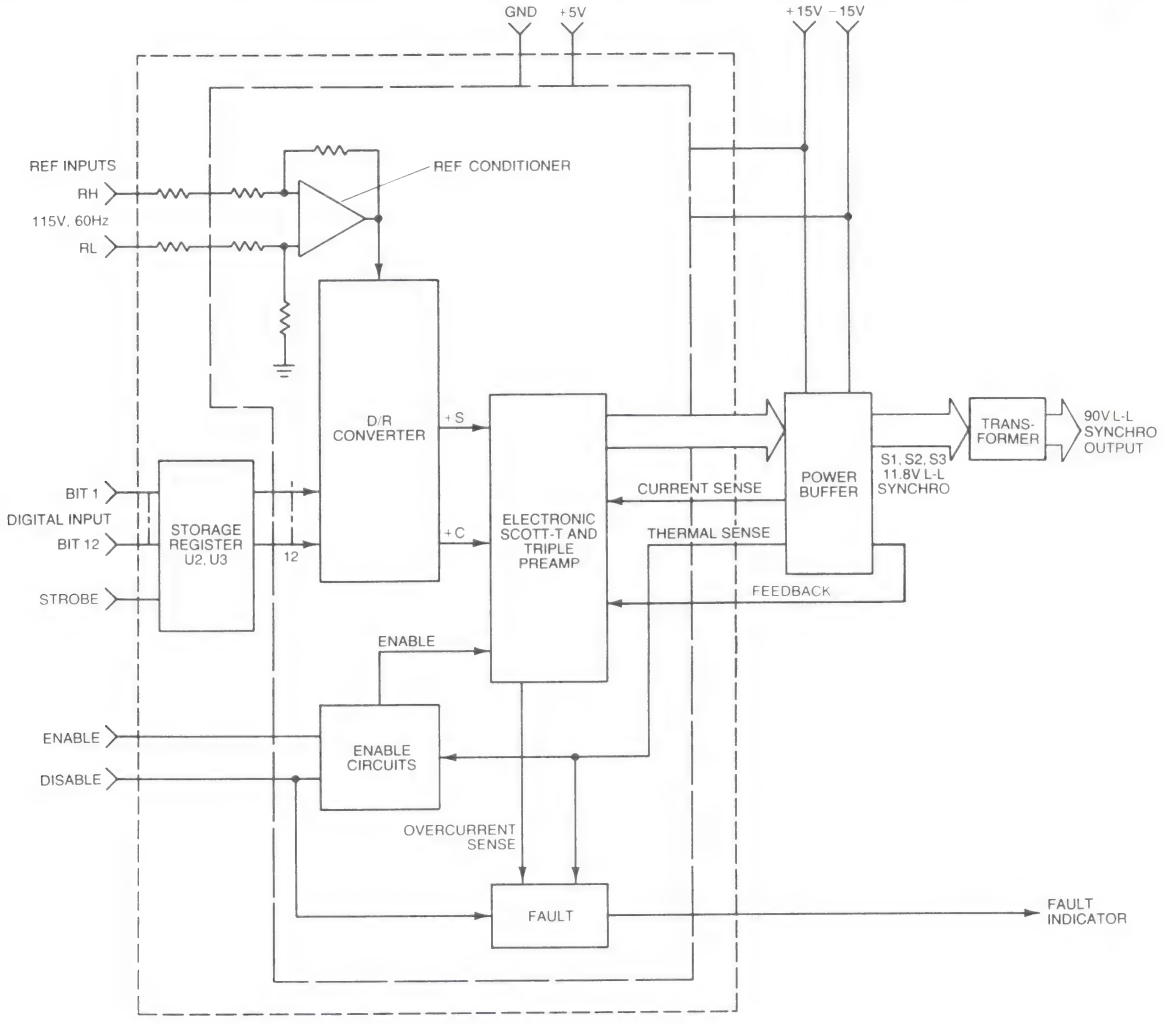

FIGURE 2. DIGITAL/SYNCHRO CONVERTER CHANNEL

the resolver output to a dual ended synchro output corresponding to the digital angle and passes the output to the High Power Buffers (see Figure 2). Each High Power Buffer delivers a three wire 11.8V L-L synchro output to a chassis mounted step-up transformer where it is converted to a 3 wire, 90V L-L synchro output suitable for driving torque receiver loads (at 30VA per channel).

KICK CIRCUIT

Each D/S converter channel includes circuitry for monitoring the current delivered to the load. A stalled synchro load will cause an overcurrent condition in the affected channel. That channel will then send a fault signal to the Fault Monitor card. The Fault Monitor card will send a fault signal to the host system. After a one second delay, the Fault Monitor card will enable a kick circuit based on bit 3. The kick circuit will deliver a string of 45° pulses to free the stalled load. The fault monitor card automatically resets when the load is cleared.

POWER SUPPLIES

The 115VAC input voltage is applied to a +5 Volt power supply module and a ±15 Volt supply through a two pole circuit breaker. The 115VAC input is also applied to each D/S converter channel as the reference source.

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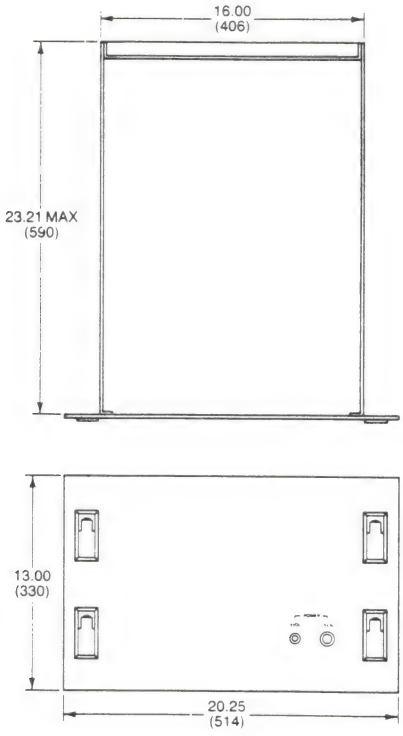
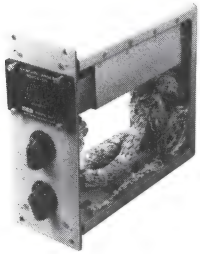
MECHANICAL OUTLINE
Dimensions in inches (millimeters).



ORDERING INFORMATION:
MODEL 6438BR

C



39 CHANNEL SWITCHBOARD SYNCHRO PANEL METER

DESCRIPTION

The DDC-6498 is a 39 channel switchboard synchro panel with removable 4 digit panel meter (DDC-5521). It is packaged in a 9.96 x 3.96 x 9.875 inch aluminum chassis and conforms to MIL-STD-1657 switchboard specifications.

Two front mounted rotary switches provide selection and display of any one of 39 separate synchro and reference inputs. An External Test switch position is provided (Figure 1) for application of user supplied test input signals via a separate connector.

The removable panel meter (DDC-5521) is designed to be reference powered, which eliminates the need for a separate power source. It can be removed from the panel and used as a portable synchro measuring instrument.

The DDC-6498 accepts reference signals of 115V rms at 60Hz or 400Hz and corresponding synchro signals of 90 V rms L-L.

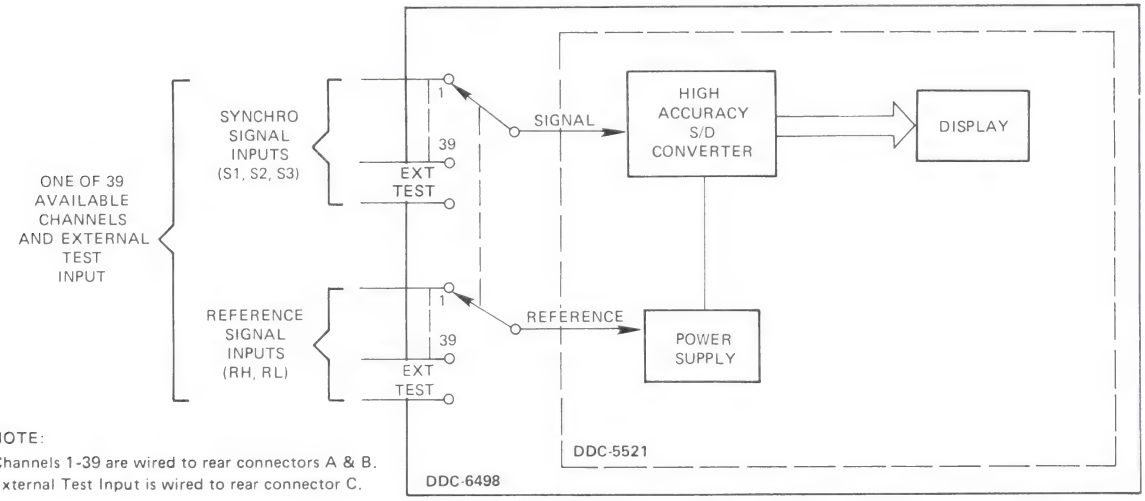
The DDC-5521 provides resolution of 0.1° with an accuracy of 0.2°. Using a type II servo loop for continuous tracking, the DDC-5521 has no velocity lag up to ±180°/sec.

APPLICATIONS

The DDC-6498 allows for monitoring of multi-channel synchro inputs at a single location for test and alignment, system verification checks and trouble shooting as applied to U.S. Navy maintenance procedures. The removable panel meter adds further flexibility to the DDC-6498.

FEATURES

- *US NAVY SWITCHBOARD COMPATIBLE (MIL-STD-1657 PACKAGING)*
- *39 SELECTABLE SYNCHRO AND REFERENCE INPUTS*
- *REMOVABLE METER: STAND-ALONE UNIT, POWERED BY REFERENCE (DDC-5521)*
- *RESOLUTION: 0.1° ACCURACY: 0.2°*
- *OPERATES AT 60 Hz AND 400 Hz*
- *SEPARATE "EXTERNAL TEST" SWITCH POSITION AND CONNECTOR*



NOTE:
Channels 1-39 are wired to rear connectors A & B.
External Test Input is wired to rear connector C.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

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SPECIFICATIONS	
PARAMETER	**VALUE**
RESOLUTION	0.1°
ACCURACY	0.2°
ANGLE RANGE	0° to +359.9°
DISPLAY	
7 Segment 0.43" LED	4 digits
REFERENCE INPUT	
Voltage level	115 V rms, ±10%
Frequency	54 to 440 Hz
Input Impedance	
Single Ended	148 kΩ min
Differential	296 kΩ min
SIGNAL INPUT	
Input Type	Synchro
Voltage (line to Line)	90 V rms ±10%
Frequency	Same as reference
Allowed Phase Shift	±10° max relative to reference
Input Impedance	148 kΩ min (resistive balanced, transformer isolated)
Breakdown Voltage	500 V min to ground
DYNAMIC CHARACTERISTICS	
Tracking Rate	180°/sec min
Settling Time for 179° Step (to ±0.2°)	3 sec
TEMPERATURE RANGE	
Operating	0°C to +70°C
Storage	–65°C to +125°C
POWER INPUT	
Power	9 VA max, 6.5 VA typ
PHYSICAL CHARACTERISTICS	
Size	
DDC-6498 (Including DDC-5521)	9.96 x 3.96 x 9.875 inch (253 x 101 x 251 mm)
DDC-5521 (Stand-alone meter)	2.81 x 3.90 x 7.59 inch (71 x 99 x 193 mm)

TECHNICAL INFORMATION

Signal and reference inputs are selected simultaneously via the front panel switches. Switch S1 selects inputs "off" and 1 through 22 (from rear connector A) and "transfer", which allows switch S2 to select inputs 23 through 39 (from rear connector B) and "external test" (from rear connector C).

REMOTE CABLE

Figure 2 illustrates the connection scheme for the remote signal and reference input cable supplied for use with the DDC-5521, when removed from the switchboard panel.

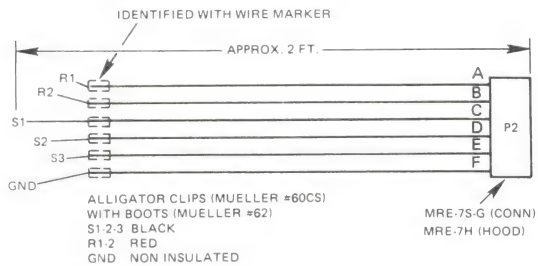


FIGURE 2. DDC-5521 REMOTE CABLE DIAGRAM

DDC-6498 WIRING LIST

SWITCH POSITION	SWITCH DECK 1 (RH)	SWITCH DECK 2 (RL)	SWITCH DECK 3 (S1)	SWITCH DECK 4 (S2)	SWITCH DECK 5 (S3)	
S1-C*	A	B	C	D	E	METER CONNECTOR P1
S1-1	N.C.	N.C.	N.C.	N.C.	N.C.	OFF
S1-2	70	71	72	73	62	REAR CONNECTOR A
S1-3	61	60	50	51	52	
S1-4	42	41	40	28	29	
S1-5	30	31	32	33	34	
S1-6	35	36	46	45	44	
S1-7	43	53	54	55	56	
S1-8	66	65	64	63	74	
S1-9	75	76	77	78	91	
S1-10	90	89	88	87	86	
S1-11	85	84	83	82	81	
S1-12	69	59	49	39	27	
S1-13	14	15	16	17	18	
S1-14	19	20	21	22	23	
S1-15	24	25	12	11	10	
S1-16	9	8	7	6	5	
S1-17	4	3	2	1	13	
S1-18	26	38	48	58	68	
S1-19	80	93	94	95	96	
S1-20	97	98	99	100	101	REAR CONNECTOR A
S1-21	70	71	72	73	62	REAR CONNECTOR B
S1-22	61	60	50	51	52	REAR CONNECTOR B
S1-23	42	41	40	28	29	REAR CONNECTOR B
S1-24	S2-C	S2-C	S2-C	S2-C	S2-C	TRANSFER POSITION

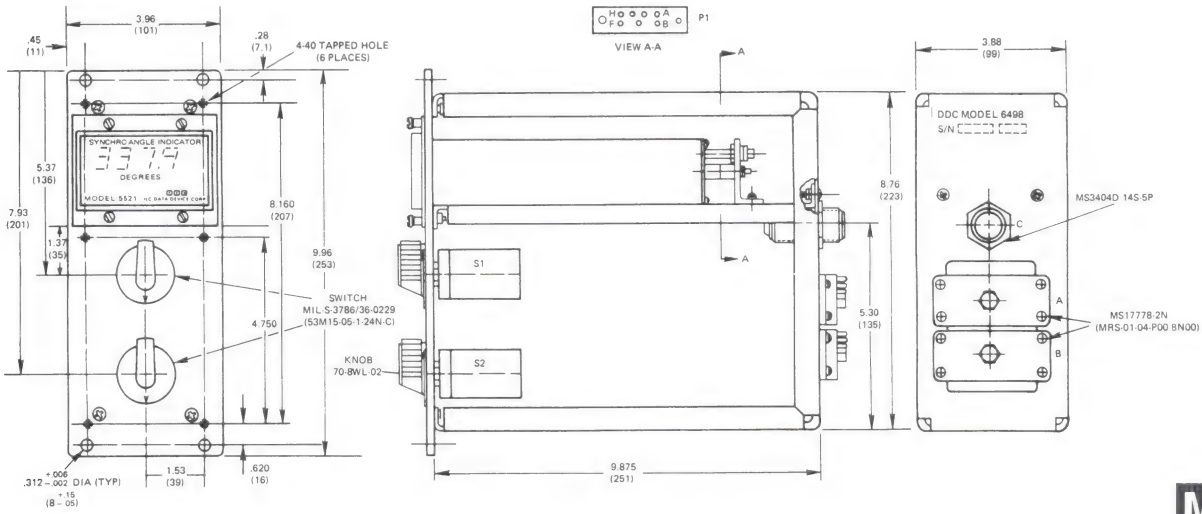
*Internal connection not a switch position

DDC-6498 WIRING LIST (CONT.)

SWITCH POSITION	SWITCH DECK 1 (RH)	SWITCH DECK 2 (RL)	SWITCH DECK 3 (S1)	SWITCH DECK 4 (S2)	SWITCH DECK 5 (S3)	
S2-C*	S1-24	S1-24	S1-24	S1-24	S1-24	TRANSFER POSITION
S2-1	30	31	32	33	34	REAR CONNECTOR B
S2-2	35	36	46	45	44	
S2-3	43	53	54	55	56	
S2-4	66	65	64	63	74	
S2-5	75	76	77	78	91	
S2-6	90	89	88	87	86	
S2-7	85	84	83	82	81	
S2-8	69	59	49	39	27	
S2-9	14	15	16	17	18	
S2-10	19	20	21	22	23	
S2-11	24	25	12	11	10	
S2-12	9	8	7	6	5	
S2-13	4	3	2	1	13	
S2-14	26	38	48	58	68	
S2-15	80	93	94	95	96	
S2-16	97	98	99	100	101	
S2-17	102	103	104	92	79	REAR CONNECTOR B
S2-18	NC	NC	NC	NC	NC	OFF
S2-19	NC	NC	NC	NC	NC	OFF
S2-20	NC	NC	NC	NC	NC	OFF
S2-21	NC	NC	NC	NC	NC	OFF
S2-22	NC	NC	NC	NC	NC	OFF
S2-23	NC	NC	NC	NC	NC	OFF
S2-24	A	B	C	D	E	REAR CONNECTOR C

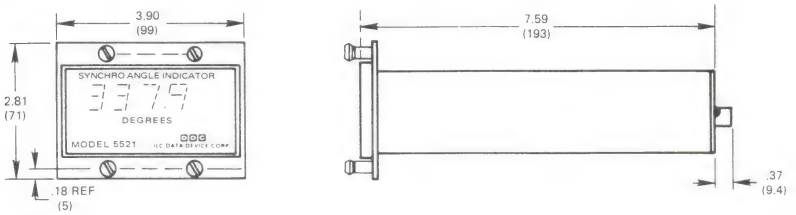
*Internal connection not a switch position

MECHANICAL OUTLINE (DDC-6498)

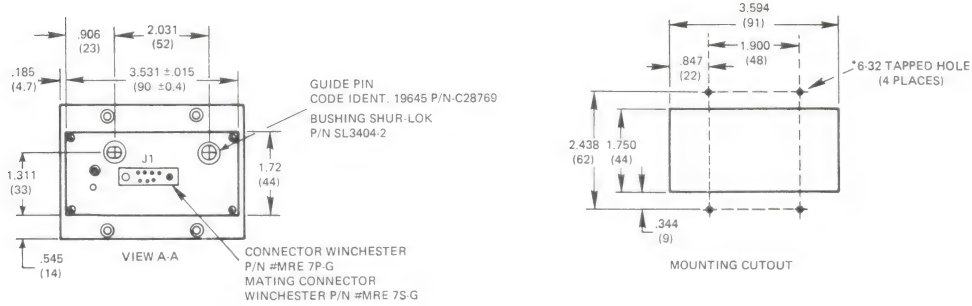


NOTES:
1. Mating connectors are not supplied.
2. Front panel plastic identification plate is not supplied.
3. All wiring is AWG22.
4. Dimensions are in inches (millimeters)

MECHANICAL OUTLINE (5521)



TERMINATION LIST	
CONNECTOR PIN	DESIGNATION
J1-A	RH
J1-B	RL
J1-C	S1
J1-D	S2
J1-E	S3
J1-F	GND
J1-H	N/C



NOTE: Dimensions are in inches (millimeters).

ORDERING INFORMATION

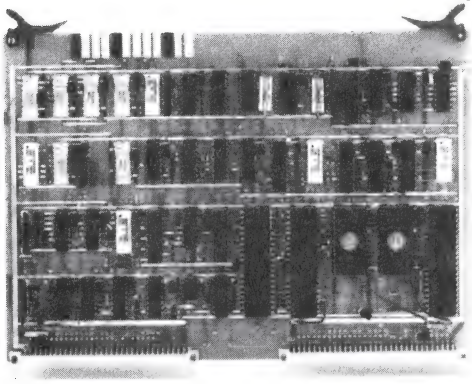
ORDER:

DDC-6498 (Switchboard panel and meter)

DDC-5521 (Synchro meter only)

B

BUILDING-BLOCK P.C. CARDS For Synchro Retransmission System (SRS) Information Retransmission System (IRS) And Custom Systems Requirements



FEATURES

- *EURO-CARD FORMAT*
- *PROVEN DESIGN*
- *INCLUDES ON-LINE BITE*
- *INCLUDES FAULT LIGHT*
- *MEETS MILITARY STANDARDS*

DESCRIPTION

The DDC S-Series P.C. cards are useable for the DDC Model 6322 Synchro Retransmission System (SRS) and DDC Model 6480 Information Retransmission System (IRS). In addition, since the P.C. cards have been designed as functional segments, a building-block concept can be utilized to create a new system based on special customer requirements. A variety of functions which are available (Figure 1) range from synchro-to-digital (S/D) converters for pitch, roll and heading calculations to interface cards for communication with shipboard equipment, such as Auto-Pilot Computer, Weapons Control Computer and Portable Bridge Control Units. All S-Series P.C. cards are in either single or double Euro-card format.

PART NUMBER	DESCRIPTION	SIZE (EURO-CARD)	APPLICATION
3700	1x/Coarse Speed S/D Converter Card	Single	IRS, SRS
3701	36x/Fine Speed S/D Converter Card	Single	IRS, SRS
3702	Low/Medium Power D/S Card	Single	IRS, SRS
3703	Low/Medium Power Synchro Buffer Card	Single	IRS, SRS
3704	High Power Synchro Buffer Card	Single	— SRS
3706	Digital-To-DC Multiplying Converter Card	Single	IRS, SRS
3707	Digital-To-AC Multiplying Converter Card	Single	— SRS
3717	Turn-On Sequence Control Card	Single	— SRS
5480	Microprocessor Card	Double	IRS, —
5481	RS422 Interface Card	Double	IRS, —
5482	ICI Interface Card	Double	IRS, —
5483	Propeller Axis Interface Input Card	Single	IRS, —
5484	Frequency-To-Digital Converter Card	Single	IRS, —
5486	Clock Generator Card	Single	IRS, —
5487	Parallel-To-Serial Converter Card	Double	IRS, —
5489	Decimal/Hexadecimal Display Card	Double	IRS, —
5490	Parallel Input Isolation Card	Double	IRS, —

FIGURE 1. TABLE OF BUILDING-BLOCK P.C. CARDS

INTRODUCTION

The concept of building-block P.C. cards was developed for the design of the Synchro Retransmission System (SRS) and the Information Retransmission System (IRS). Both systems include several common functional blocks.

The Model 6322 SRS is an all solid-state system designed to consolidate all prime synchro data transformations and distribution. It provides power boost as well as line-to-line frequency transformation and speed ratio transformations of ship's navigation and attitude synchro information. The system distributes the data it receives in synchro, DC or AC format to all other ship's systems requiring that data. Typical inputs of Pitch, Roll and Heading are distributed to systems such as Weapons Control, Auto-Pilot, Sonar and Remote Displays.

The Model 6480 IRS is a microprocessor based information management system. Like the SRS, it is of an all solid-state design. However, the IRS is a more powerful state-of-the-art system. In addition to the synchro data transformation performed by the SRS, the IRS features active redundant automatic selection of critical channels such as Pitch, Roll, Heading, Speed and Time. It processes and formats synchro, frequency and digital information, and integrates the ship compasses, depth transducers, Fire Control Computer, Auto-Pilot Computer and Platform Computer. One of the unique features of the IRS is its flexibility to have its output data format changed by a simple replacement of a P.C. card.

BUILDING-BLOCK P.C. CARDS

All cards contain on-line BITE (self test) which has automatic reset capabilities and thus requires no external reset. They also contain an indicator light for easy fault isolation to the card level.

1. MODEL 3700 1x/COARSE SPEED S/D CONVERTER – When configured for single speed conversions the 3700 accepts inputs such as Sagem Compass heading, Kollmorgan Periscope roll and pendulum pitch. The single speed configuration is generally used as a secondary back-up system in a redundant application.

2. MODEL 3701 36x/FINE SPEED S/D CONVERTER – When high resolution synchro conversions are required, both the 3700 and the 3701 cards are used. The high resolution (up to 18 bits) 1 or 2 and 36 speed configuration, is typically used in primary heading, roll and pitch channels.

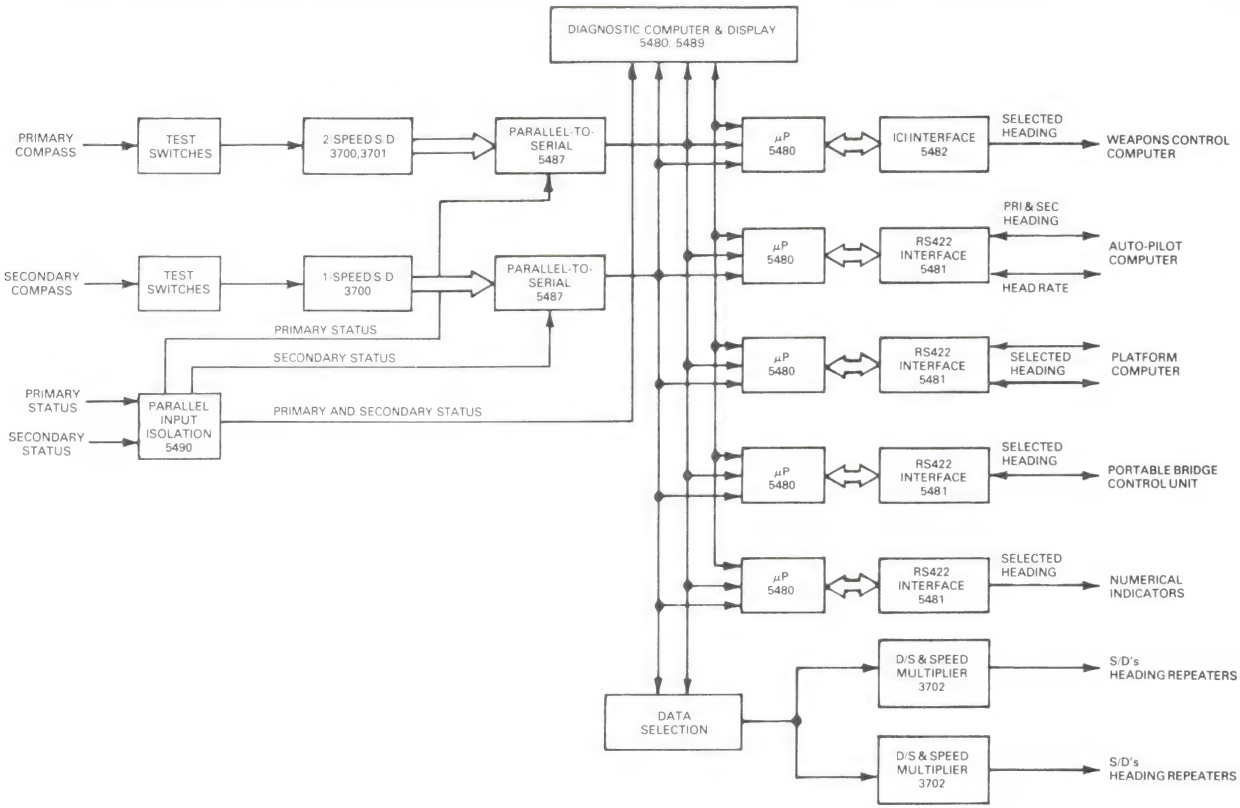


FIGURE 2. TYPICAL ACTIVE-REDUNDANT HEADING CHANNEL (COMBINED FROM BUILDING-BLOCK P.C. CARDS)

3. MODEL 3702 LOW/MEDIUM POWER D/S CONVERTER – This card converts the serial data into a synchro output suitable for driving low or moderate power loads. The connector into which the 3702 is plugged is dedicated to a particular speed ratio, depending on its system application. The associated connector is hard wired for the required speed ratio which may vary from approximately 0.3 to 360.

4. MODEL 3703 LOW/MEDIUM POWER BUFFER – The 3703 consists of a 3-channel synchro power buffer. It also contains BITE circuits that monitor synchro voltages. A power output of approximately 5VA may be obtained.

5. MODEL 3704 HIGH POWER BUFFER – The 3704 contains 3 high power buffers and associated BITE circuits. Except for its increased power capability of up to approximately 10VA AC per line and the addition of a switching circuit, it is almost identical to the 3703. It has been designed to drive an active load such as a 23TR4 Torque Receiver.

6. MODEL 3706 DIGITAL-TO-DC MULTIPLYING CONVERTER – The 3706 converts a serially transmitted 12-bit digital word into a DC output of desired scaling. The digital input may be programmed for binary (2's complement) when unipolar output is desired, or for offset binary when bipolar output is required.

7. MODEL 3707 DIGITAL-TO-AC MULTIPLYING CONVERTER – The 3707 converts a serially transmitted 12-bit digital word to an AC output of desired scaling, just as in the 3706. The digital input may be programmed for unipolar or bipolar output.

8. MODEL 3717 TURN-ON SEQUENCE CONTROL – The 3717 ensures that the power supply current drain is not exceeded when power is applied to the high power torque loads in the system. Such a condition could occur upon system turn-on as a result of large angular errors in more than one torque receiver. The 3717 overrules in sequence the disabling of the high power buffer amplifiers for 2 seconds.

9. MODEL 5480 MICROPROCESSOR – Operating in conjunction with the interface cards, the 5480 performs 2 basic functions: (a) receives data from a system such as the IRS, reprocesses the data and supplies it in the required form to a particular peripheral system, such as a Weapons Control Computer, Portable Bridge and Mark 29 Navigator; (b) receives data from the associated peripheral system, reprocesses the data and transmits it in the required form to the IRS type system.

10. MODEL 5481 RS422 INTERFACE – The 5481 provides the interface between an RS422 output channel and a 5480 Microprocessor Card. Under microprocessor control, the 5481 is fully duplexed and can transmit and receive data simultaneously.

11. MODEL 5482 ICI (1MHz SERIAL DATA BUS) INTERFACE – The 5482 interfaces an associated 5480 Microprocessor Card with an external ICI compatible equipment. It enables the 5480 to transmit and/or receive data from the associated peripheral system. A handshaking routine precedes each data transfer so that data passes between the 5482 and an external device at the receiver's rate.

12. MODEL 5483 PROPELLER AXIS INTERFACE – The 5483 interfaces propeller axis shaft signals with an associated 5480 Microprocessor Card. It receives differential signals from a transducer on the propeller axis shaft and transforms the signal into a single ended form. The signals are then buffered and routed to the associated microprocessor card for decoding

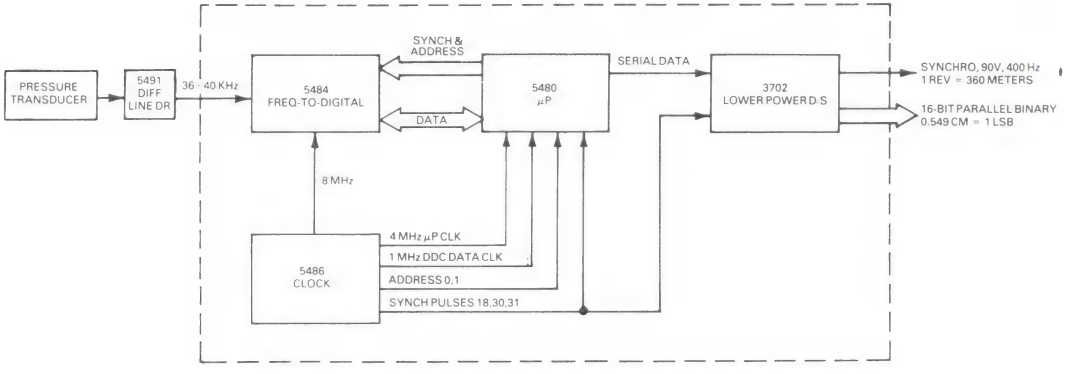


FIGURE 3. SIMPLIFIED DEPTH SYSTEM (COMBINED FROM 5 BUILDING-BLOCK P.C. CARDS)

13. MODEL 5484 FREQUENCY-TO-DIGITAL CONVERTER – This card converts a 36 to 40KHz signal from a quartz pressure transducer to a digital value that is a function of depth. It also contains ROMs and an ALU which are used with an associated 5480 microprocessor card.

14. MODEL 5486 CLOCK GENERATOR – This card generates the clock and timing pulses used for system synchronization. In an active redundant system, the circuits are configured such that the primary card normally supplies the various timing signals. If a fault is detected in the primary, the secondary card is automatically enabled, thus preventing a system failure.

15. MODEL 5487 PARALLEL-TO-SERIAL CONVERTER – This card is used in conjunction with each S/D converter channel. It is basically a parallel-to-serial converter which accepts 18 data bits, 4 validity bits, various select and address bits and converts them into a 32-bit serial data word which is multiplexed onto the internal serial bus.

16. MODEL 5489 DECIMAL/HEXADECIMAL DISPLAY CARD — The 5489 is used in conjunction with a 5481 RS422 Interface Card, a 5480 Microprocessor Card, a binary display and a data entry keyboard. Integral with the 5489 is an 8-digit decimal display and a 5-digit hexadecimal keyboard display.

17. MODEL 5490 PARALLEL INPUT ISOLATION – The 5490 provides galvanic isolation for parallel data inputs. Typical applications include the isolation of BCD inputs of the Echo Sounder and discrete status bits of the Mark 29 and Sagem Compasses.

TYPICAL ACTIVE-REDUNDANT HEADING CHANNEL

Figure 2 depicts a system which has been assembled from the S-Series Building-Block P.C. cards. This typical system has been configured to interface with the shipboard equipment which requires heading information. The primary channel of this active redundant system utilizes the Model 3700 and 3701 S/D card for a 2-speed high resolution conversion. The selection of primary or secondary heading is normally made by the shipboard Auto-Pilot Computer. However, in the event of a fault with the primary, the associated 5480 and 5481 cards automatically makes the new selection and notifies the other microprocessor cards of this decision. Except for the switches, all of the above system can be implemented with the S-Series Building-Block P.C. cards.

SIMPLIFIED DEPTH SYSTEM – A simplified depth system can be implemented with the use of only 5 S-Series P.C. cards (Figure 3). This simplified system provides 90V, 400Hz synchro output scaled to 1 revolution equalling 360 meters. It also provides a 16-bit parallel binary output where 1 LSB is equivalent to 0.549 centimeters. The 5491 Differential Line Driver card accepts the low level input from a pressure transducer. It would be located close to the transducer while the 5484, 5486, 5480 and 3702 cards would be located in a separate enclosure located in the electronics compartment of the boat.

For further information and system configuration assistance utilizing the S-Series cards, contact our systems marketing group

SECTION N
SOLID-STATE POWER CONTROLLERS

PRODUCT SUMMARY TABLE

MODEL	PACKAGE	DESCRIPTION/FEATURES	PAGE
SSP-21110 Series	2.740 x 1.34 x 0.29 inches	The SSP-21110 Series of 28 Vdc Solid- State Power Controllers are Remote Solid-State Circuit Breakers with I^2t trip characteristics and status outputs. Using Power MOSFET switches, these Power Controllers offer low 'on' resistance, low voltage drop, high off impedance, and low power dissipation.	N-2
SSP-21116 Series	2.0 x 3.0 x 0.33* inches *0.68 including pins	The SSP-21116 Series of 270 Vdc Solid- State Power Controllers are Remote Solid-State Circuit Breakers with I^2t trip characteristics and status outputs. Using Power MOSFET switches, these Power Controllers offer low 'on' resistance, low voltage drop, high off impedance, and low power dissipation.	N-10

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

28 VDC SOLID-STATE POWER CONTROLLERS

DESCRIPTION

The SSP-21110 Series of 28 Volt, dc, Solid-State Power Controllers (SSPCs) replace electromagnetic circuit breakers and solid-state relays rated from 2 through 25 amperes. These SSPCs offer status outputs and permit external input logic control so that they may be remotely located near to the load. There are five models in the series, differing only in rated current, so that fault and I^2T trip characteristics can be selected to protect wiring and loads.

Using Power MOSFET switches, these Power Controllers offer low "on" resistance, low voltage drop, high "off" impedance, and low power dissipation. Built with Power MOSFETs and custom monolithics and using thick-film hybrid technology, they offer small size, low power, and high reliability.

Built-In-Test (BIT) has been provided to monitor, in real time, the status of the internal circuitry as well as circuitry external to the SSPC. This BIT monitors MOSFET failure and control circuit failure.

The SSP-21110 Series will operate over the full MIL temperature range from -55°C to +125°C with no derating, see ordering information.

APPLICATIONS

Designed to replace circuit breakers in land, air, and space vehicles, these Solid-State Power Controllers provide status outputs for light and heavy overloads as well as minimum load current.

FEATURES:

- ***True I^2T Protection***
- ***Isolated Control Circuitry***
- ***Status Outputs***
- ***Instant Trip Protection***
- ***Low Power Dissipation***
- ***Solid-State Reliability***

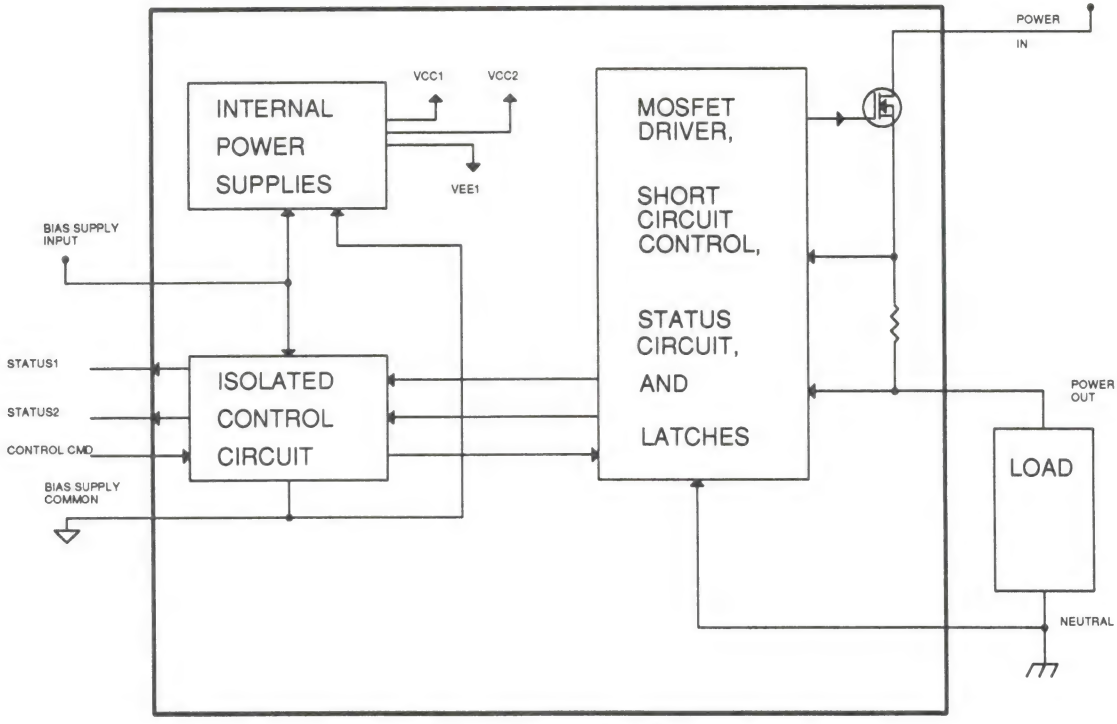


FIGURE 1. SSP-21110 BLOCK DIAGRAM

TABLE 1. ABSOLUTE MAXIMUM RATINGS		
PARAMETER	UNIT	VALUE
Power Input To Power Ground	Vdc	50 continuous 100Volts, 50ms transient
Control Input To Signal Ground	Vdc	-0.5 to +7.0
Power Ground To Signal Ground	Vdc	-100 to +100
Bias voltage	Vdc	-0.5 to +7.0
Pin-to-Case	Vdc	-1000 to +1000
Lead Temperature (soldering)	°C	+300
Junction Temperature	°C	+150

TABLE 2. RECOMMENDED OPERATING CONDITIONS		
PARAMETER	UNIT	VALUE
Power Input To Power Ground	Vdc	+9.0 to +40.0
Control Input To Signal Ground	Vdc	+4.5 to +5.5
Power Ground To Signal Ground	Vdc	-40 to +40
Bias voltage	Vdc	+4.5 to +5.5

TABLE 3. SSP-21110 SPECIFICATIONS (see notes 1 and 2)			
PARAMETER	CONDITIONS	UNIT	VALUE
CONTROL CIRCUIT			
Logic Type			TTL/CMOS compatible
Bias Supply Current	V_{CC} = 4.5 to 5.5Vdc	mA	25typ
Control Turn-On Voltage		V	2.0 to 5.5
Control Turn-Off Voltage		V	-0.5 to 0.8
Control Input Current	control voltage = 5.0V	µA	50max
Control Input Current	control voltage = 2.4V	µA	50max
Control Input Current	control voltage = 0.8V	µA	-50min
Status Output Voltage	V_{CC}= 4.5V, I_{OL}= 2.5mA	V	0.4max
Status Output Voltage	V_{CC}= 4.5V, I_{OH}= -1.0mA	V	2.4min
Status Truth Table	see table 5		
POWER CIRCUIT			
Max. Continuous Current			See Table 4
'On' Resistance			See Table 4
Power Dissipation			See Table 4
Power Out Leakage Current to Power Ground	Power In = 9 - 40V (see note 2)	mA/A	0.1max
Max Load Capacitance for Start-Up	Power In = 9 - 40V (see note 2)	µF/A	36typ
Signal to Neutral Ground Isolation	at 100Vdc	pF	1000typ
Output Capacitance	see note 2	pF/A	300typ
Trip Reset Time		ms	30min
Rupture Capacity	Unlimited	A	Unlimited
Output-to Input Parasitic Diode, Continuous Current Per Amp Of Rated Current	Power Out Voltage > Power In Voltage	A	1.0typ
Output-to Input Parasitic Diode, Pulsed Current Per Amp Of Rated Current	Power Out Voltage > Power In Voltage Pulse Width ≤ 100µS	A	4.0typ

TABLE 3. SSP-21110 SPECIFICATIONS (continued) (see notes 1 and 2)			
PARAMETER	CONDITIONS	UNIT	VALUE
POWER CIRCUIT (continued)			
Output-to Input Parasitic Diode, Forward Voltage at Continuous Current	Power Out Voltage > Power In Voltage	V	1.8max
Isolation Resistance, Any Pin to Case	Pin-to-Case Voltage = 100Vdc	MΩ	50min
Isolation Resistance, Power Ground to Signal Ground	Power Ground to Signal Ground Voltage = 50Vdc	MΩ	50min
Voltage Drop	across pins 6&7, 9&10	Vdc	0.25max
Trip Characteristics	see figure 2		
Response Time	see figure 3		
TEMPERATURE RANGE			
Operating (Case)		°C	-55 to +125
Storage		°C	-55 to +150
THERMAL RESISTANCE			
Case to Sink (θ_{CS})		°C/W	0.5
Case to Ambient (θ_{CA})		°C/W	12
Temperature Rise, Junction-to-Case	Rated Load	°C	10
PHYSICAL CHARACTERISTICS			
Size	see figure 4		
Weight		g	65

Notes:
1. -55°C ≤ Case Temperature ≤ 125°C.
2. 'A' is Amps of Rated SSPC Current.

TABLE 4			
PART NUMBER	I-MAX* (Amps)	'ON' RESISTANCE (Ohms)**	POWER DISSIPATION (Watts)**
SSP21110-002	2	0.1	0.6
SSP21110-007	7	0.03	1.6
SSP21110-015	15	0.015	3.5
SSP21110-020	20	0.012	5.0
SSP21110-025	25	0.012	7.7

* I-MAX is the maximum continuous current.
** Specified for -55°C to +105°C; increases 0.6%/°C between +105°C and +125°C.

Note: Other Amp ratings are available, consult factory.

N

FUNCTIONAL DESCRIPTION

The SSP-21110 series of Solid-State Power Controllers incorporate the wire protection feature of electromechanical circuit breakers and the reliability of solid-state relays. In addition to the solid-state relay's input logic compatibility, the SSP-21110 series provide logic compatible status outputs.

A TTL/CMOS compatible input provides external control of the power switch's "ON/OFF" state. A logic high on this control input turns the power to the load "on". A logic low will turn the power switch off, which removes power from the load.

In the event of an overload, the SSP-21110 series will trip, just like a circuit breaker, and automatically remove power from the load. In order to turn back on, the control input must be brought to a logic low, and then returned to a logic high state.

As in a circuit breaker, the SSPC's time to trip depends on the current level. Slight overloads will cause longer trip times. Heavy overloads will cause shorter trip times. The fault ("Instant Trip") and I^2T trip curve, Figure 2, shows the trip time as a function of current for a single trip or repetitive trips with at least 10 seconds between trip and turn on. Attempts to repeatedly turn on into an overload will result in the thermal memory shortening each trip time. This "memory" protects the wire, load, and the Solid-State Power Controller.

The status lines are TTL/CMOS compatible outputs which reflect the state of the SSPC, the load and the Built-In-Test (BIT) circuits. The status permits an external subsystem to monitor and ultimately control the SSPC. Table 5 defines the status lines' states which indicate the various states of the SSPC. Further explanation of the status lines appears in the applications information section.

The SSP-21110 series SSPCs are characterized by their current rating and maximum "on" resistance listed in Table 4. These parameters are established by the number of Power FETs placed in parallel within the SSPC.

The trip function is implemented by two separate circuits, a true I^2T trip comparator and a short circuit fault comparator. They are independent of each other but work together to protect the system.

If the load current is less than 110% of rated current, the SSPC will never trip. If the load current is greater than 145%, the SSPC will always trip.

For load currents less than 800%, the trip time can be found from Figure 2 by drawing a horizontal line on Figure 2 at the current level of interest. The SSPC will always trip at a time between the two curves. This is true I^2T tripping.

When the SSPC trips in accordance with the I^2T characteristics, the fall time is 200µs, maximum.

For load currents greater than 1200%, the SSPC will turn off in less than 25µs. Between 800% and 1200%, the SSPC will turn off in a time less than the "max. trip limit" shown in Figure 2 and may turn off in less than 25µs. When the SSPC turns off under these fault conditions, the fall time is less than 25µs.

While the SSPC will always turn off in less than 25µs when the load current is greater than 1200%, the actual current may 'spike'

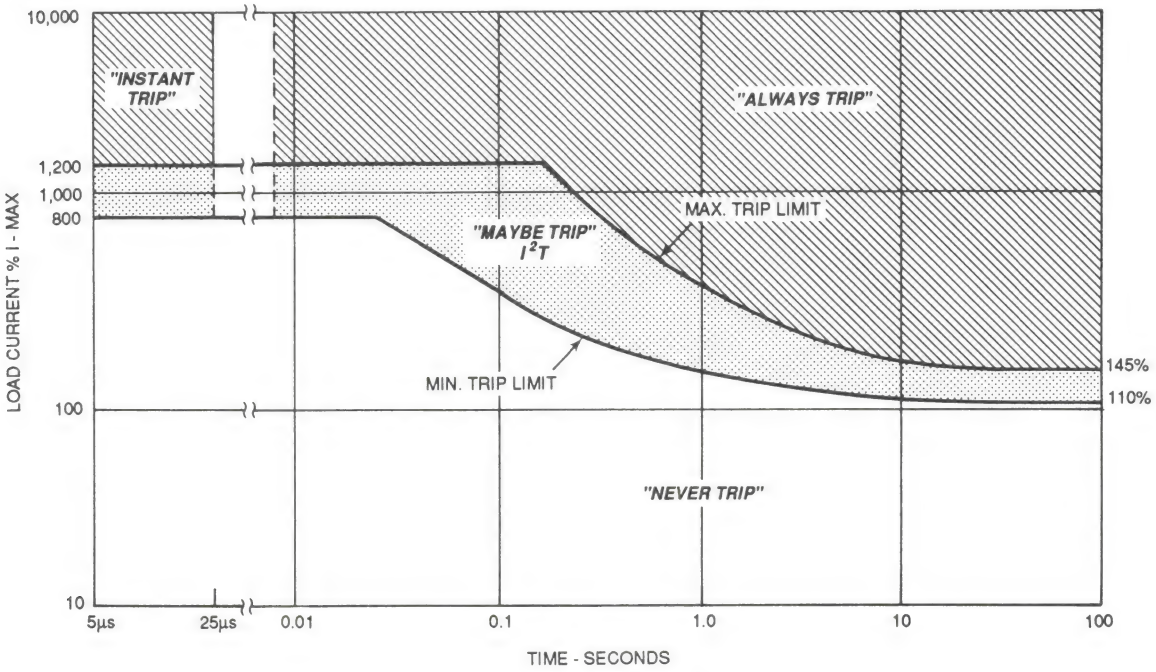


FIGURE 2. TRIP CHARACTERISTICS

to a value higher than 1200% due to circuit delays. The MOSFETs inherently self-limit the maximum current, depending on the number of MOSFETs and their rating.

During turn-on and turn-off the rise and fall time of the output voltage is controlled to be less than 200µs. This value is a compromise between faster response time with a greater amount of RFI and EMI generated, and slower response time with less RFI and EMI but greater power dissipated in the SSPC during transitions. Since the Power MOSFET switches are not saturated during transitions the switching power dissipation is much greater than the static dissipation, and longer transitions result in a larger temperature rise. If the SSPC is rapidly turned on and off, the high average dissipation could result in a significant temperature rise in the SSPC. For this reason do not turn the SSPC off and on more rapidly than 30 msec. This will limit the maximum temperature of the switches to a safe level.

The SSP-21110 has been designed to dervive its internal power requirements from the bias supply input (5Vdc).

APPLICATIONS INFORMATION

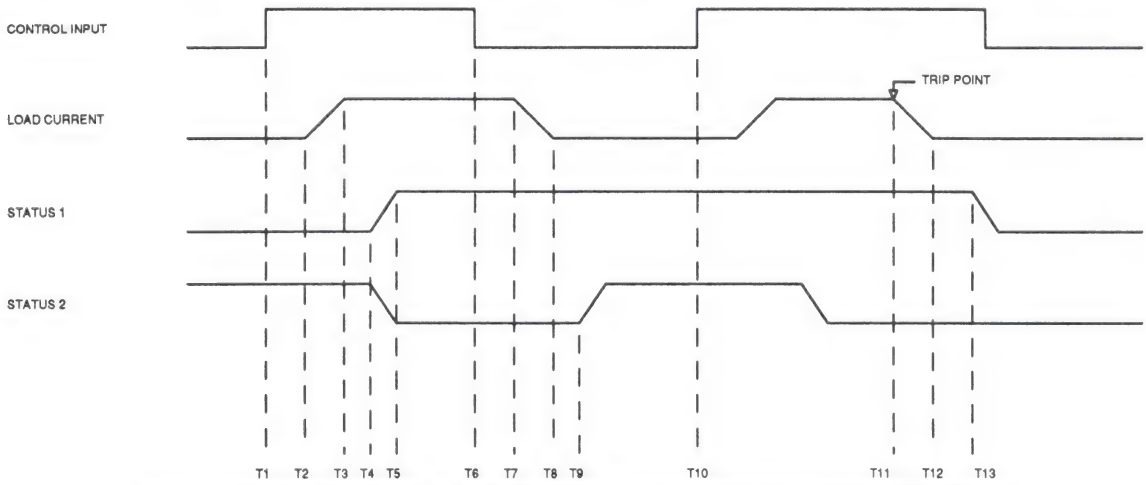
Selection

The selection of a proper sized SSPC is essential for protection of the wire and load. This selection should be based on the steady state and transient overload currents.

The shape of the trip curve (I^2T) is selected as optimum to protect the system wiring. The power dissipated in the wire is the wire resistance times the load current squared, and the temperature of the wire is determined by the length of time that this power is being dissipated. This makes the wire temperature proportional to the current squared times the on time. Since the trip curve follows this same characteristic the SSPC can accurately predict the wire temperature rise as a result of overloads and remove load current before the wiring is damaged from overtemperature. Of course, the wire I^2T product should be greater than the SSPC I^2T product for the SSPC to protect the wire.

Precautions

When a short circuit causes turn off of the SSPC, precautions have to be taken to limit the transient voltages generated by the wire inductance. The magnitude of this voltage is L*di/dt where "L" is the wire inductance in Henries and "di/dt" is the rate of change of output current. If the SSPC turns off in 10 µsec from



SOLID-STATE POWER CONTROLLER TIMING at 28Vdc.				
TIME	DESCRIPTION	MAXIMUM	UNIT	NOTES
T1-T2	TURN-ON DELAY	150	µs	
T2-T3	CURRENT RISE TIME	200	µs	
T1-T4	STATUS 1 & STATUS 2 TURN-ON DELAY	7.5	ms	
T4-T5	STATUS 1 & STATUS 2 RISE AND FALL TIME	20	ns	
T6-T7	TURN-OFF DELAY	130	µs	
T7-T8	CURRENT FALL TIME	200	µs	
T6-T9	STATUS 1 & STATUS 2 TURN-OFF DELAY	5.0	ms	
T10-T11	TRIP TIME AFTER TURN-ON	SEE FIG. 2	s	
T11-T12	CURRENT FALL TIME AFTER TRIP	200	µs	LOAD CURRENT < 800%
T11-T12	CURRENT FALL TIME AFTER TRIP	25	µs	LOAD CURRENT > 1200%
T11-T13	TRIP TURN-OFF STATUS 1 DELAY	5.0	ms	

FIGURE 3. SOLID-STATE POWER CONTROLLER TIMING

a 250 amp overload (1000% for 25 amp unit) with a wire inductance of only 10 µH it would generate a spike of 125 volts. This exceeds the voltage rating of the MOSFETs. In order to provide protection from these transients, transient voltage suppressors should be used between the SSPC Neutral and the Power In and between the SSPC Neutral and Power Out terminals. The rating of the transient voltage suppressors should be selected so that at the maximum expected short circuit current, the transient voltage suppressor voltage drop would not exceed the SSPC voltage rating, and the power to be dissipated can be safely absorbed without transient suppressor failure.

While circuit inductance can cause high voltage transients during turn off, lack of circuit inductance can cause current transients prior to turn off. If the output of the SSPC is shorted and there is no circuit inductance, the current from the source can rise instantaneously to a high value. The SSPC will limit the current to about 100 times its rating (10,000%). Circuit inductance will limit the rate of rise of this current. The SSPC can take 25µs to turn off. The current will always overshoot the 1200% maximum level of the SSPC due to this 25µs delay. If the current rises slowly due to circuit inductance, the overshoot will be negligible; if the current rises quickly, the overshoot will be more significant. In any case, the current spike will be less than 25µs.

In most real applications, there will always be significant circuit inductance. The problem to guard against is voltage transients, not current transients.

When testing individual SSPCs, be careful to simulate actual system conditions.

Power-On Reset

When power is first applied, the SSPC will be off regardless of the CONTROL CMD input. If the CONTROL CMD input is a logic low, the SSPC will turn on by bringing the CONTROL CMD to a logic high. If the CONTROL CMD input is at a logic high when power is applied, the SSPC may be turned on by cycling the CONTROL CMD input to a logic low and then to a logic high. The system controller can be programmed to do this cycling of the CONTROL CMD input. Subsequent loss of the bias supply power causes the SSPC to turn off. Re-application of the bias supply power again causes a power-on reset. Loss of power to the POWER IN terminals does not turn off the SSPC and re-application of this power does not cause a power-on reset.

Status Codes

This section contains a fuller explanation of the conditions and meaning of the status codes shown in Table 5. Each paragraph number corresponds to the STATE in Table 5.

The first four conditions show the control input has commanded the SSPC to be off.

1) The SSPC has failed or shorted to ground. STATUS 1 indicates the load is drawing current but the SSPC should be off.

2) The SSPC has failed. STATUS 1 indicates the load is drawing current; STATUS 2 indicates the Power MOSFET switch is on; the SSPC should be off.

3) Normal off condition. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET switch is off.

4) The SSPC has failed or STATUS 2 has shorted to the bias supply. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET is on ; the SSPC should be off.

The next four conditions show the control input has commanded the SSPC to be on.

5) The SSPC has failed or there is a short to ground on the STATUS 2 output. STATUS 1 indicates the load is drawing current but STATUS 2 indicates the Power MOSFET switch is off.

6) Normal on condition. STATUS 1 indicates the load is drawing current and STATUS 2 indicates the Power MOSFET switch is on.

7) Tripped condition. STATUS 1 indicates the load is not drawing current and STATUS 2 indicates the Power MOSFET switch if off. The SSPC can be turned back on by cycling the input control to a logic low and then back to a logic high. If the excessive load has not been removed, the SSPC will trip again.

8) No load current. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET switch is on.

TABLE 5

STATE	INPUT CONTROL	OUTPUT STATUS 1 (see note 2)	OUTPUT STATUS 2 (seenote 3)	POWER CONTROLLER AND LOAD STATUS
1	L	L	L	SSPC failure or short to ground.
2	L	L	H	Load 'on'; showing SSPC failure.
3	L	H	L	Load 'off' showing normal 'off' condition.
4	L	H	H	SSPC failure or STATUS 2 shorted to bias supply.
5	H	L	L	SSPC failure or short to ground on STATUS 2 line.
6	H	L	H	Load 'on' showing normal 'on' condition.
7	H	H	L	Load 'off'; showing 'trip' (see note 1).
8	H	H	H	Normal power out with load < 5% of rated SSPC current.

NOTES:
1) Any trip condition per Figure 2.
2) STATUS 1 indicates a logic low when the load is > 15% of rated SSPC current.
3) STATUS 2 indicates a logic high when the Power MOSFET switch is on.

Loads

The SSP-21110 series can be used with any type of load: any combination of inductive, resistive, and capacitive. In addition, they can be used with dc motors and lamps.

Inductive loads require protecting the SSPC against voltage transients. See the section on Precautions above.

Capacitive loads require comparing the load in-rush current to the trip curve of Figure 2. The in-rush current must be below the minimum trip curve to avoid tripping on the in-rush current.

Capacitive loads can present a discharge problem. The SSPCs use Power MOSFETs as the switching element. The MOSFETs contain a parasitic diode which will be forward biased if the SSPC power output terminal is more positive than the power input terminal. If the 28Vdc source is turned off while a charge is held on the capacitive load, this diode will turn on and discharge the load through the generator. The SSPC can carry a reverse current equal to its forward current rating; however, the dissipation with reverse current is up to seven times the forward current dissipation for the same current. The user must ensure that the maximum case temperature is not exceeded.

Incandescent lamps must be treated like capacitive loads for in-rush current. Since they do not store charge, they do not present a discharge problem.

DC motors also must be treated like capacitive loads for in-rush current. If they continue rotating when power is removed, reverse current is a possibility due to back EMF. Voltage transients must also be considered when using dc motors as loads on SSPCs.

Heatsinking

The SSP-21110 series are designed so that the junction temperature can never exceed its maximum rating if the case temperature is held to 125°C or less. Heatsinking is recommended to keep the case temperature to 125°C when operating at high ambient temperatures. The SSPCs may be operated at room temperature without a heat sink. The maximum ambient temperature, T_A, for operation without a heat sink is $125 - P_d \times \theta_{CA}$ (where P_d is the power dissipation from Table 4 and θ_{CA} is the thermal resistance from case-to-ambient from Table 3).

The same expression is used for finding the maximum ambient temperature with a heat sink except θ_{CA} is now the sum of the thermal resistance from case-to-sink and from sink-to-ambient.

No Offset Voltage

The Power MOSFET used in the DDC SSPCs have no inherent voltage offset. The voltage drop across the Power MOSFET is solely dependant on the current flowing through the device and its "ON" resistance.

Bipolar transistors, on the other hand, have an inherent dc offset voltage to which is added a voltage drop proportional to the devices' "ON" resistance and the current flowing through it. It is this inherent offset voltage that is missing from the power MOSFET. The Power MOSFET in many applications, leads to a lower voltage drop and power dissipation as an SSPC switch. In addition the Power MOSFETs driver logic requirements are much simplier, especially when multiple MOSFETs are used, as in the SSPC product.

No Secondary Breakdown, and Paralleling SSPCs

A bipolar transistor has a set of current-voltage limits that form an envelope that cannot be exceeded; this is known as the safe operating area of the device. If this envelope is exceeded local hot spots will occur. These hot spots conduct currents more readily then adjacent cool areas and tend to become hotter. This thermal runaway leads to the ultimate destruction of the device; called secondary breakdown.

The Power MOSFETs have the opposite characteristics from that of thermal runaway in bipolar devices. A local hot-spot will steer current away from itself as its resistance in this area goes up. This results in even current sharing throughout the entire device, thereby eliminating hot-spots. The inherent advantage of not having secondary breakdown is that the entire MOSFET has to exceed its temperature limitations before damage results. This characteristic makes the Power MOSFET more rugged when used for power switching then bipolar devices.

Due to the current sharing aspects of the power MOSFET, they can be placed in parallel and share the load equally. DDC, has a standard 28 Vdc 80 AMP power module which uses this technique.

Isolation of Control and Status

The SSPC was designed with isolation between the load power and the five volt control logic input and the status outputs. This is necessary to prevent noise caused by transients or power spikes on the power line from adversely affecting the operation of the SSPC. Therefore the case, POWER IN, and Control Circuit are all electrically isolated. Figure 1, SSPC BLOCK DIAGRAM, shows this isolation as the "ISOLATED CONTROL CIRCUIT"; also notice the separation of the power (neutral) ground and signal (bias supply common) ground.

The electrical isolation is supported by an internal power oscillator that electrically isolates separate internal power supplies that will power the internal analog and digital monolithics. This isolation prevents load or logic ground loops from affecting the proper operation of the SSPC. The isolation also insures that a fault of the switch (MOSFET) could never propagate back into the SSPC logic or cause damage to the logic side.

OPTIONS

The following characteristics can be factory modified on special orders:

- I^2T TRIP CURVE: K-factor adjustments
- OUTPUT RISE AND FALL TIMES :
  Turn-Off and Turn-On time can be factory modified.
  (e.g., capacitive loads.)
- CURRENT RANGE
- POWER-ON RESET: Other options are available.
- INPUT CONTROL:
  TTL or CMOS or Both with Hysteresis (Schmitt trigger characteristics)
- CUSTOM PACKAGING
- OPTIONAL STATUS TRUTH TABLE (See Table 6.)

TABLE 6. OPTIONAL STATUS TRUTH TABLE

CONTROL	STATUS 1	STATUS 2	SYSTEM STATUS
LOW	LOW	LOW	SSPC failure, or Status 1 and Status 2 shorted to ground, or No Bias
LOW	LOW	HIGH	SSPC failure or Status 1 shorted to ground
LOW	HIGH	LOW	SSPC failure or Status 2 shorted to ground
LOW	HIGH	HIGH	Load is 'OFF', Normal Condition
HIGH	LOW	LOW	SSPC failure or Status 2 shorted to ground
HIGH	LOW	HIGH	Load is 'ON', Normal Condition
HIGH	HIGH	LOW	Load is 'OFF', Tripped
HIGH	HIGH	HIGH	Load is 'ON', Load < 5.0% Rated Current

Status 1 indicates a logic LOW if > 15% of the rated current is flowing.
Status 2 indicates a logic LOW if the SSPC is tripped due to overcurrent.

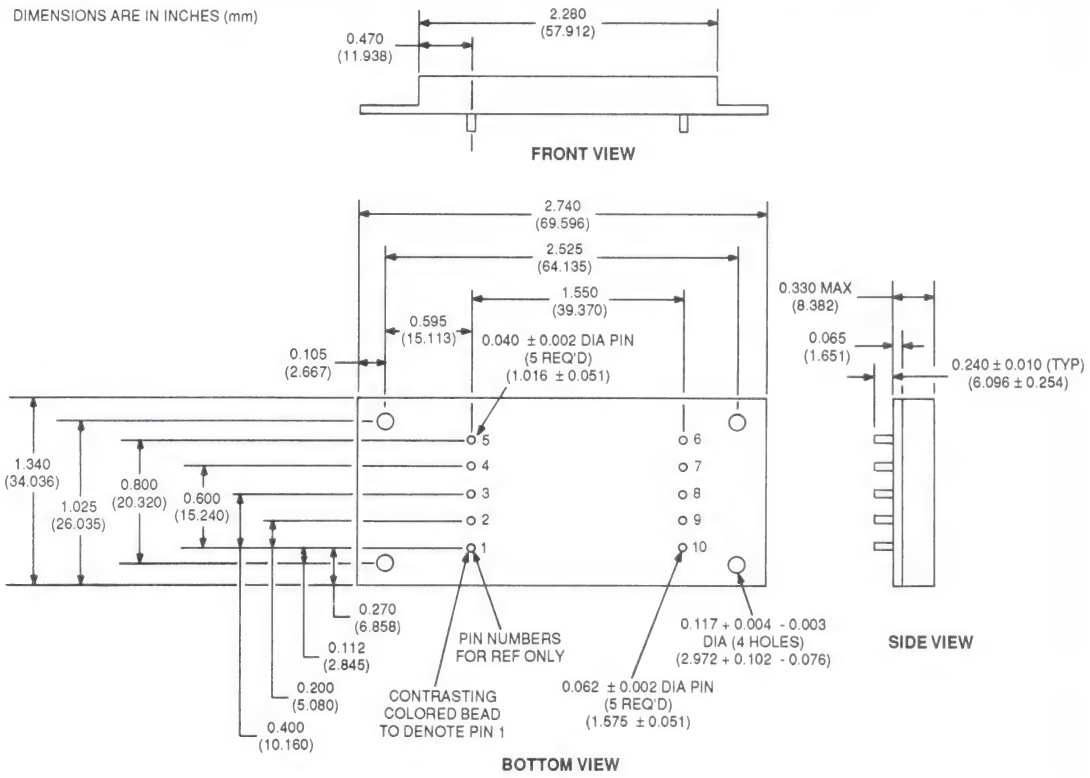


FIGURE 4. MECHANICAL OUTLINE

TABLE 7. PINOUTS

PIN	FUNCTION	PIN	FUNCTION
5	CONTROL COMMAND	6	POWER IN
4	STATUS 1	7	POWER IN
3	STATUS 2	8	NEUTRAL
2	BIAS SUPPLY COMMON	9	POWER OUT
1	BIAS SUPPLY INPUT	10	POWER OUT

ORDERING INFORMATION

SSP-21110- X XX - X

- Reliability grade:
  883B = 883B processing
  B = Screened to 883B but without QCI testing.
  Blank = Standard DDC procedures.
- X X - Current in Amps.
- Temperature Range:
  0 = -55 to +125°C

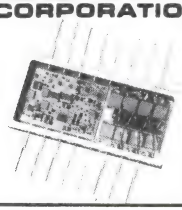
Other temperature ranges are available, consult factory.
Consult factory for other current ranges.

C

N

SSP-21116

270 VDC SOLID-STATE POWER CONTROLLERS



DESCRIPTION

The SSP-21116 Series of 270 Volt, dc, Solid-State Power Controllers (SSPCs) replace electromagnetic circuit breakers and solid-state relays rated from 5 through 15 amperes. These SSPCs offer status outputs and permit external input logic control so that they may be remotely located near to the load. There are five models in the series, differing only in rated current, so that fault and I^2T trip characteristics can be selected to protect wiring and loads.

Using Power MOSFET switches, these Power Controllers offer low "on" resistance, low voltage drop, high "off" impedance, and low power dissipation. Built with Power MOSFETs and custom monolithics and using thick-film hybrid technology, they offer small size, low power, and high reliability.

Built-In-Test (BIT) has been provided to monitor, in real time, the status of the internal circuitry as well as circuitry external to the SSPC. This BIT monitors MOSFET failure and control circuit failure.

The SSP-21116 Series will operate over the full MIL temperature range from -55°C to +125°C with no derating, see ordering information.

APPLICATIONS

Designed to replace circuit breakers in land, air, and space vehicles, these Solid-State Power Controllers provide status outputs for light and heavy overloads as well as minimum load current.

FEATURES:

- ***True I^2T Protection***
- ***Isolated Control Circuitry***
- ***Status Outputs***
- ***Instant Trip Protection***
- ***Leakage Clamp***
- ***Low Power Dissipation***
- ***Solid-State Reliability***

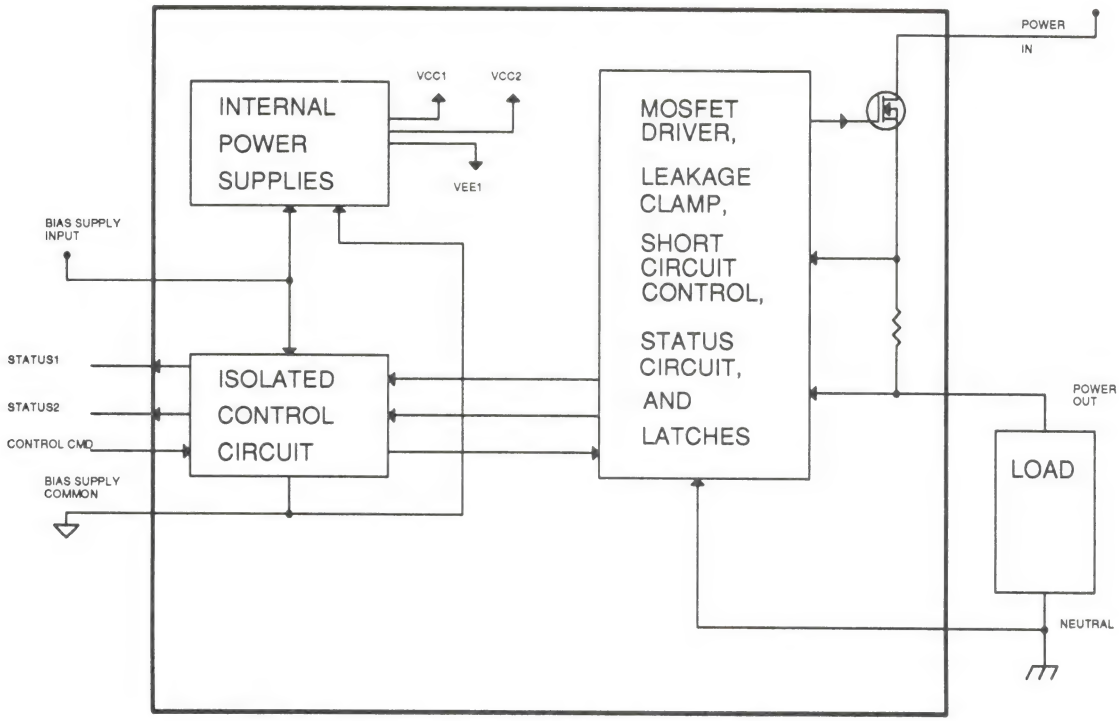


FIGURE 1. SSP-21116 BLOCK DIAGRAM

TABLE 1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	VALUE
Power Input To Power Ground	Vdc	450 continuous 500Volts, 50ms transient
Control Input To Signal Ground	Vdc	-0.5 to +7.0
Power Ground To Signal Ground	Vdc	-1000 to +1000
Bias voltage	Vdc	-0.5 to +7.0
Pin-to-Case	Vdc	-1000 to +1000
Lead Temperature (soldering)	°C	+300
Junction Temperature	°C	+150

TABLE 2. RECOMMENDED OPERATING CONDITIONS

PARAMETER	UNIT	VALUE
Power Input To Power Ground	Vdc	+60.0 to +300.0
Control Input To Signal Ground	Vdc	+4.5 to +5.5
Power Ground To Signal Ground	Vdc	-300 to +300
Bias voltage	Vdc	+4.5 to +5.5

TABLE 3. SSP-21116 SPECIFICATIONS (see notes 1 and 2)

PARAMETER	CONDITIONS	UNIT	VALUE
CONTROL CIRCUIT			
Logic Type			TTL/CMOS compatible
Bias Supply Current	V_{CC} = 4.5 to 5.5Vdc	mA	25typ
Control Turn-On Voltage		V	2.0 to 5.5
Control Turn-Off Voltage		V	-0.5 to 0.8
Control Input Current	control voltage = 5.0V	µA	50max
Control Input Current	control voltage = 2.4V	µA	50max
Control Input Current	control voltage = 0.8V	µA	-50min
Status Output Voltage	V_{CC}= 4.5V,I_{OL}= 2.5mA	V	0.4max
Status Output Voltage	V_{CC}= 4.5V,I_{OH}= -1.0mA	V	2.4min
Status Truth Table	see table 5		
POWER CIRCUIT			
Max. Continuous Current			See Table 4
'On' Resistance			See Table 4
Power Dissipation			See Table 4
Power Out Leakage Current to Power Ground	Power In = 60 - 300V (see note 2)	mA/A	0.1max
Power Out Voltage with Switch OFF	Power In = 60 - 300V No Load	V	30max
Max Load Capacitance for Start-Up	Power In = 60 - 300V (see note 2)	µF/A	4typ
Signal to Neutral Ground Isolation	at 100Vdc	pF	1000typ
Output Capacitance	see note 2	pF/A	300typ
Trip Reset Time		ms	30min
Rupture Capacity	Unlimited	A	Unlimited
Output-to Input Parasitic Diode, Continuous Current Per Amp Of Rated Current	Power Out Voltage > Power In Voltage	A	1.0typ
Output-to Input Parasitic Diode, Pulsed Current Per Amp Of Rated Current	Power Out Voltage > Power In Voltage Pulse Width ≤ 100µS	A	4.0typ

TABLE 3. SSP-21116 SPECIFICATIONS (continued) (see notes 1 and 2)

PARAMETER	CONDITIONS	UNIT	VALUE
POWER CIRCUIT (continued)			
Output-to Input Parasitic Diode, Forward Voltage at Continuous Current	Power Out Voltage > Power In Voltage	V	1.8max
Isolation Resistance, Any Pin to Case	Pin-to-Case Voltage = 100Vdc	MΩ	50min
Isolation Resistance, Power Ground to Signal Ground	Power Ground to Signal Ground Voltage = 500Vdc	MΩ	50min
Voltage Drop	across pins 6&7, 9&10	Vdc	see note 3
Trip Characteristics	see figure 2		
Response Time	see figure 3		
TEMPERATURE RANGE			
Operating (Case)		°C	-55 to +125
Storage		°C	-55 to +150
THERMAL RESISTANCE			
Case to Sink (θ_{CS})		°C/W	0.4
Case to Ambient (θ_{CA})		°C/W	6
Temperature Rise, Junction-to-Case	Rated Load	°C	10
PHYSICAL CHARACTERISTICS			
Size	see figure 4		
Weight		g	115

Notes:
1. -55°C ≤ Case Temperature ≤ 125°C.
2. 'A' is Amps of Rated SSPC Current.
3. For 2A, 5A, and 10A units the value is 1V max; for 15A unit the value is 1.5V max.

TABLE 4

PART NUMBER	I-MAX* (Amps)	'ON' RESISTANCE (Ohms)**	POWER DISSIPATION (Watts)**
SSP21116-002	2	0.460	2.0
SSP21116-005	5	0.160	4.2
SSP21116-010	10	0.085	8.7
SSP21116-015	15	0.085	19.3

* I-MAX is the maximum continuous current.
** Specified for -55°C to +105°C; increases 0.6%/°C between +105°C and +125°C.

Note: Other Amp ratings are available, consult factory.

FUNCTIONAL DESCRIPTION

The SSP-21116 series of Solid-State Power Controllers incorporate the wire protection feature of electromechanical circuit breakers and the reliability of solid-state relays. In addition to the solid-state relay's input logic compatibility, the SSP-21116 series provide logic compatible status outputs.

A TTL/CMOS compatible input provides external control of the power switch's "ON/OFF" state. A logic high on this control input turns the power to the load "on". A logic low will turn the power switch off, which removes power from the load.

In the event of an overload, the SSP-21116 series will trip, just

like a circuit breaker, and automatically remove power from the load. In order to turn back on, the control input must be brought to a logic low, and then returned to a logic high state.

As in a circuit breaker, the SSPC's time to trip depends on the current level. Slight overloads will cause longer trip times. Heavy overloads will cause shorter trip times. The fault ("Instant Trip") and I^2T trip curve, Figure 2, shows the trip time as a function of current for a single trip or repetitive trips with at least 10 seconds between trip and turn on. Attempts to repeatedly turn on into an overload will result in the thermal memory shortening each trip time. This "memory" protects the wire, load, and the Solid-State Power Controller.

The status lines are TTL/CMOS compatible outputs which reflect the state of the SSPC, the load and the Built-In-Test (BIT) circuits. The status permits an external subsystem to monitor and ultimately control the SSPC. Table 5 defines the status lines' states which indicate the various states of the SSPC. Further explanation of the status lines appears in the applications information section.

The SSP-21116 series SSPCs are characterized by their current rating and maximum "on" resistance listed in Table 4. These parameters are established by the number of Power FETs placed in parallel within the SSPC.

The trip function is implemented by two separate circuits, a true I^2T trip comparator and a short circuit fault comparator. They are independent of each other but work together to protect the system.

If the load current is less than 110% of rated current, the SSPC will never trip. If the load current is greater than 145%, the SSPC will always trip.

For load currents less than 800%, the trip time can be found from Figure 2 by drawing a horizontal line on Figure 2 at the current level of interest. The SSPC will always trip at a time between the two curves. This is true I^2T tripping.

When the SSPC trips in accordance with the I^2T characteristics, the fall time is 200µs, maximum.

For load currents greater than 1200%, the SSPC will turn off in less than 25µs. Between 800% and 1200%, the SSPC will turn off in a time less than the "max. trip limit" shown in Figure 2 and may turn off in less than 25µs. When the SSPC turns off under these fault conditions, the fall time is less than 25µs.

While the SSPC will always turn off in less than 25µs when the load current is greater than 1200%, the actual current may 'spike' to a value higher than 1200% due to circuit delays. The MOSFETs inherently self-limit the maximum current, depending on the number of MOSFETs and their rating.

During turn-on and turn-off the rise and fall time of the output voltage is controlled to be less than 200µs. This value is a compromise between faster response time with a greater amount of RFI and EMI generated, and slower response time with less RFI and EMI but greater power dissipated in the SSPC during transitions. Since the Power MOSFET switches are not saturated during transitions the switching power dissipation is much greater than the static dissipation, and longer transitions result in a larger temperature rise. If the SSPC is rapidly turned on and off, the high average dissipation could result in a significant

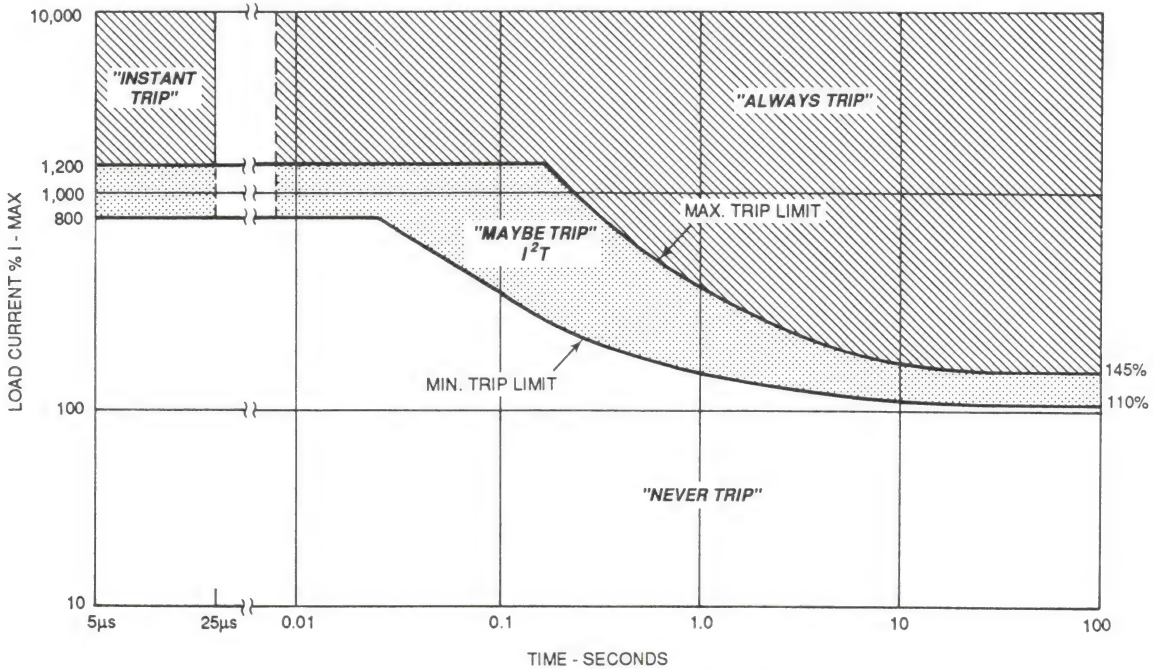


FIGURE 2. TRIP CHARACTERISTICS

temperature rise in the SSPC. For this reason do not turn the SSPC off and on more rapidly than 30 msec. This will limit the maximum temperature of the switches to a safe level.

The SSP-21116 has been designed to dervive its internal power requirements from the bias supply input (5Vdc).

APPLICATIONS INFORMATION

Selection

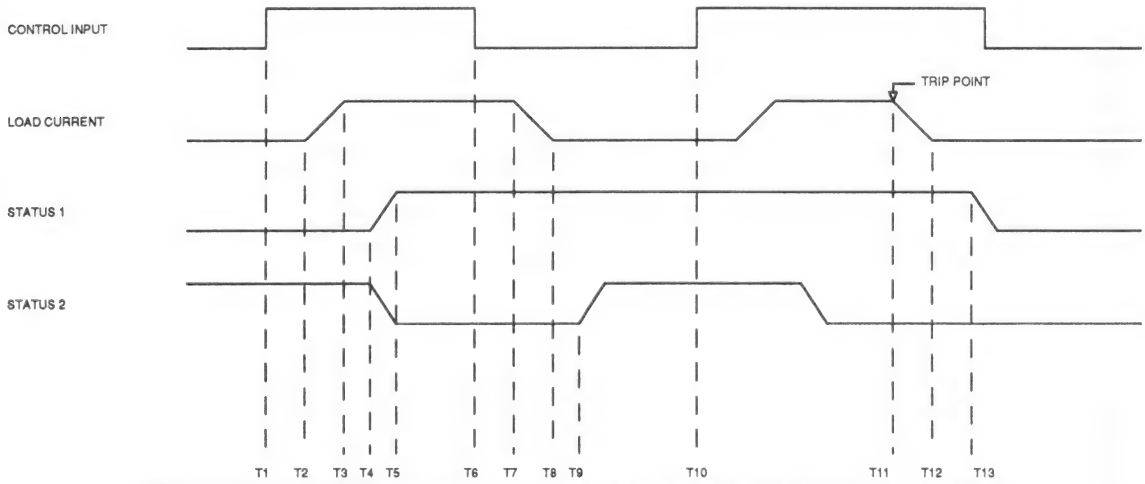
The selection of a proper sized SSPC is essential for protection of the wire and load. This selection should be based on the steady state and transient overload currents.

The shape of the trip curve (I^2T) is selected as optimum to protect the system wiring. The power dissipated in the wire is the wire resistance times the load current squared, and the temperature of the wire is determined by the length of time that this power is being dissipated. This makes the wire temperature proportional to the current squared times the on time. Since the trip curve follows this same characteristic the SSPC can accurately predict the wire temperature rise as a result of overloads and remove load current before the wiring is damaged from overtemperature. Of course, the wire I^2T product should be greater than the SSPC I^2T product for the SSPC to protect the wire.

Precautions

When a short circuit causes turn off of the SSPC, precautions have to be taken to limit the transient voltages generated by the wire inductance. The magnitude of this voltage is L*di/dt where "L" is the wire inductance in Henries and "di/dt" is the rate of change of output current. If the SSPC turns off in 10 µsec from a 150 amp overload (1000% for 15 amp unit) with a wire inductance of only 33 µH it would generate a spike of 500 volts. This exceeds the voltage rating of the MOSFETs. In order to provide protection from these transients, transient voltage suppressors should be used between the SSPC Neutral and the Power In and between the SSPC Neutral and Power Out terminals. The rating of the transient voltage suppressors should be selected so that at the maximum expected short circuit current, the transient voltage suppressor voltage drop would not exceed the SSPC voltage rating, and the power to be dissipated can be safely absorbed without transient suppressor failure.

While circuit inductance can cause high voltage transients during turn off, lack of circuit inductance can cause current transients prior to turn off. If the output of the SSPC is shorted and there is no circuit inductance, the current from the source can rise instantaneously to a high value. The SSPC will limit the current to about 30 times its rating (3,000%). Circuit inductance will limit the rate of rise of this current. The SSPC can take 25µs to turn off. The current will always overshoot the 1200% max-



SOLID-STATE POWER CONTROLLER TIMING at 270Vdc.				
TIME	DESCRIPTION	MAXIMUM	UNIT	NOTES
T1-T2	TURN-ON DELAY	150	µs	
T2-T3	CURRENT RISE TIME	200	µs	
T1-T4	STATUS 1 & STATUS 2 TURN-ON DELAY	7.5	ms	
T4-T5	STATUS 1 & STATUS 2 RISE AND FALL TIME	20	ns	
T6-T7	TURN-OFF DELAY	130	µs	
T7-T8	CURRENT FALL TIME	200	µs	
T6-T9	STATUS 1 & STATUS 2 TURN-OFF DELAY	5.0	ms	
T10-T11	TRIP TIME AFTER TURN-ON	SEE FIG. 2	s	
T11-T12	CURRENT FALL TIME AFTER TRIP	200	µs	LOAD CURRENT < 800%
T11-T12	CURRENT FALL TIME AFTER TRIP	25	µs	LOAD CURRENT > 1200%
T11-T13	TRIP TURN-OFF STATUS 1 DELAY	5.0	ms	

FIGURE 3. SOLID-STATE POWER CONTROLLER TIMING

imum level of the SSPC due to this 25µs delay. If the current rises slowly due to circuit inductance, the overshoot will be negligible; if the current rises quickly, the overshoot will be more significant. In any case, the current spike will be less than 25µs.

In most real applications, there will always be significant circuit inductance. The problem to guard against is voltage transients, not current transients.

When testing individual SSPCs, be careful to simulate actual system conditions.

Power-On Reset

When power is first applied, the SSPC will be off regardless of the CONTROL CMD input. If the CONTROL CMD input is a logic low, the SSPC will turn on by bringing the CONTROL CMD to a logic high. If the CONTROL CMD input is at a logic high when power is applied, the SSPC may be turned on by cycling the CONTROL CMD input to a logic low and then to a logic high. The system controller can be programmed to do this cycling of the CONTROL CMD input. Subsequent loss of the bias supply power causes the SSPC to turn off. Re-application of the bias supply power again causes a power-on reset. Loss of power to the POWER IN terminals does not turn off the SSPC and re-application of this power does not cause a power-on reset.

Status Codes

This section contains a fuller explanation of the conditions and meaning of the status codes shown in Table 5. Each paragraph number corresponds to the STATE in Table 5.

The first four conditions show the control input has commanded the SSPC to be off.

1) The SSPC has failed or shorted to ground. STATUS 1 indicates the load is drawing current but the SSPC should be off.

2) The SSPC has failed. STATUS 1 indicates the load is drawing current; STATUS 2 indicates the Power MOSFET switch is on; the SSPC should be off.

3) Normal off condition. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET switch is off.

4) The SSPC has failed or STATUS 2 has shorted to the bias supply. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET is on ; the SSPC should be off.

The next four conditions show the control input has commanded the SSPC to be on.

5) The SSPC has failed or there is a short to ground on the STATUS 2 output. STATUS 1 indicates the load is drawing current but STATUS 2 indicates the Power MOSFET switch is off.

6) Normal on condition. STATUS 1 indicates the load is drawing current and STATUS 2 indicates the Power MOSFET switch is on.

7) Tripped condition. STATUS 1 indicates the load is not drawing current and STATUS 2 indicates the Power MOSFET switch if off. The SSPC can be turned back on by cycling the input control to a logic low and then back to a logic high. If the excessive load has not been removed, the SSPC will trip again.

8) No load current. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET switch is on.

TABLE 5

STATE	INPUT CONTROL	OUTPUT STATUS 1 (see note 2)	OUTPUT STATUS 2 (seenote 3)	POWER CONTROLLER AND LOAD STATUS
1	L	L	L	SSPC failure or short to ground.
2	L	L	H	Load 'on'; showing SSPC failure.
3	L	H	L	Load 'off' showing normal 'off' condition.
4	L	H	H	SSPC failure or STATUS 2 shorted to bias supply.
5	H	L	L	SSPC failure or short to ground on STATUS 2 line.
6	H	L	H	Load 'on' showing normal 'on' condition.
7	H	H	L	Load 'off'; showing 'trip' (see note 1).
8	H	H	H	Normal power out with load < 5% of rated SSPC current.

NOTES:
1) Any trip condition per Figure 2.
2) STATUS 1 indicates a logic low when the load is > 15% of rated SSPC current.
3) STATUS 2 indicates a logic high when the Power MOSFET switch is on.

Loads

The SSP-21116 series can be used with any type of load: any combination of inductive, resistive, and capacitive. In addition, they can be used with dc motors and lamps.

Inductive loads require protecting the SSPC against voltage transients. See the section on Precautions above.

Capacitive loads require comparing the load in-rush current to the trip curve of Figure 2. The in-rush current must be below the minimum trip curve to avoid tripping on the in-rush current.

Capacitive loads can present a discharge problem. The SSPCs use Power MOSFETs as the switching element. The MOSFETs contain a parasitic diode which will be forward biased if the SSPC power output terminal is more positive than the power input terminal. If the 270Vdc source is turned off while a charge is held on the capacitive load, this diode will turn on and discharge the load through the generator. The SSPC can carry a reverse current equal to its forward current rating; however, the dissipation with reverse current is up to four times the forward current dissipation for the same current. The user must ensure that the maximum case temperature is not exceeded.

Incandescent lamps must be treated like capacitive loads for in-rush current. Since they do not store charge, they do not present a discharge problem.

DC motors also must be treated like capacitive loads for in-rush current. If they continue rotating when power is removed, reverse current is a possibility due to back EMF. Voltage transients must also be considered when using dc motors as loads on SSPCs.

Heatsinking

The SSP-21116 series are designed so that the junction temperature can never exceed its maximum rating if the case temperature is held to 125°C or less. Heatsinking is recommended to keep the case temperature to 125°C when operating at high ambient temperatures. The SSPCs may be operated at room temperature without a heat sink. The maximum ambient temperature, T_A, for operation without a heat sink is $125 - P_d \times \theta_{CA}$ (where P_d is the power dissipation from Table 4 and θ_{CA} is the thermal resistance from case-to-ambient from Table 3).

The same expression is used for finding the maximum ambient temperature with a heat sink except θ_{CA} is now the sum of the thermal resistance from case-to-sink and from sink-to-ambient.

No Offset Voltage

The Power MOSFET used in the DDC SSPCs have no inherent voltage offset. The voltage drop across the Power MOSFET is solely dependant on the current flowing through the device and its "ON" resistance.

Bipolar transistors, on the other hand, have an inherent dc offset voltage to which is added a voltage drop proportional to the devices' "ON" resistance and the current flowing through it. It is this inherent offset voltage that is missing from the power MOSFET. The Power MOSFET in many applications, leads to a lower voltage drop and power dissipation as an SSPC switch. In addition the Power MOSFETs driver logic requirements are much simplier, especially when multiple MOSFETs are used, as in the SSPC product.

No Secondary Breakdown, and Paralleling SSPCs

A bipolar transistor has a set of current-voltage limits that form an envelope that cannot be exceeded; this is known as the safe operating area of the device. If this envelope is exceeded local hot spots will occur. These hot spots conduct currents more readily then adjacent cool areas and tend to become hotter. This thermal runaway leads to the ultimate destruction of the device; called secondary breakdown.

The Power MOSFETs have the opposite characteristics from that of thermal runaway in bipolar devices. A local hot-spot will steer current away from itself as its resistance in this area goes up. This results in even current sharing throughout the entire device, thereby eliminating hot-spots. The inherent advantage of not having secondary breakdown is that the entire MOSFET has to exceed its temperature limitations before damage results. This characteristic makes the Power MOSFET more rugged when used for power switching then bipolar devices.

Due to the current sharing aspects of the power MOSFET, they can be placed in parallel and share the load equally. DDC, has a standard 28 Vdc 80 AMP power module which uses this technique.

Isolation of Control and Status

The SSPC was designed with isolation between the load power and the five volt control logic input and the status outputs. This is necessary to prevent noise caused by transients or power spikes on the power line from adversely affecting the operation of the SSPC. Therefore the case, POWER IN, and Control Circuit are all electrically isolated. Figure 1, SSPC BLOCK DIAGRAM, shows this isolation as the "ISOLATED CONTROL CIRCUIT"; also notice the separation of the power (neutral) ground and signal (bias supply common) ground.

The electrical isolation is supported by an internal power oscillator that electrically isolates separate internal power supplies that will power the internal analog and digital monolithics. This isolation prevents load or logic ground loops from affecting the proper operation of the SSPC. The isolation also insures that a fault of the switch (MOSFET) could never propagate back into the SSPC logic or cause damage to the logic side.

OPTIONS

The following characteristics can be factory modified on special orders:

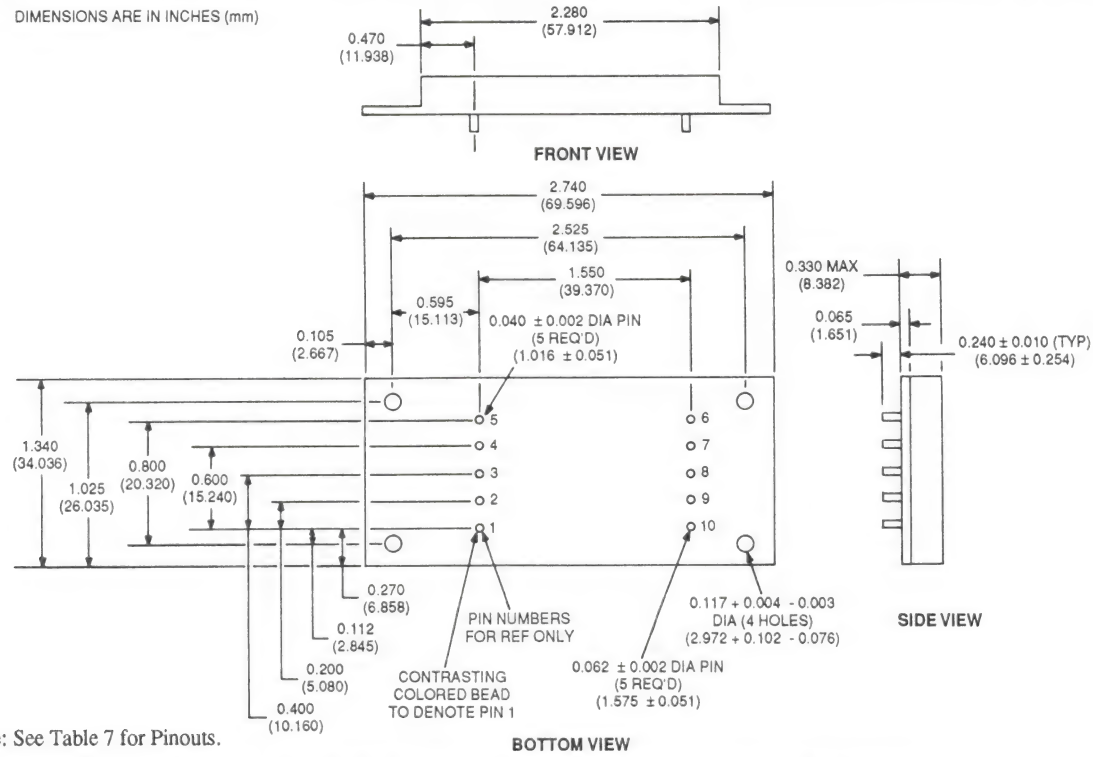
- I^2T TRIP CURVE: K-factor adjustments
- OUTPUT RISE AND FALL TIMES :
  Turn-Off and Turn-On time can be factory modified.
  (e.g., capacitive loads.)
- CURRENT RANGE
- POWER-ON RESET: Other options are available.
- LEAKAGE CLAMP: can be deleted
- INPUT CONTROL:
  TTL or CMOS or Both with Hysteresis (Schmitt trigger characteristics)
- CUSTOM PACKAGING
  DIP, Flatpack, or Smaller 2-5 Amp package.
- OPTIONAL STATUS TRUTH TABLE (See Table 6.)

TABLE 6. OPTIONAL STATUS TRUTH TABLE

CONTROL	STATUS 1	STATUS 2	SYSTEM STATUS
LOW	LOW	LOW	SSPC failure, or Status 1 and Status 2 shorted to ground, or No Bias
LOW	LOW	HIGH	SSPC failure or Status 1 shorted to ground
LOW	HIGH	LOW	SSPC failure or Status 2 shorted to ground
LOW	HIGH	HIGH	Load is 'OFF', Normal Condition
HIGH	LOW	LOW	SSPC failure or Status 2 shorted to ground
HIGH	LOW	HIGH	Load is 'ON', Normal Condition
HIGH	HIGH	LOW	Load is 'OFF', Tripped
HIGH	HIGH	HIGH	Load is 'ON', Load < 5.0% Rated Current

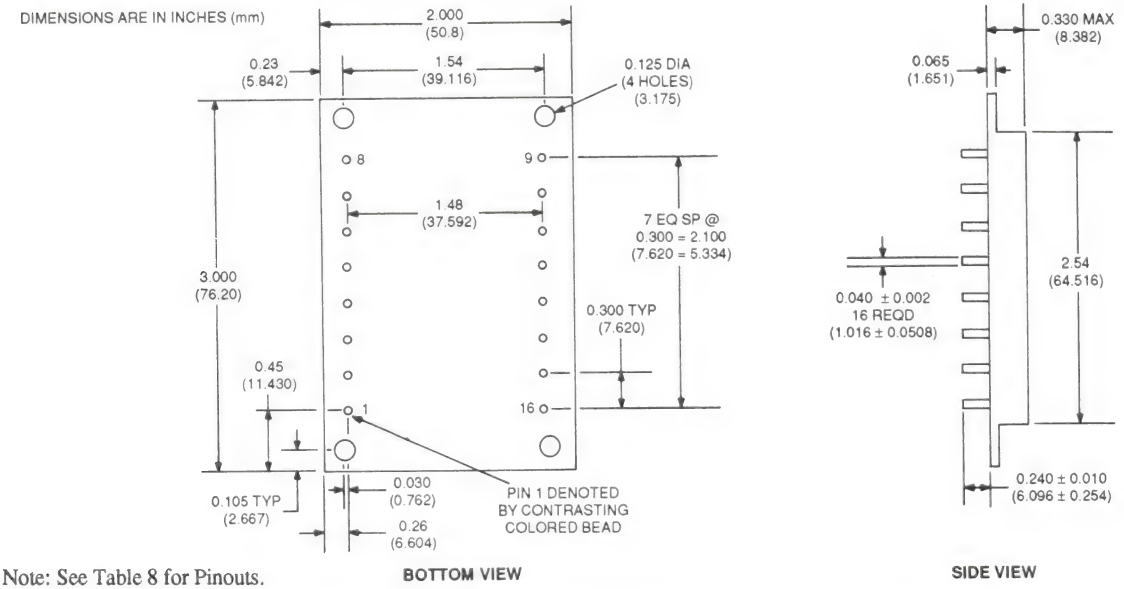
Status 1 indicates a logic LOW if > 15% of the rated current is flowing.
Status 2 indicates a logic LOW if the SSPC is tripped due to overcurrent.

N



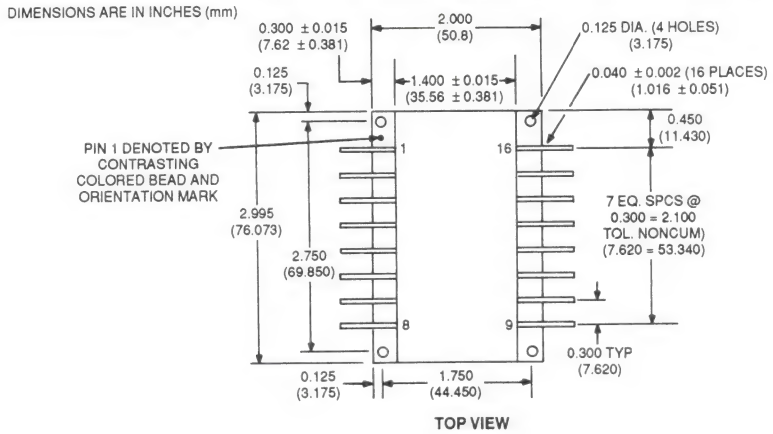
Note: See Table 7 for Pinouts.

FIGURE 4. MECHANICAL OUTLINE FOR OPTIONAL 2-5 AMP PACKAGING

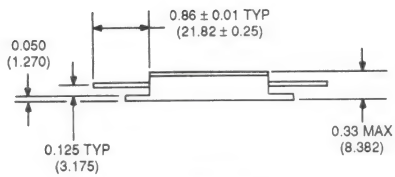


Note: See Table 8 for Pinouts.

FIGURE 5. MECHANICAL OUTLINE FOR OPTIONAL 7-15 AMP DIP PACKAGING



TOP VIEW



SIDE VIEW

FIGURE 6. MECHANICAL OUTLINE FOR STANDARD SSP-21116 PACKAGE

TABLE 7. PINOUTS FOR FIGURE 4.

PIN	FUNCTION	PIN	FUNCTION
5	CONTROL COMMAND	6	POWER IN
4	STATUS 1	7	POWER IN
3	STATUS 2	8	NEUTRAL
2	BIAS SUPPLY COMMON	9	POWER OUT
1	BIAS SUPPLY INPUT	10	POWER OUT

TABLE 8. PINOUTS FOR FIGURES 5 AND 6.

PIN	FUNCTION	PIN	FUNCTION
1	POWER OUT	16	POWER IN
2	POWER OUT	15	POWER IN
3	POWER OUT	14	POWER IN
4	NEUTRAL	13	BIAS SUPPLY COMMON
5	NC	12	BIAS SUPPLY INPUT
6	NC	11	STATUS 1
7	NC	10	STATUS 2
8	NC	9	CONTROL CMD

ORDERING INFORMATION

SSP-21116- X XX - X

- Reliability grade:
  - 883B = 883B processing
  - B = Screened to 883B but without QCI testing .
  - Blank = Standard DDC procedures.
- X X - Current in Amps.
- Temperature Range:
  - 0 = -55 to +125°C

Other temperature ranges are available, consult factory.
Consult factory for other current ranges.

N

B

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APPLICATION NOTES

The following Application Notes are available.
Send your request on company letterhead to:

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Bohemia, N.Y. 11716
Attention: Literature Department

MIL-STD-1553 DATA BUS:

Order Number	Title
AN/B-1	Designing a Remote Terminal to Talk with a MIL-STD-1553 Network.
AN/B-2	Manchester Coding Data Bus.
AN/B-3	MIL-STD-1553 B: Military Standard for Avionics Integration.
AN/B-5	MIL-STD-1553 Bus Monitor.
AN/B-6	Hybrid Trio Takes Charge of the Bus-to-CPU Interface in Military Avionics Gear.
AN/B-7	Avoiding Pitfalls in MIL-STD-1553 Transceivers.
AN/B-8	A Standard Local Network for Industrial Use.
AN/B-10	Monolithic/Superhybrids Support 1553 Interfaces.
AN/B-11	Low Cost Implementation of the SAE-AE9 RTU Production Test Plan.
AN/B-12	Test Whether a Noise Source is Gaussian.
AN/B-13	Hybrid modules help you implement a 1553B interface.
AN/B-14	Processor Interfaces To 1553 Buses.
AN/B-15	Steamline Your MIL-STD-1553 Design By Eliiminating The CPU.
AN/B-16	A Systems Approach To MIL-STD-1553 Terminal Design.
AN/B-17	8088 Microprocessor To BUS-61553 Interface.
AN/B-18	A MIL-STD-1553B NOTICE 2 Solution For Bulk Data Transfers.
AN/B-19	Upgrading from the BUS-61553 AIM-HY to the BUS-61559 AIM-HYer.
AN/B-20	Multi-Protocol RT with Shared RAM Interface and Memory Management.
AN/B-21	Stanag 3910 NATO Standard for 20MHz Fiber Bus.

LINEAR DATA CONVERTERS:

Order Number	Title
AN/L-3	Getting the Best from A-D Converters.
AN/L-7	Optimizing D/A Converter Performance.
AN/L-8	High Resolution A/D Works Better with Track-Hold.
AN/L-10	Mend Flash-Converter Flaws with a Track/Hold Cure.
AN/L-11	Watch for Superposition Errors in Data Converter Applications.
AN/L-12	A/D Simulation Programs Predicts Signal-to-Noise Ratio.
AN/L-13	Deglitched DACs Improve Vector-Stroke Displays.
AN/L-14	Fast Fourier Transform Speed Signal to Noise Analysis for A/D Converters.
AN/L-15	2-Step Conversion Increases ADC Speed.
AN/L-17	Design do's and don'ts polish 16-bit D/A performance.
AN/L-18	Histograms Simplify A/D Converter Testing.
AN/L-19	Spreadsheet Helps You Evaluate System Noise.
AN/L-20	Analog/Digital Dynamic Testing Of High-Speed A/D.
AN/L-21	Noise Power Ratio Characterizes A/D Performance For Communications.
AN/L-22	Reconstruct with the ADC-00300-605 Evaluation Board.

(continued on next page)

APPLICATION NOTES
-continued

SYNCHRO CONVERTERS:

Order Number	Title
AN/S-4	Consider Basic Parameters When Choosing S/D Converters.
AN/S-8	Shaft Position Encoders for Industrial Applications.
AN/S-12	Choosing the Right Encoder Simplifies Motor Control.
AN/S-14	A Reliable, Low Cost Approach to Shaft Position Control.
AN/S-16	Let a Modern R/D Converter Simplify Your Design Effort!
AN/S-18	Testing Of S/D Converters.

SYSTEM PRODUCTS:

Order Number	Title
AN/SP-1	Solid-state Retransmission System for Ship's Navigation: Flexibility, Availability, and Maintainability

HYBRID PROCESSING:

Order Number	Title
AN/QC-2	Certification Requirements for Hybrid Microcircuit Facilities.
AN/QC-5	Application and Use of Acceleration Factors in Microelectronics Testing.
AN/QC-6	Volume Resistivity Techniques for I-A Process Evaluation of Conductive Epoxies.
AN/QC-7	Recovering Precious Metal from Scrap Generated by the Hybrid Manufacturing Process.
AN/QC-8	Understanding Quality Conformance Inspection of Hybrid Microcircuits.
AN/QC-9	Effective Hybrid Process Controls on Assembly Operations.

POWER HYBRIDS:

Order Number	Title
AN/H-1	Hybrids Take on Power.
AN/H-2	Custom Power Hybrids.

SOLID-STATE POWER CONTROLLERS :

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AN/P-1	Hybrid Solid-State Power Controller Outperforms Conventional Circuit Breakers.

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